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Development of a monolithic pixel detector with SOI technology for ILC vertex detector

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We have been developing a monolithic type pixel detector for the ILC vertex detector with 0.2 um fully depleted SOI CMOS process. We are aiming to achieve 3 um of a single point resolution that is required for the ILC with a 20 um x 20 um pixel. Beam test result of the first prototype sensor that an amplifier and an analog memory are implemented in each pixel is presented. Design of second prototype with the time stamp function to recognize the bunch crossing information is also reported.

Summary

The ILC needs a vertex detector that has fine space-time resolution to distinguish decay of heavy flavor quark for precise measurement of the Higgs boson. We have been developing a monolithic type pixel detector with silicon-on-insulator technology (SOIPIX) which is fabricated using a 0.2 um FD-SOI CMOS process. SOIPIX has a potential of decrease in pixel size and sense node capacitance compared to a hybrid type pixel detector since there is no mechanical bump bonding. Smaller parasitic capacitance than bulk CMOS process perform higher speed and lower noise. SOI CMOS are isolated from bulk silicon, so that it is less sensitive to single event effects. Additionally, SOI CMOS has an advantage in an integration of circuit because there is no well structure for MOSFET. Therefore, SOIPIX enables us to implement a complex circuit in a small size pixel and fulfill the requirements of spatial and timing resolution for the ILC.

We are designing and evaluating prototype pixel sensor for the ILC, which is named as SOFIST (SOi sensor for FIne measurement of Space and Time) to optimize pixel size and signal readout circuit. Currently we are aiming the pixel size less than 25 um. In May 2016, SOFIST ver.2 was submitted. We integrated an amplifier, comparator, shift register, analog memory and time stamp in each pixel. Signal of charges is kept to the analog memory if it exceeds a threshold of the comparator. To achieve requirement of a single point resolution of 3 um, we will employ that the charges are spread among multi pixels. At the ILC, bunch crossing occurs every 366 ns in 1-msec-long bunch trains with an interval 200 ms. To identify a collision bunch, each pixel records the charge and time stamp of a hit. Column ADC on the chip converts the charge and timing information. These digital data have to be send to backend circuit before next beam train injection. Zero-suppression logic extracts hit pixels and reduces the data to transfer.

Our first prototype sensor, SOFIST ver.1, has the amplifier and two analog memories for storing signal charges up to two hits in a 20 x 20 um^2 pixel, and an 8-bit column ADC on the chip. We plan to test SOFIST ver.1 by using an 840 MeV electron beam in June 2016. Detection of a minimum ionizing particle and tracking of charged particle with multiple sensors are purposes.

Second prototype sensor, SOFIST ver.2, will be submitted to a multi project wafer run in May 2016. The pixel size of SOFIST ver.2 is 25 x 25 um^2. Necessary functions; the amplifier, comparator, shift register, analog memory, time stamp, column ADC and Zero-suppression logic, are implemented in the pixel chip. However, pixels for the analog memories and the time stamps are separated to evaluate the functions individually. In this presentation, recent progress of SOFIST ver.1 and 2 will be reported.

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