IC-PIX28: Pixel Detectors Read-Out in Bulk-CMOS 28nm

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IC-PIX28

Outline

- Introduction
- ScalTech
- Proposed Channel
- Pre-radiation Measurements
- Post-radiation Measurements
- Performance Resume
- Conclusion

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Introduction

Application

- **Silicon Detectors used in**
  - Digital Cameras to detect visible light
  - *Physics Experiments to detect charged particles (few fC)*
  - Astrophysics satellites to detect X-rays, γ-rays, visible and infrared light
  - Medical Imaging

- **Read-Out Systems for Pixel**
  - Matrix of Active Pixel Cells (APSs)
  - Higher number of Pixel Cells
    - Resolution increasing

- **CMOS Active Pixel Sensors (APSs)**
  - Detector: Photon to Electron conversion
  - Read-out Front-end: Charge to Voltage conversion

Introduction

Front-End for Pixel Detectors

- **Read-out electronics**
  - Sensor and read-out electronics are on-chip
    - More compatibility
    - More accuracy
    - More complexity
- **Functions:**
  - Charge to voltage conversion and voltage amplification
  - Signals digitalization
  - Signals recording and sending to data acquisition systems
- **Critical Parameters:**
  - Noise performance (SNR>10dB)
  - Power consumption (<5µW)
  - Speed (peaking time <25ns)
  - Chip size (smallest size compared to sensor)
  - Radiation Hardness (**Total Ionizing Dose (TID) up to 1Grad in 10 years)**

Introduction

Front-End for Pixel Detectors

- **Read-out electronics**
  - Sensor and read-out electronics are on-chip
    - More compatibility
- **F**
- **C**
  - Speed (peaking time <25ns)
  - Chip size (smallest size compared to sensor)
  - Radiation Hardness (**Total Ionizing Dose (TID) up to 1Grad in 10 years)**

Design in Scaled Technologies could help!

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ScalTech

ScalTech28

- **Present or under-development HEP electronics could fail**
- **<u>New electronics</u> to be designed in Scaled Technologies (<u>*ScalTech*</u>):**

  ➔ **Rad-hard performance**

  ➔ **Low-power consumption**

- **<u>INFN (National Institute of Nuclear Physics) Project</u>**

  ➔ **ScalTech28**

  - Integrated Circuits for High-Energy Physics (HEP) experiments designed in CMOS bulk 28nm technology
  - Investigating on 28nm radiation hardness
    - (see S. Mattiazzo's talk on this conference – Thursday 29th)
  - The TID tolerance increases with scaling down technological nodes (according [1])

[1] Saks, N. S., M. G. Ancona, and J. A. Modolo., Radiation Effects in MOS Capacitors with Very Thin Oxides at 80Â° K, Nuclear Science, IEEE Transactions on 31.6 (1984)

ScalTech

28nm Bulk CMOS Technology

BENEFITS (in Digital Circuits)	DRAWBACKS (in Analog Circuits)
• High Clock Frequency • Minimum Pixel Feature Size Reduction • Scaling Down • Low Power Consumption • Low Costs	• Reduced supply-voltage (0.9V) • Operating Point Issues • Intrinsic Gain reduction • More Sensibility to PVT Variations • Scaling Down not imply Low Power!

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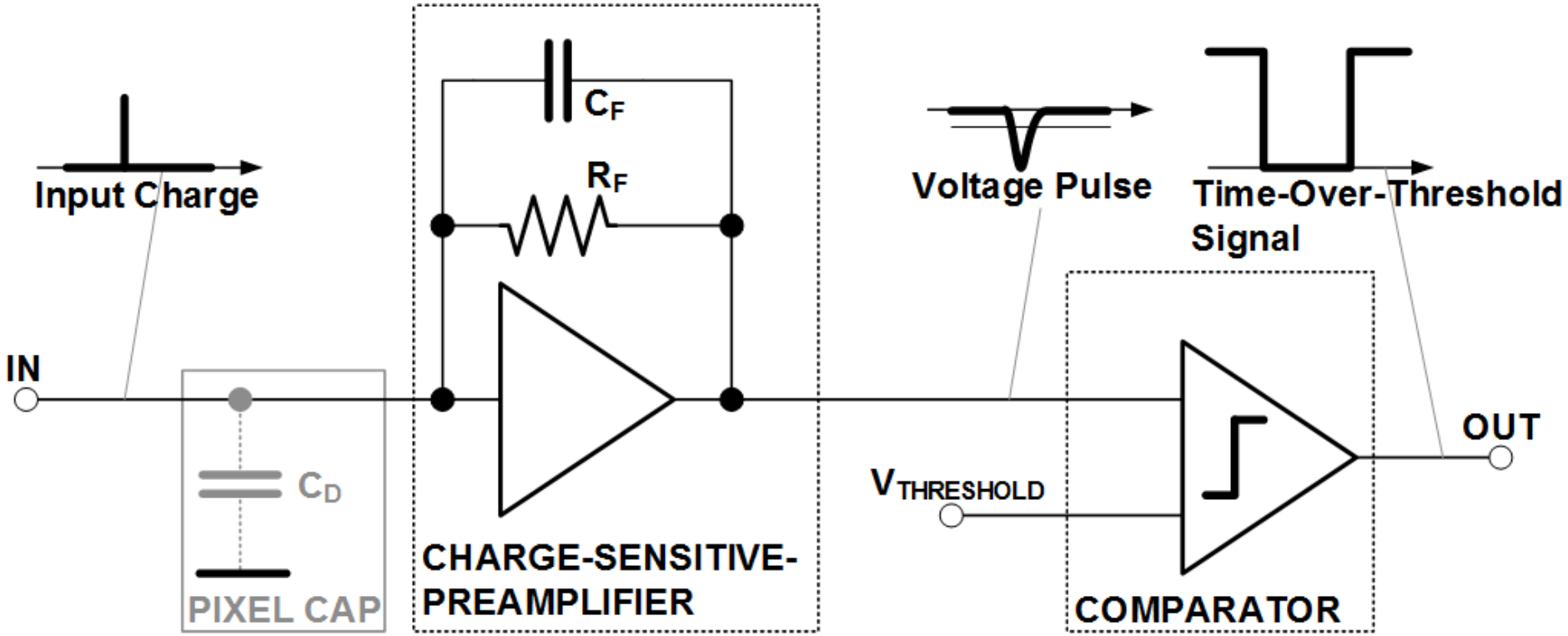
Proposed Channel

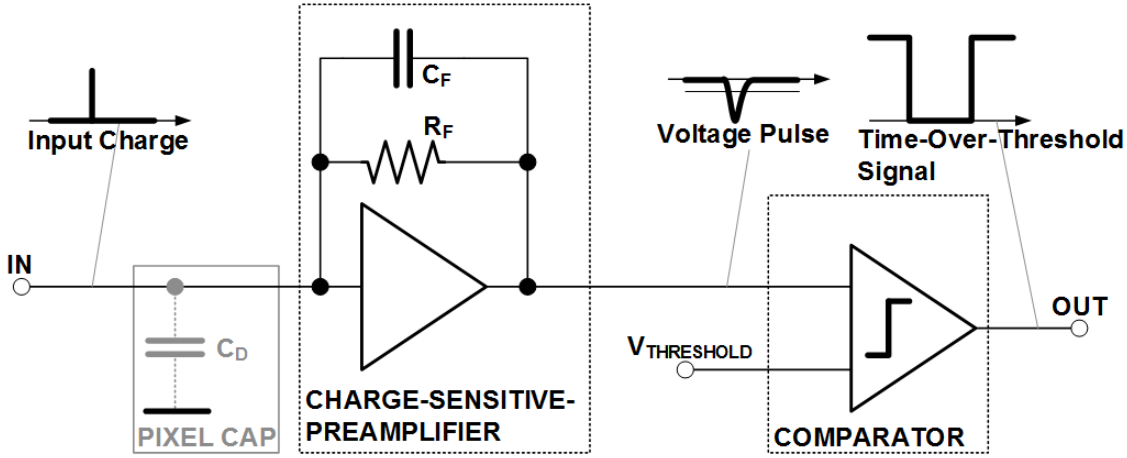
Generic Block Scheme



- **Cascade of:**
  - **Charge Sensitive Preamplifier (CSPreamp)**
    - Charge to Voltage conversion
  - **Discriminator Stage (Comparator)**
    - Voltage to Time conversion

Proposed Channel

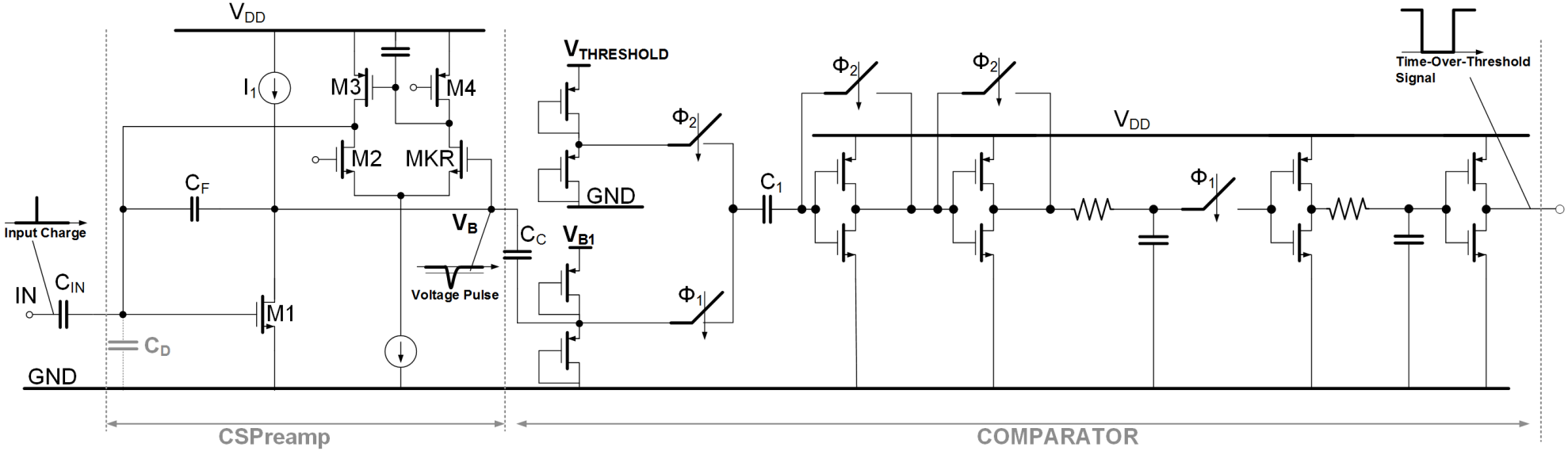
Specifications



Parameter	Value
Maximum Power Consumption	5 µW
Input Charge Range	Up to 30 ke^-
Minimum Detectable Charge	1 ke^- (0.16fC)
Maximum Comparator Delay	25 ns
Noise Level	< 200 e^-
Detector Capacitance - C_D	100 fF

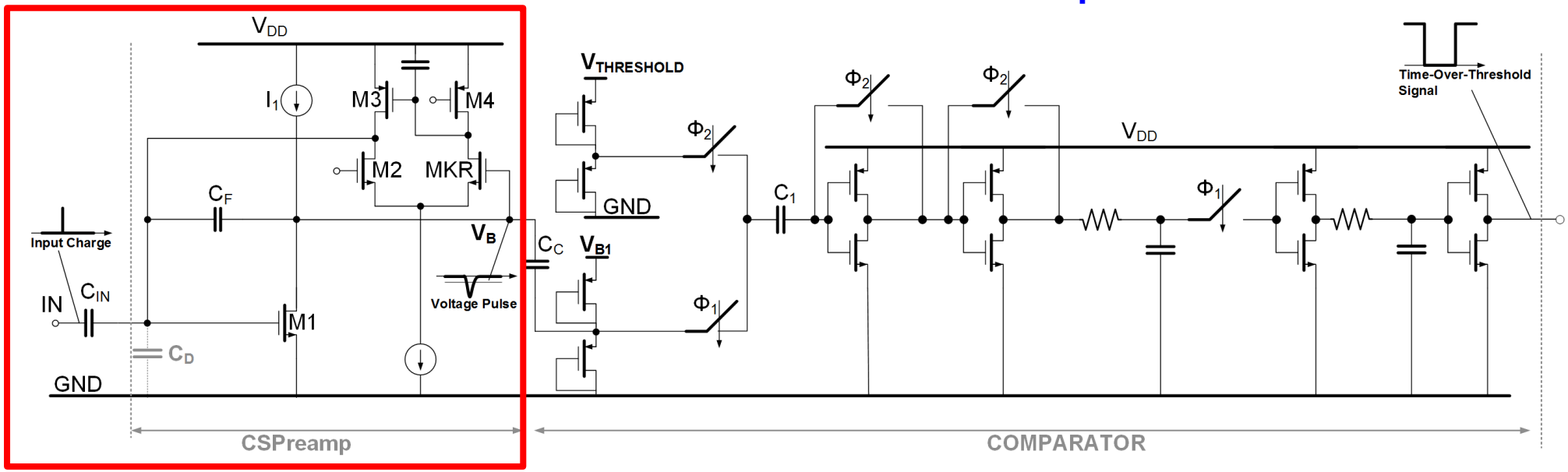
Proposed Channel

Transistor Level Scheme



Proposed Channel

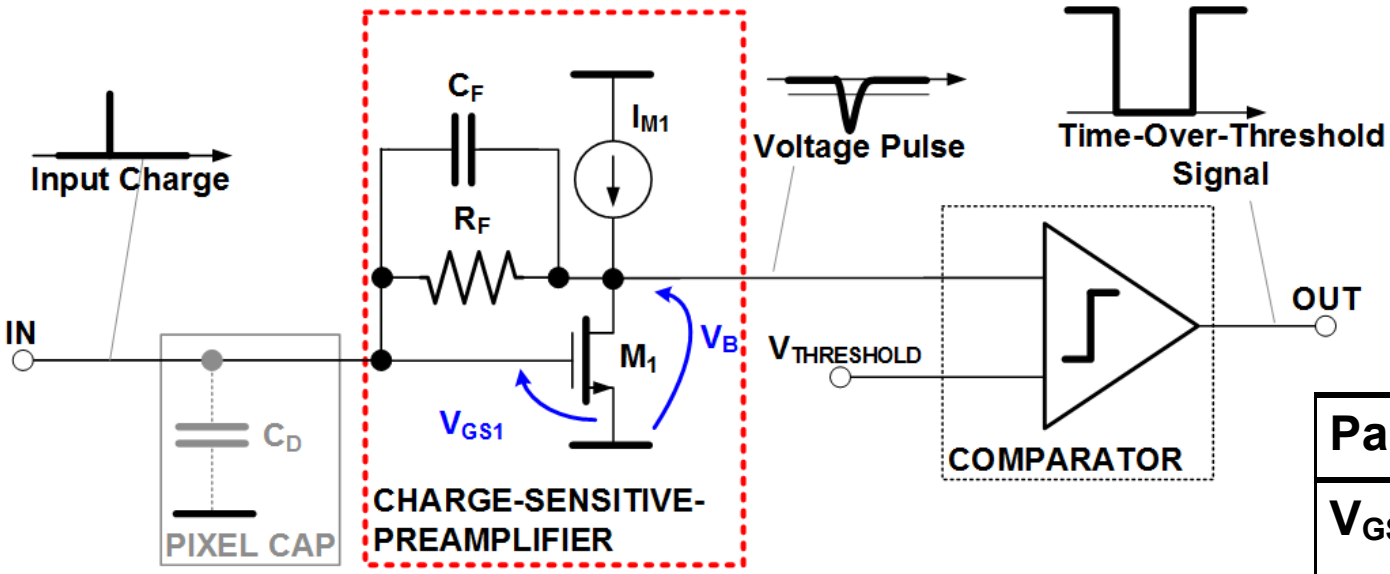
Transistor Level Scheme – CSPreamp 1/2



- Closed-Loop Common Source Stage (M_1):
  - **Capacitor C_F in feedback**
  - **Resistor R_F in feedback**
- Reduced Noise Contributions
- Reduced Current Consumption

Proposed Channel

Transistor Level Scheme – CSPreamp 2/2



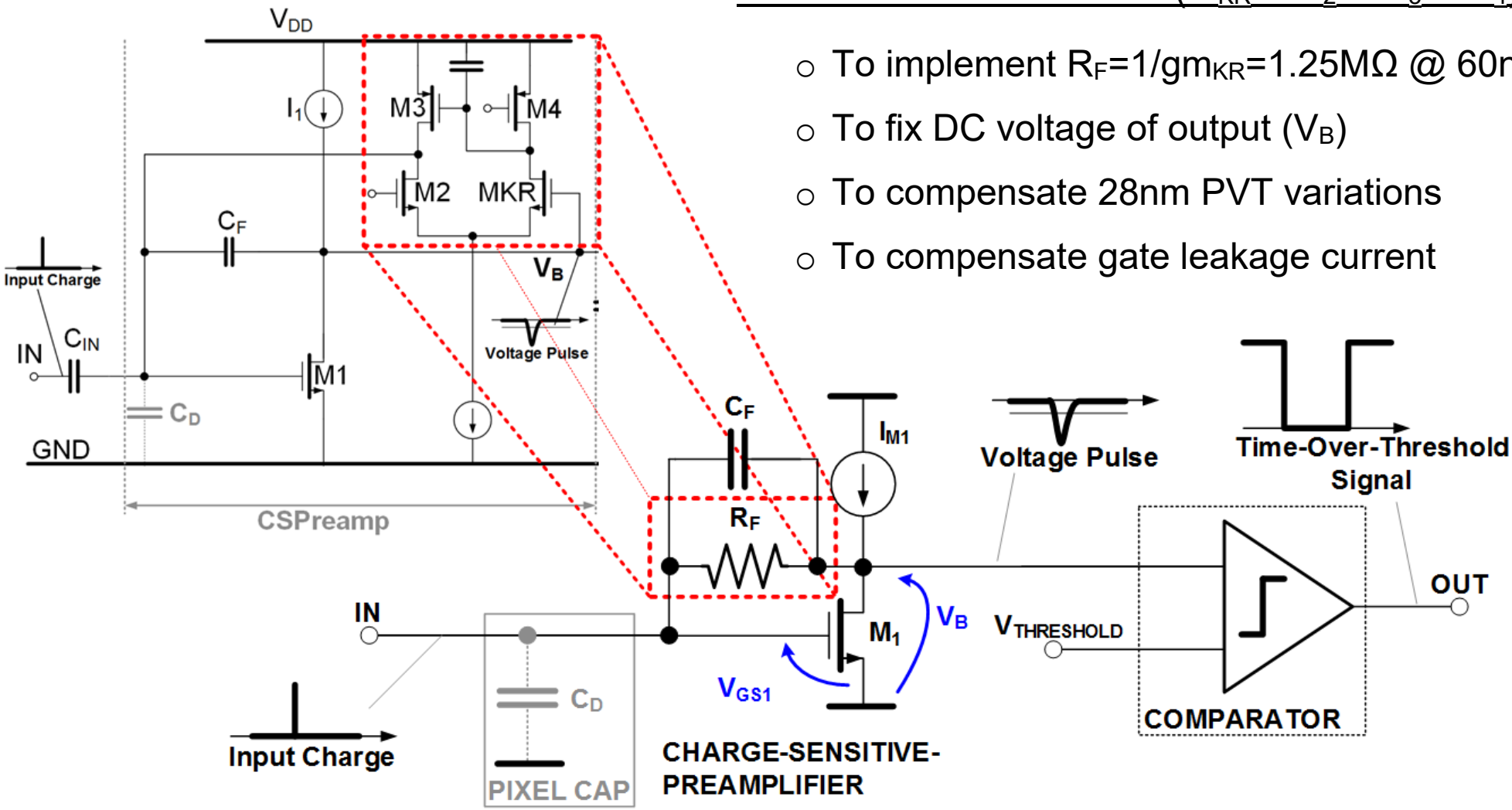
- Transistor M_1 in strong subthreshold:
  - **To maximize g_{m1}**
  - **To minimize thermal noise**

Parameter	Value
V_{GS1}	300mV
V_B	550mV
g_{m1}	51µA/V
I_{M1}	1.7µA
C_D	100fF
C_F	10fF
R_F	1.25MΩ
$(W/L)_{M1}$	12µm/100nm

Proposed Channel

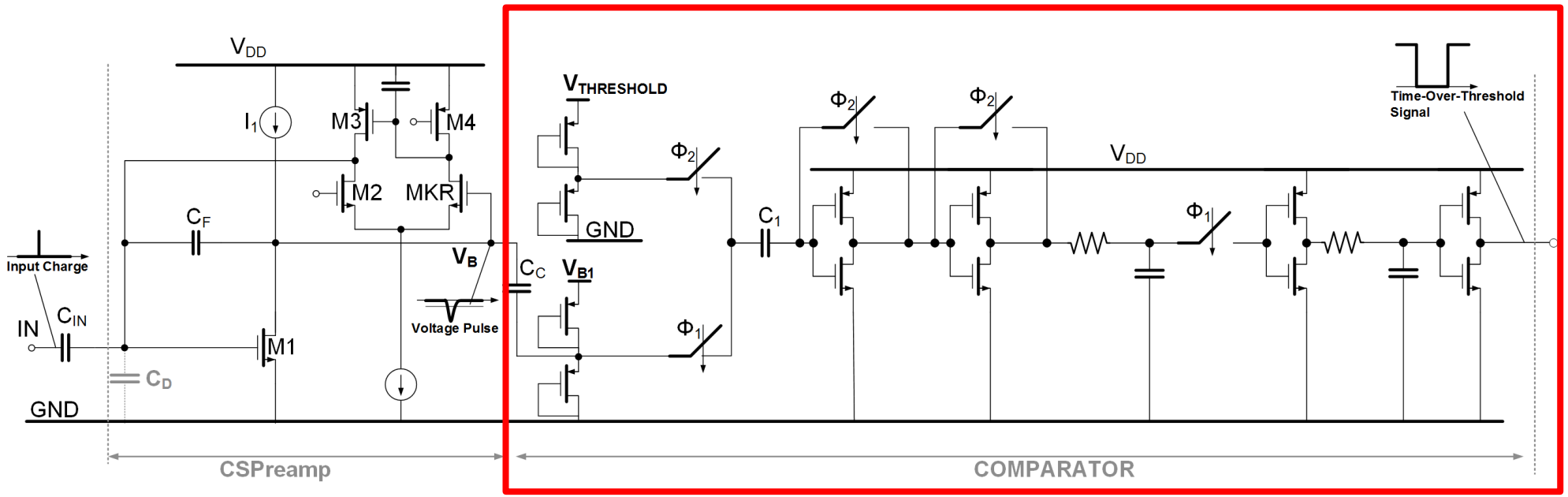
R_F implementation

- Krummenacher Feedback (M_{KR} – M_2 – M_3 – M_4):
  - To implement $R_F=1/gm_{KR}=1.25M\Omega$ @ 60nA
  - To fix DC voltage of output (V_B)
  - To compensate 28nm PVT variations
  - To compensate gate leakage current



Proposed Channel

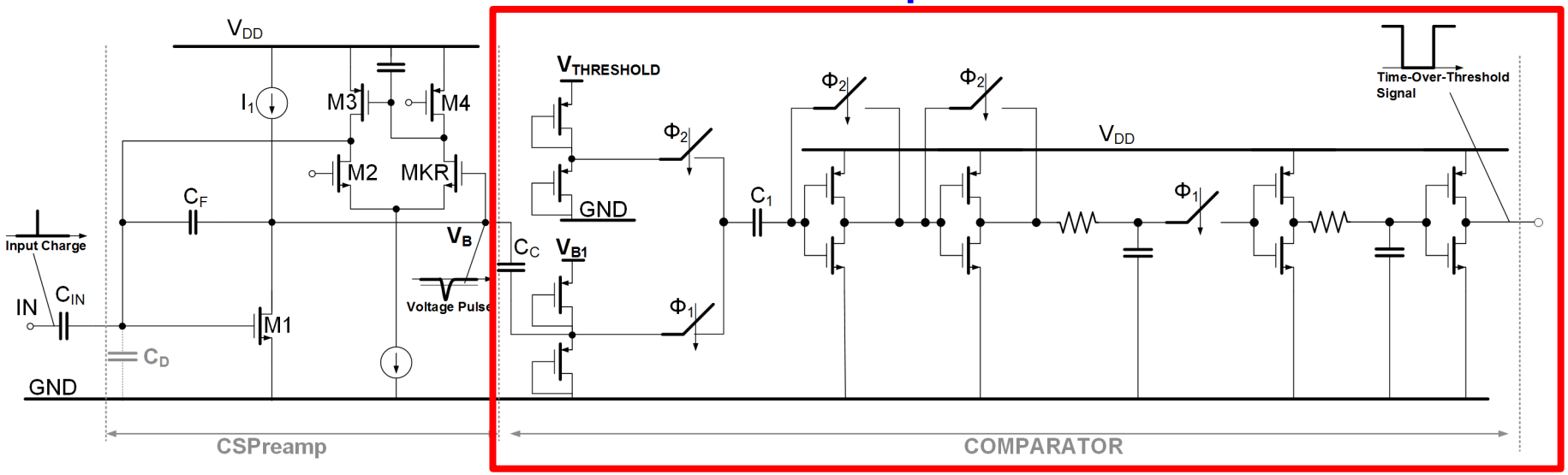
Switched-Inverter-Based Comparator 1/2

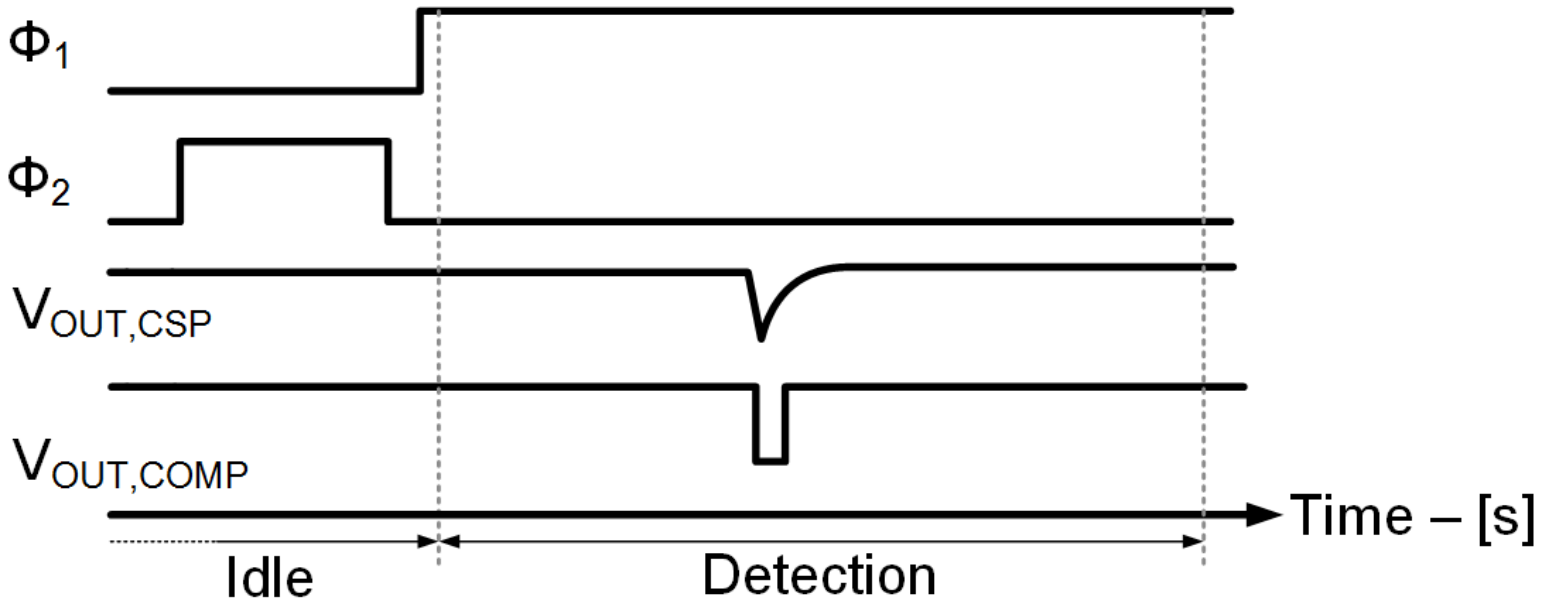


- Decoupling through 1pF - C_C
- Chained of 4 inverters:
  - ***Speed maximization*** @ $0.9V_{DD}$
  - ***Distributed noise-shaping*** function
  - Digital ***Time-over-Threshold (ToT)*** implementation
    - Arrival time and amount of input charges information

Proposed Channel

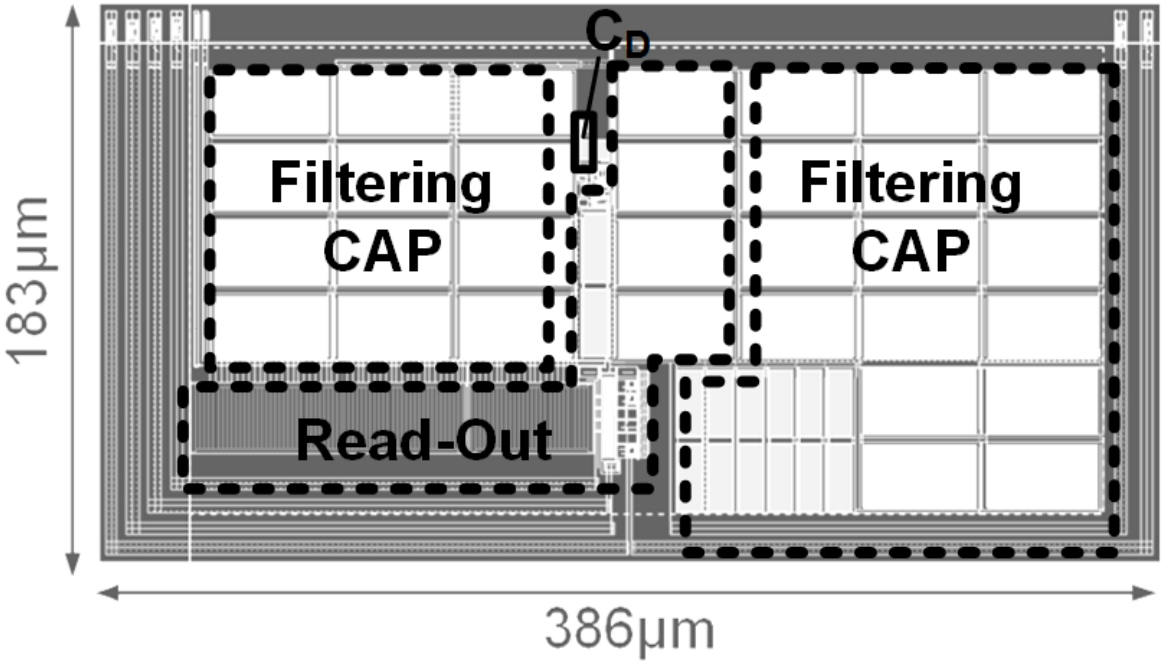
Switched-Inverter-Based Comparator 2/2





Proposed Channel

ICPIX28 Layout



Chip Photo is ***meaningless***

→ due to dummy insertion

Sub-circuit	Description	Area - mm^2
Read-Out	Channel Circuit	**0.02**
Filtering CAP	Filtering capacitance for bias current mirrors	0.04
C_D	On-chip parasitic detector capacitance	0.00052
Total Area	Area of Read-Out +Filtering CAP + C_D +Final Routing	**0.07**

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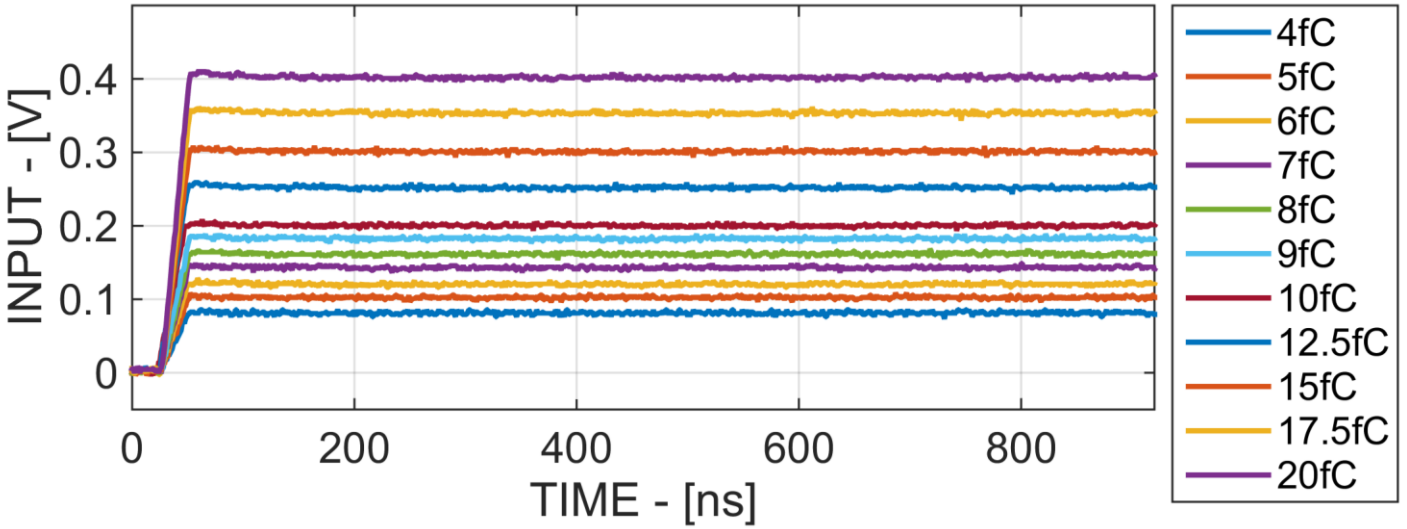
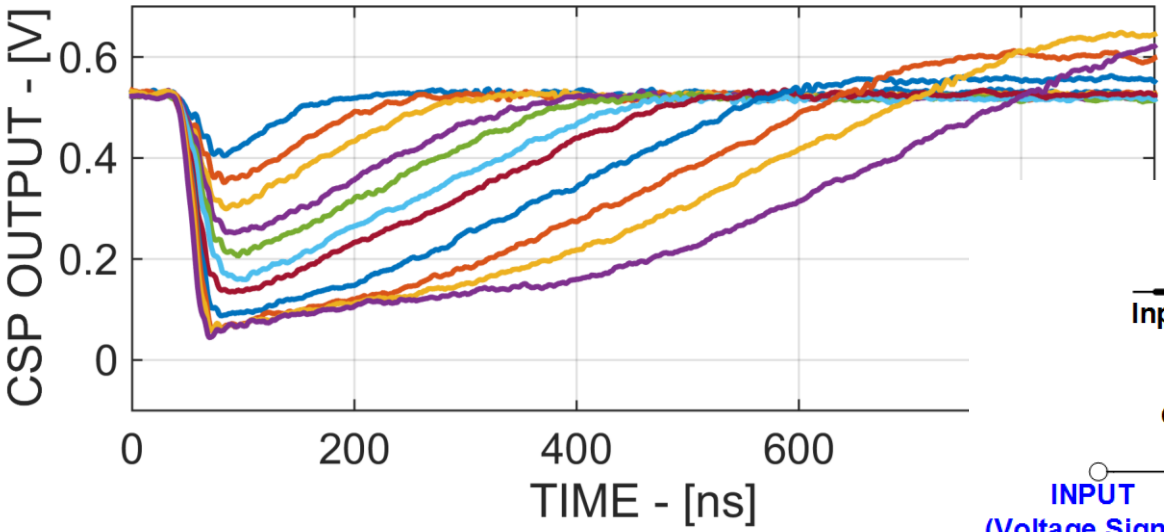
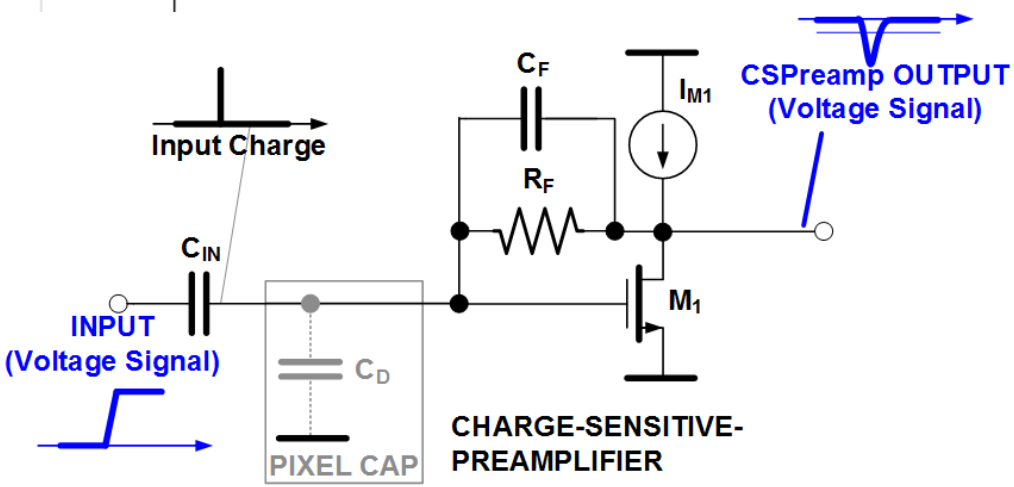
Pre-Radiation Measurements

CSPreamp Output Signal

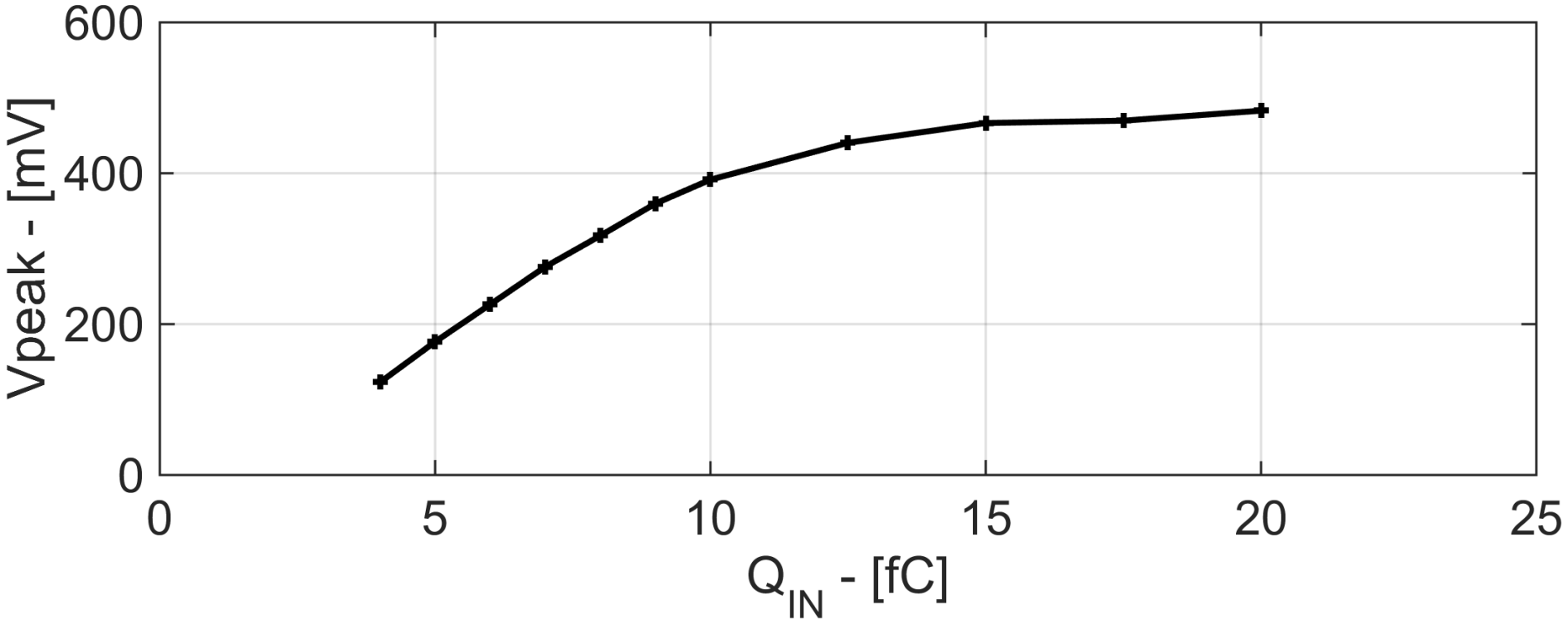






Pre-Radiation Measurements

CSPreamp Peak Voltage

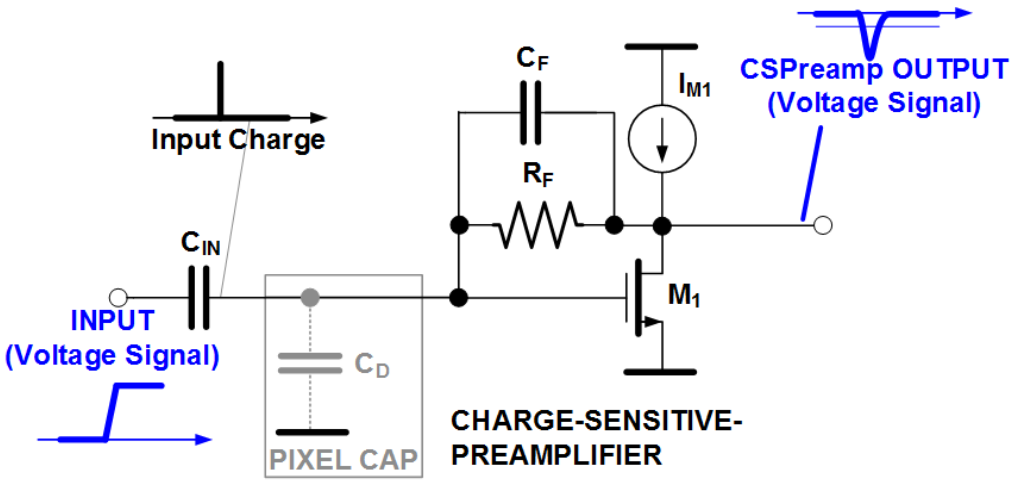


Input charge

→ 4fC – 20fC

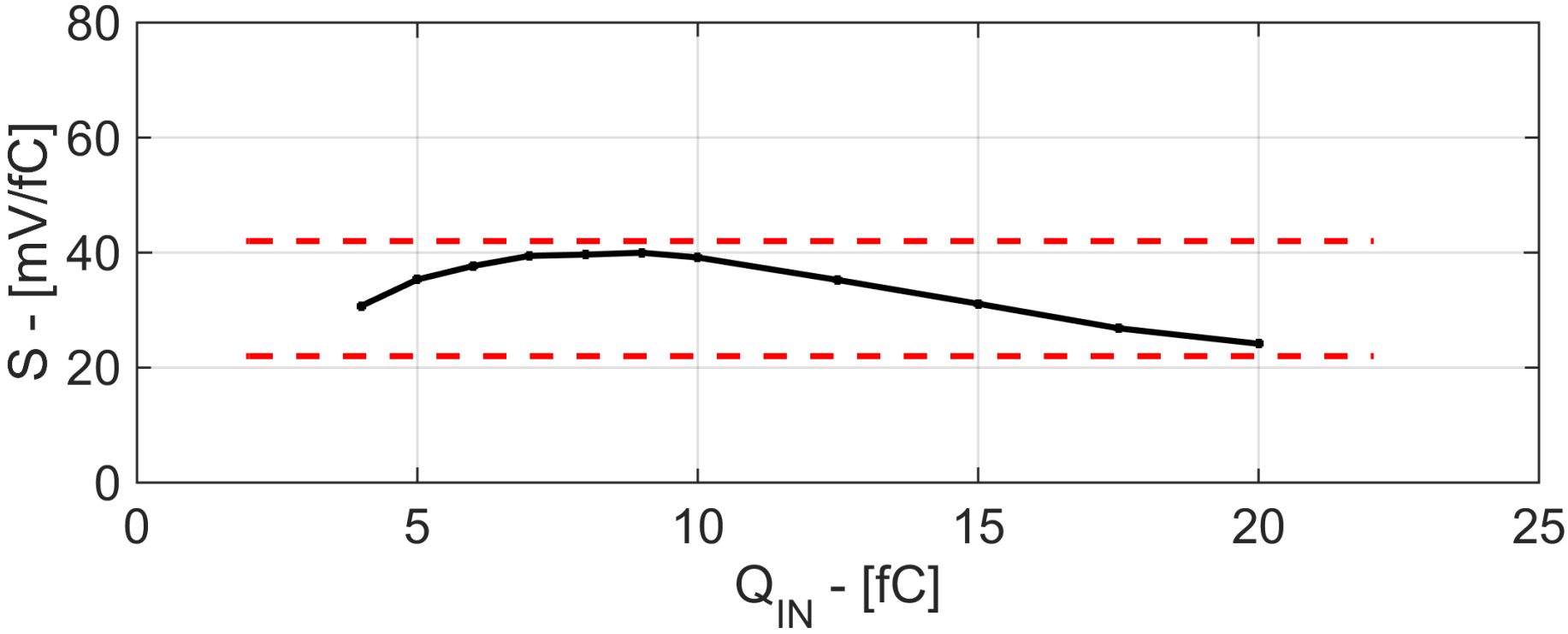
CSPreamp Peak Voltage

→ 122.9mV – 482.9mV



Pre-Radiation Measurements

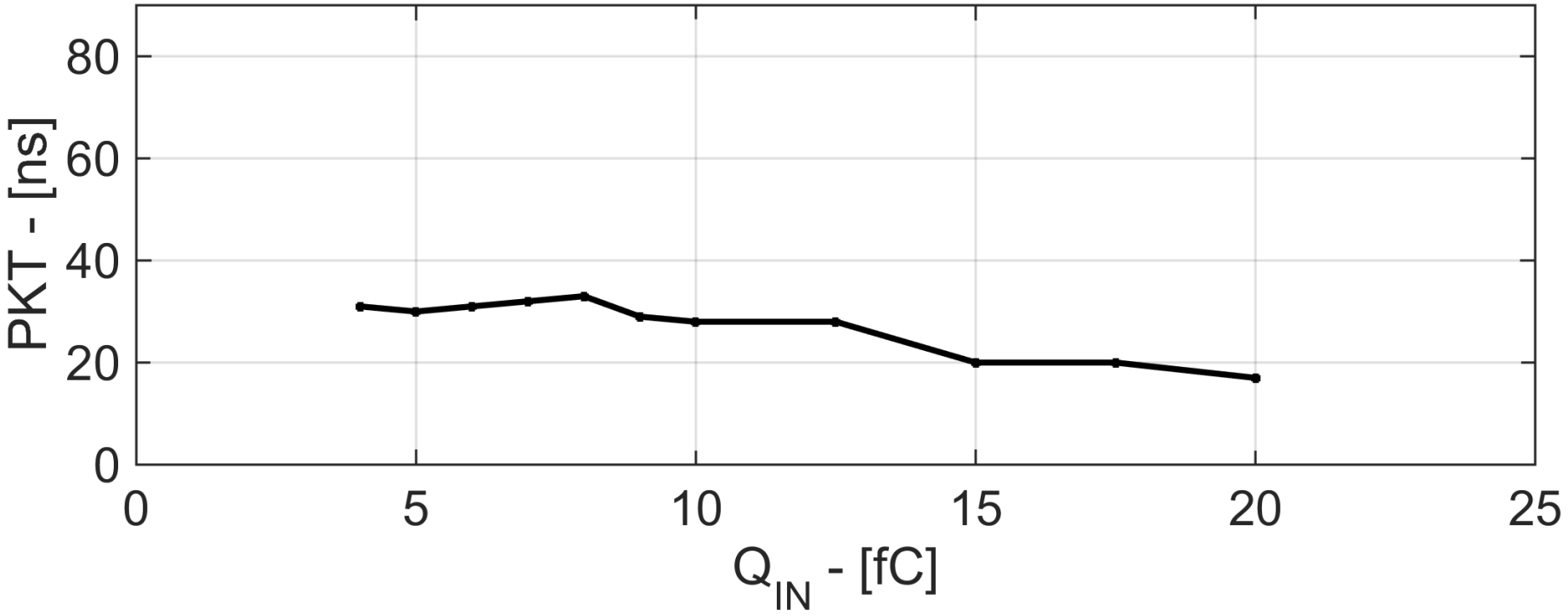
CSPreamp Sensitivity



Parameter	Range Value
Input charge	4fC – 20fC
CSPreamp Peak Voltage	122.9mV – 482.9mV
Sensitivity (average value)	30mV/fC

Pre-Radiation Measurements

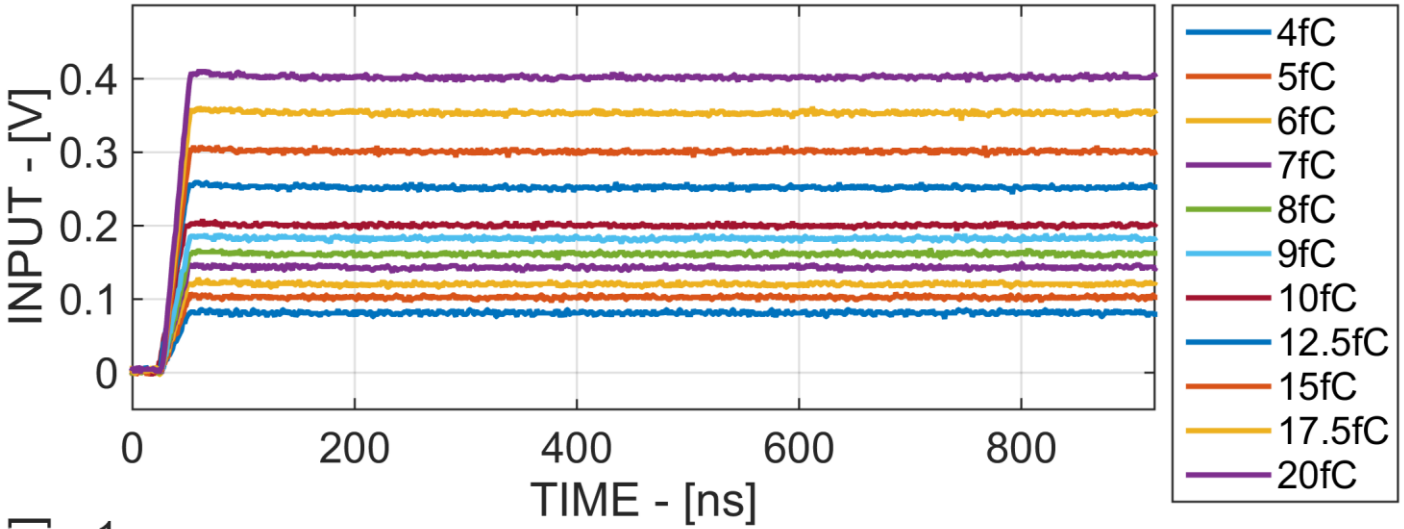
PKT Characteristics

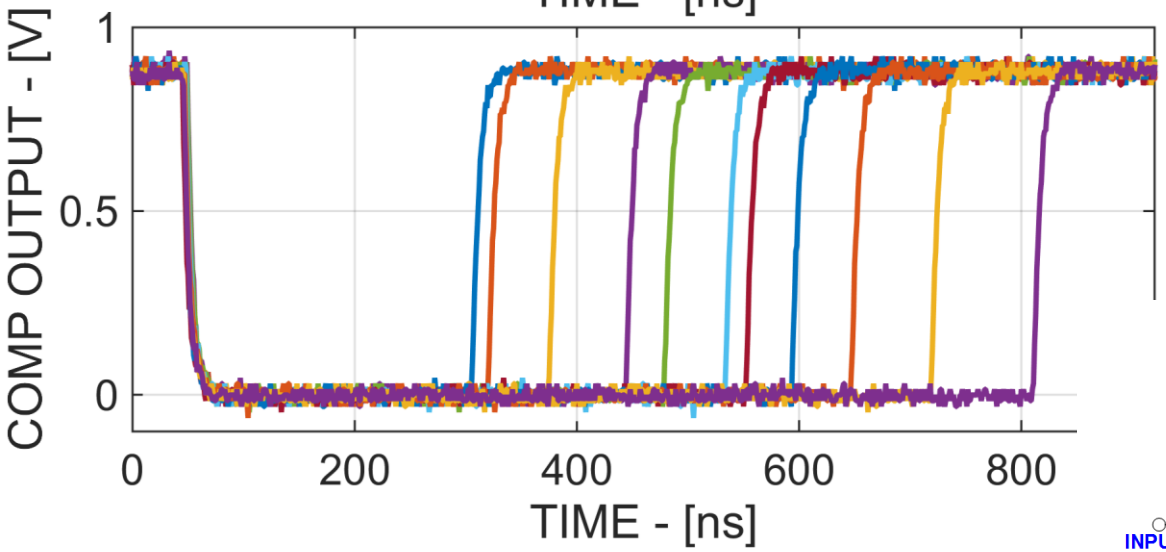


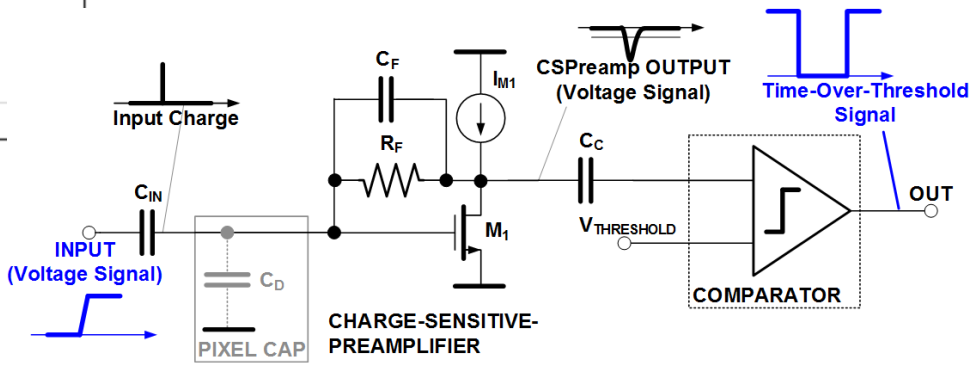
Parameter	Range Value
Input charge	4fC – 20fC
CSPreamp Peak Voltage	122.9mV – 482.9mV
Sensitivity (average value)	30mV/fC
PeaKTime Delay (average value)	30ns

Pre-Radiation Measurements

Comparator Output Signal

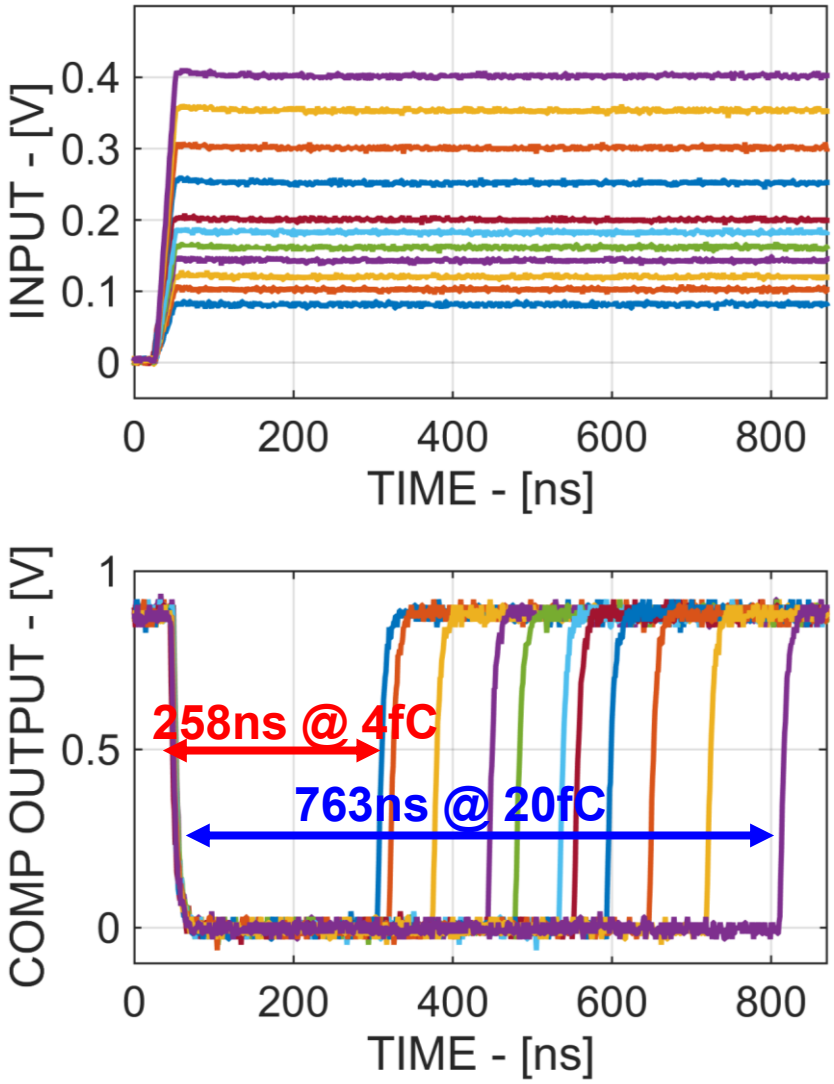


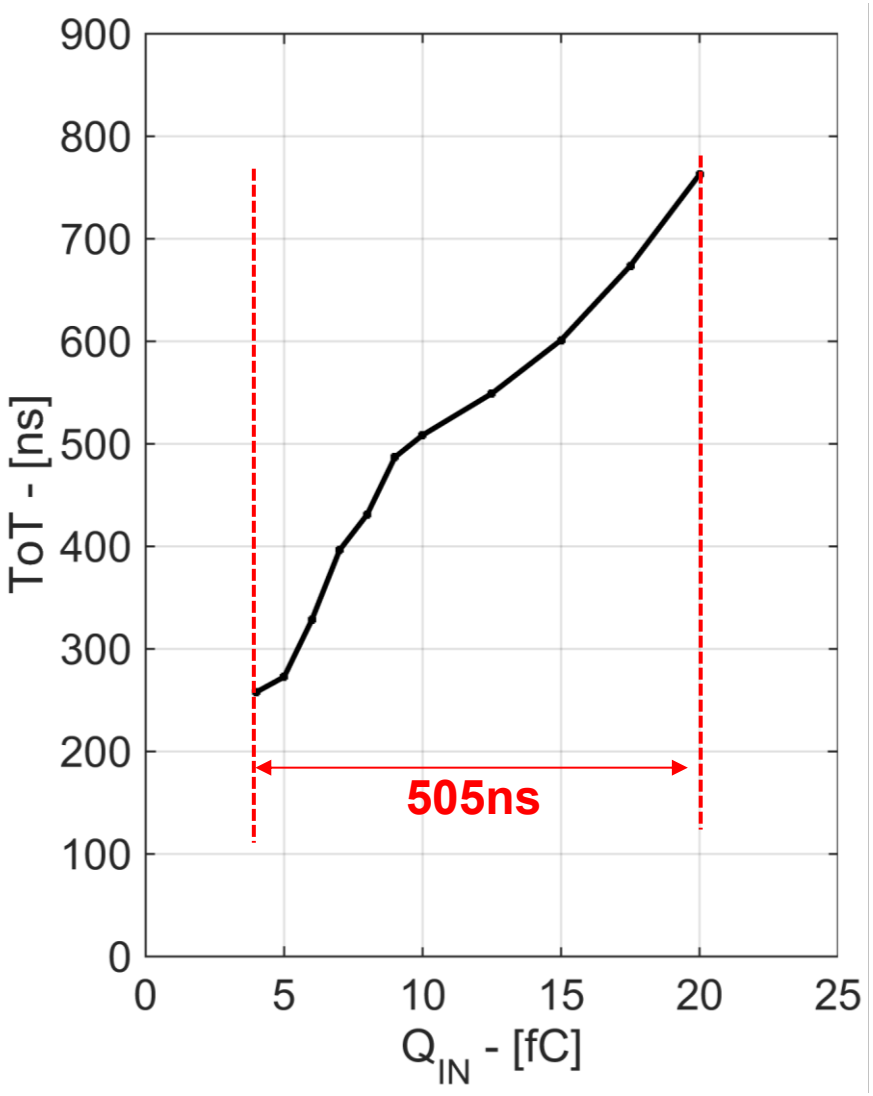




Pre-Radiation Measurements

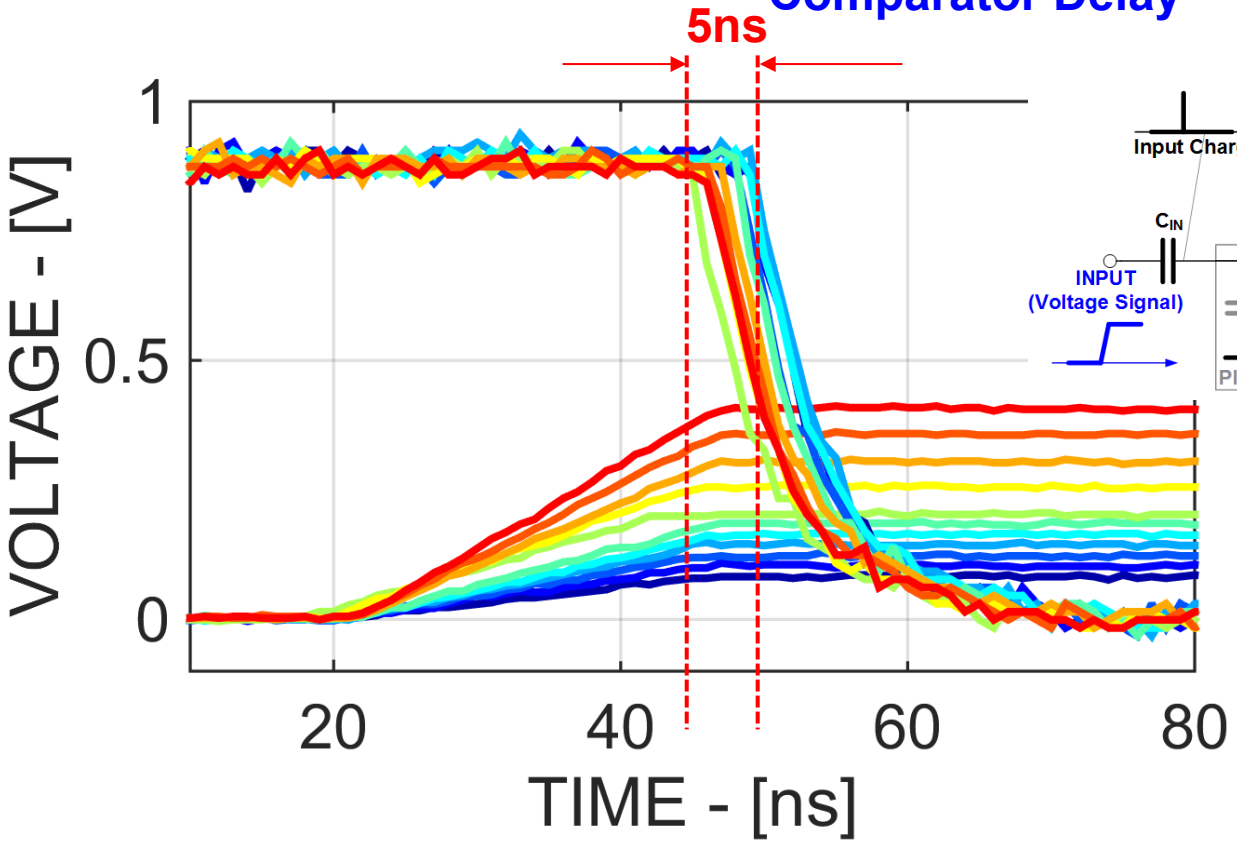
Time-over-Threshold

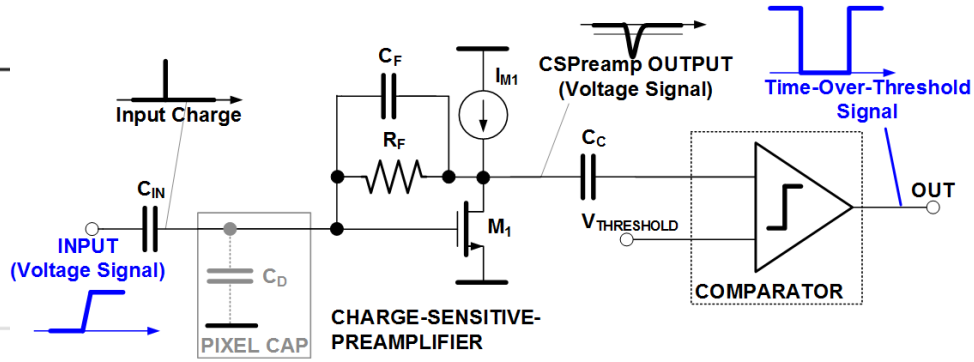




Pre-Radiation Measurements

Comparator Delay





Parameter	Range Value
Input charge	4fC – 20fC
Maximum Comparator Delay	5ns
Time-over-Threshold (ToT)	258ns – 763ns

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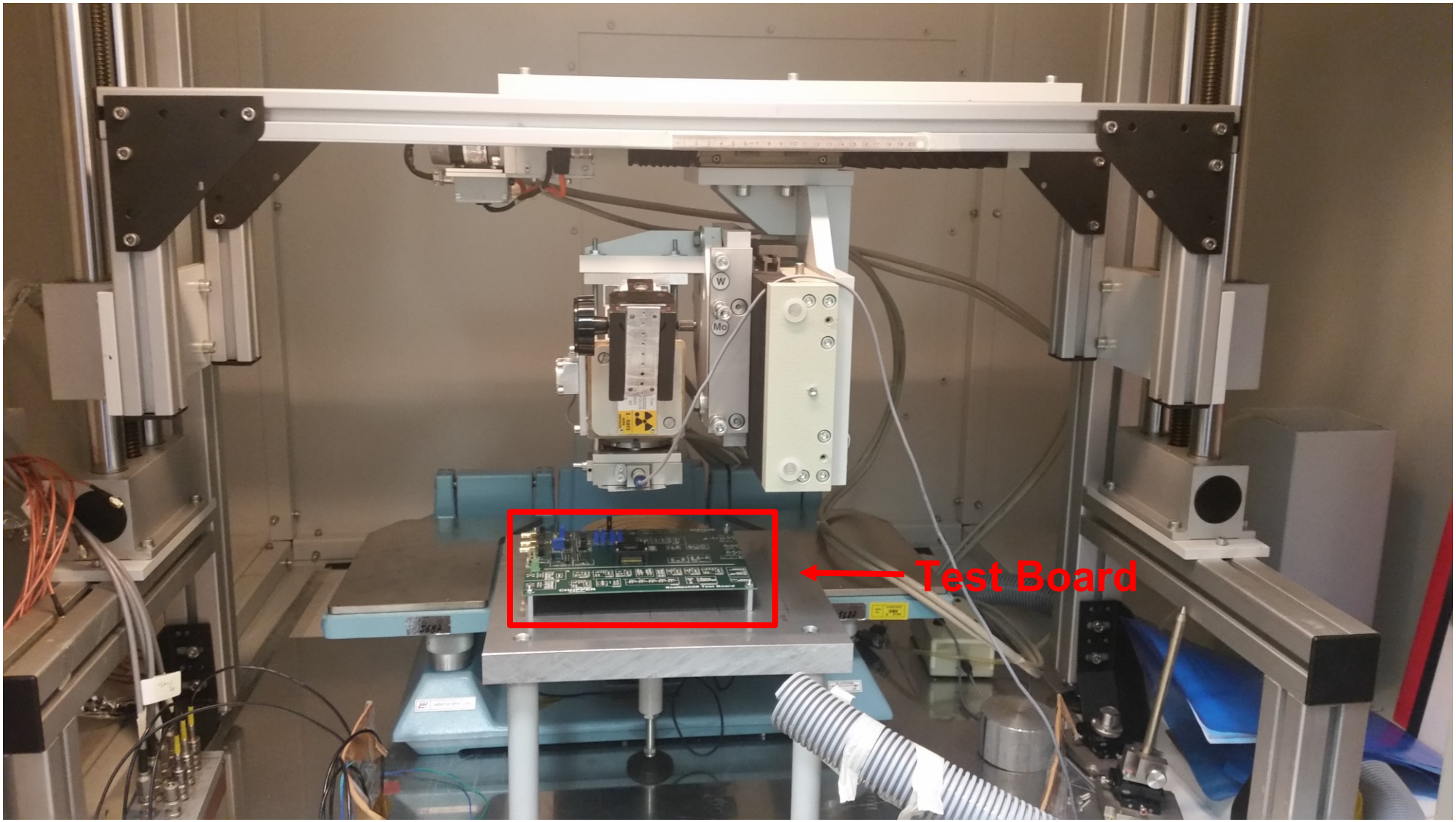
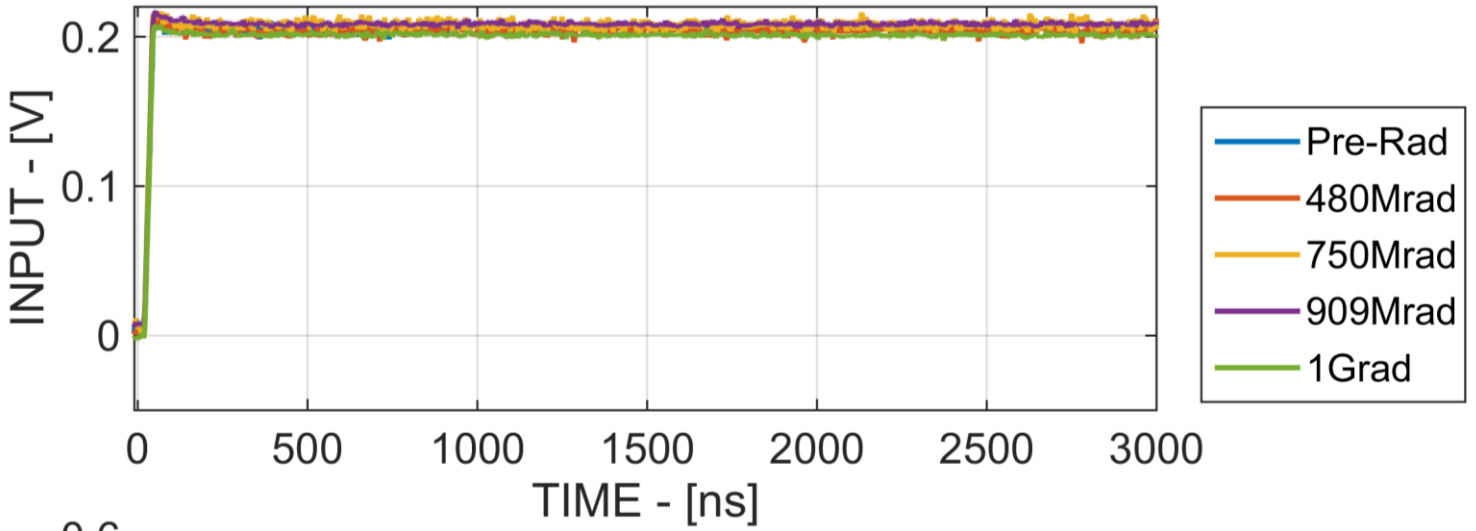
Post-Radiation Measurements

Setup for X-ray Radiation

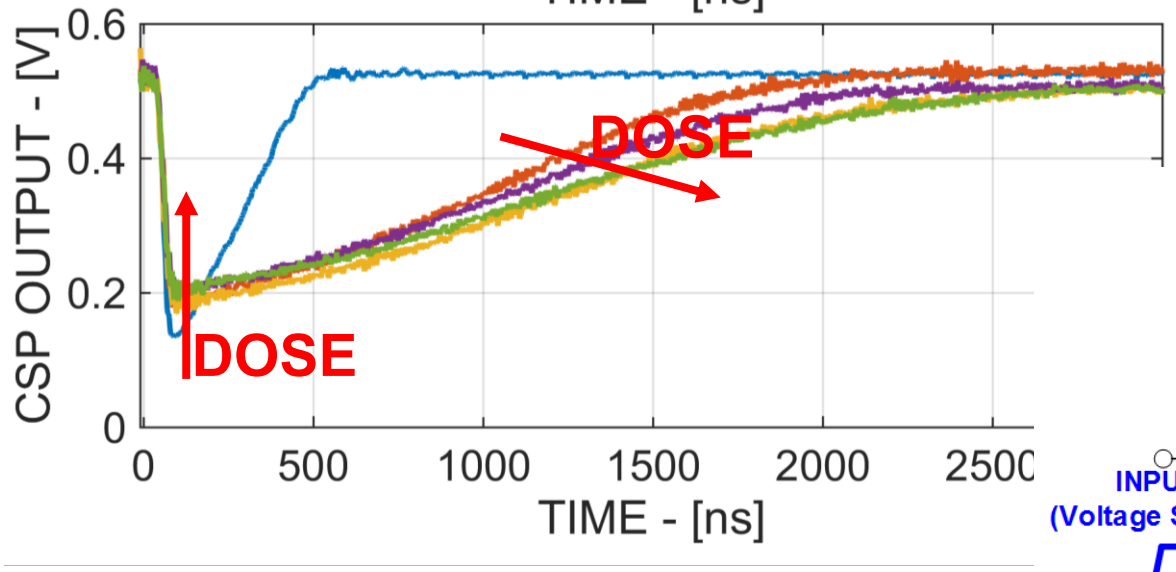


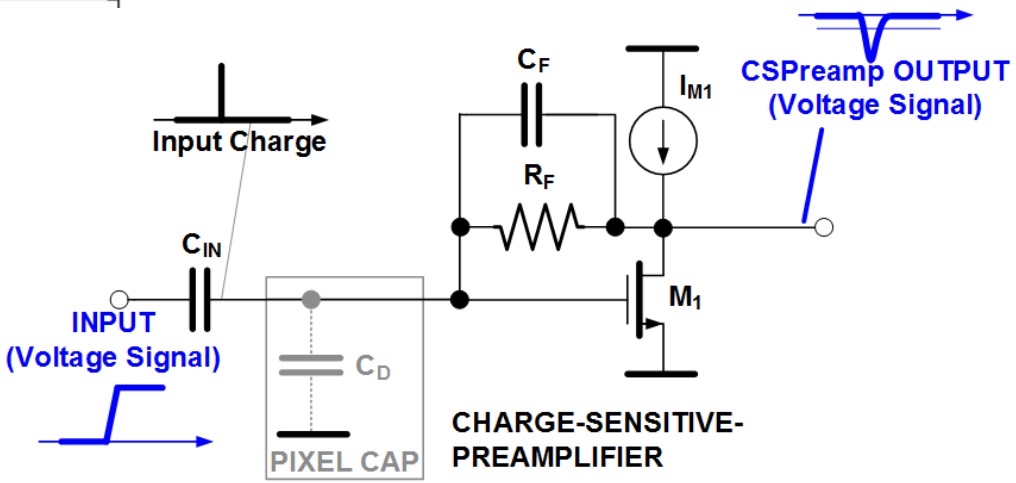
Post-Radiation Measurements

CSPreamp Output Signal @ 10fC Input Charge



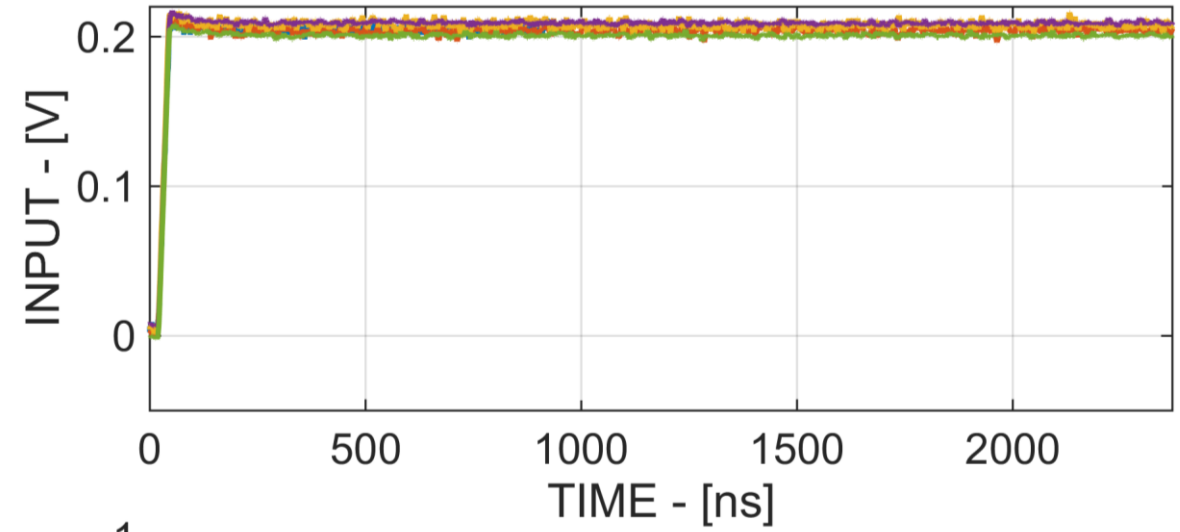
PRELIMINARY RESULTS!

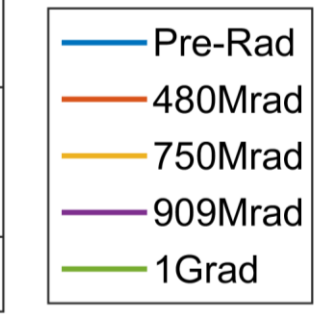




Post-Radiation Measurements

Comparator Output Signal @ 10fC Input Charge





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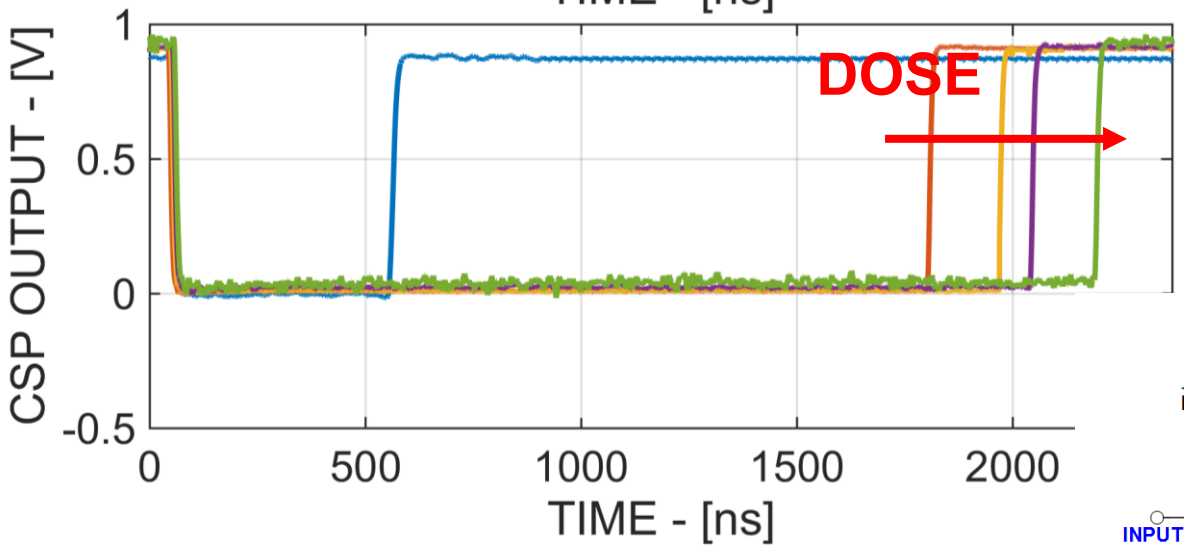

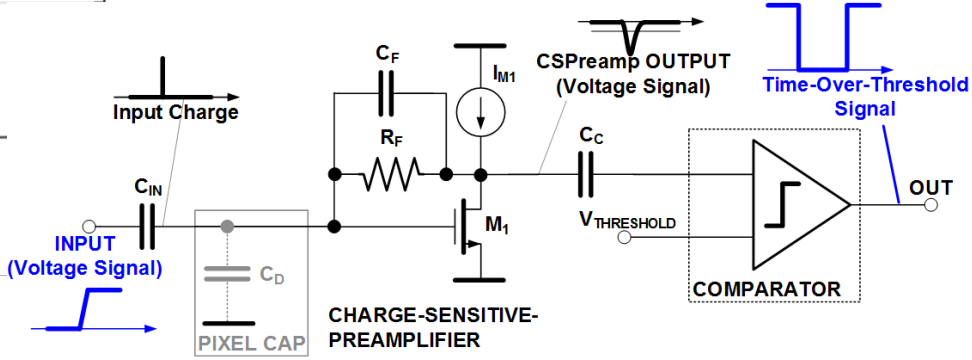

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Pre-Radiation Performance Resume

Parameter	Range Value
Bulk CMOS Technology	28nm
Supply Voltage	0.9V
Power Channel Consumption	4.3µW
Die Size	$0.02mm^2$
Detector Parasitic Capacitance	100fF
Feedback Capacitance	10fF
Feedback Resistor	1.25MΩ
Input charge	4fC – 20fC
CSPreamp Peak Voltage	122.9mV – 482.9mV
Sensitivity (average value)	30mV/fC
PeaKTime Delay (average value)	30ns
Maximum Comparator Delay	5ns
Time-over-Threshold (ToT)	258ns – 763ns

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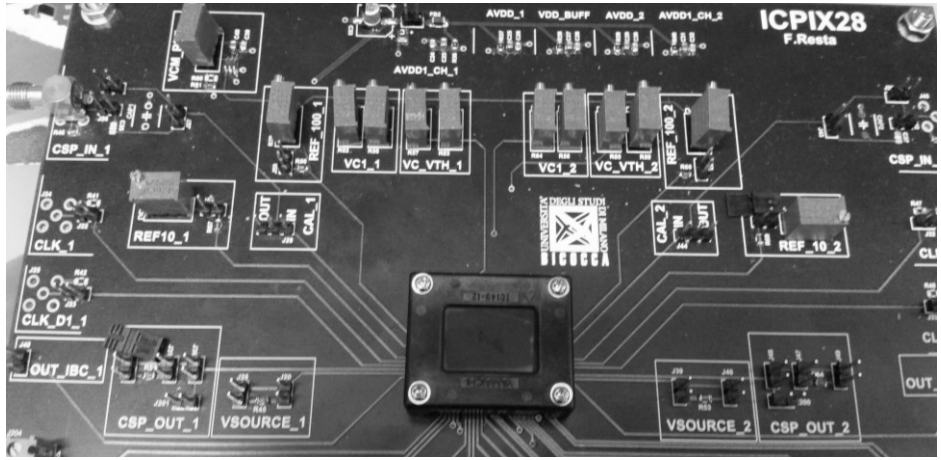
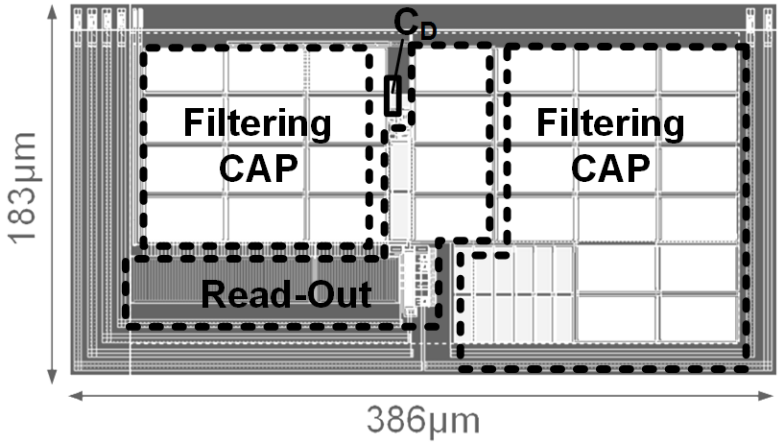
Conclusion

- Single channel in ***28nm bulk CMOS Technology*** has been integrated
- Simple circuit with minimal function
    - To test a new sub-µm technology with and without radiation
- Test under Radiation will be completed in the next weeks
- **Current Consumption** of 4.6 µA → 2.4 µA for CSA + 2.2 µA for Discriminator
- **Supply Voltage** of 0.9 V
- **Area** Occupancy 0.07mm^2
    - Most of it is occupied by filtering capacitance





THANK YOU!

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