Contribution ID: **61** Type: **Oral**

# IC-PIX28: Pixel Detectors Read-Out in Bulk-CMOS 28nm

*Tuesday, 27 September 2016 14:50 (25 minutes)*

ICPIX28 is the first 28nm bulk-CMOS readout frontend for High Energy Physics pixel detectors. It performs the conversion of the input charge into a voltage signal, hence detect the charge arrival time and amount of charge information through Time-over-Threshold signal. The front-end is composed by the cascade of a Charge Sensitive Preamplifier and a low-power switched-capacitor logic-inverter-based comparator. A single channel area occupancy is 0.07mm2. It operates at0.9V supply voltage and consumes 4.3µW at 46dB@SNR. 10mV/fC sensitivity at 0.05fC Equivalent Noise Charge demonstrates design efficiency.

## Summary

The necessity to improve the Large Hadron Collider performance is the basis of High Luminosity Large Hadron Collider (HL-LHC) project at the CERN. The main goal is to rise the number of proton-proton collisions that occur in a given amount of time through a 10 times higher luminosity. Increasing the potential data rate, the researchers can detect more rare processes and discover new particles after 2025. The upgrade requires challenging changes in the High Energy Physics experiments and in the electronic readout front-end. Advanced scaled-down electronic with nmetric CMOS technologies development, i.e. bulk CMOS 28nm, is possible and includes Silicon Pixel Detectors (SPDs). SPDs play a key role in both ATLAS and CMS experiments and a careful design is necessary. Typical requirements for this circuit topology are radiation hardness (up to 1Grad), miniaturization (to increase spatial resolution), fast time response (within 20ns), low power consumption (due to huge number of the pixels) and very low Equivalent Noise Charge (ENC).
In this scenario, the first read-out front-end for pixels detectors (with 100fF parasitic capacitance) in 28nm bulk-CMOS technology has been developed. Technology choice is imposed by higher radiation hardness and forces analog designers to manage 0.9V supply voltage operation at higher standard process MOS transistors threshold voltage (about 0.5V in nominal conditions), leading to difficult operating point stability. Moreover, large SNR is challenging, since at lower supply voltage, the dynamic range also decreases.
The proposed pixel detector front-end is composed by a Charge Sensitive Preamplifier (CSPreamp, a common source topology with Krummenacher feedback), and a Comparator. Krummenacher feedback fixes the operating point at the input and the output of the CSPreamp helping to automatically compensate the detector leakage current. The Comparator based on switched-capacitor logic-inverter topology allows to save power and provides arrival time and amount of charge information.
The IC-PIX28 has been extensively tested in time domain, in terms of operating point and time response vs. input charge. With a detector capacitance of 100fF and an input charge in the range 5fC–14fC, the voltage peak at CSPreamp output linearly grows from 14 mV to 109mV. IC-PIX28 performs 10mV/fC of sensitivity and 46dB of SNR with 0.05fC of ENC. It is enable to manage the signal with almost constant time delay around 17ns and 180ns Time-over-Threshold range. Most advanced 28nm Time-To-Digital Converters (TDC) use about 50ps as minimum time resolution, while old TDCs, actually mounted at CERN have about 10 times higher minimum time resolution (i.e. 500ps). Hence, feeding the IC-PIX28 with the TDC, the equivalent conversion bits ranges from 8.5bits (old TDCs) up to 12bits (advanced 28nm TDC), demonstrating this way the high charge quantization resolution achievable with this front-end. With 0.9V of supply voltage and 0.5V transistor threshold voltage, the power consumption of the overall chain is 4.2µW. The measurements demonstrate the high performance charge sensing for pixel detectors.

**Primary author:** RESTA, Federica (University and INFN Milano Bicocca)

**Co-authors:** PIPINO, Alessandra (University and INFN Milano Bicocca); PEZZOTTA, Alessandro (University of Milano-Bicocca); BASCHIROTTO, Andrea (University and INFN Milano Bicocca); DE MATTEIS, Marcello (University and INFN Milano Bicocca)

**Presenter:** RESTA, Federica (University and INFN Milano Bicocca)

**Session Classification:** ASIC

**Track Classification:** ASIC