HARDROC3, a 3rd generation ASIC with zero suppress for ILC Semi Digital Hadronic Calorimeter

26-30 September 2016 - TWEPP 2016

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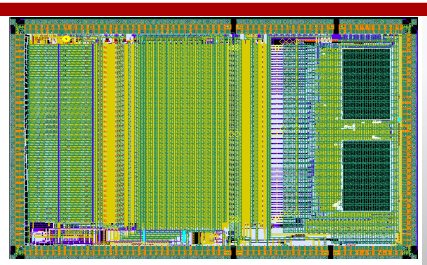
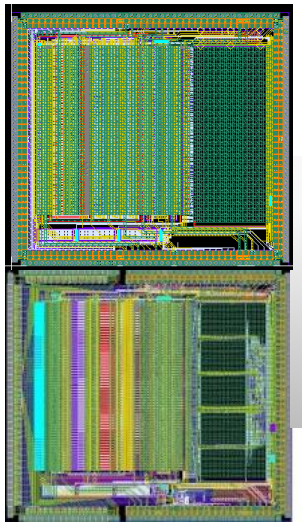
Organization for Micro-Electronics desiGn and Applications

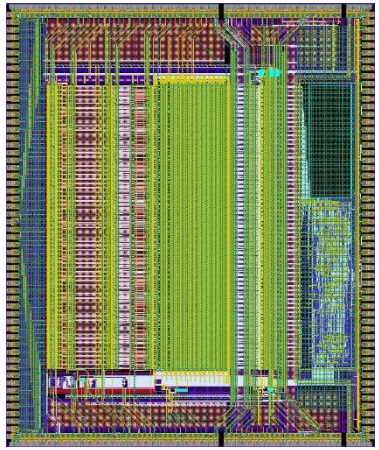
ROC chips for ILC prototypes



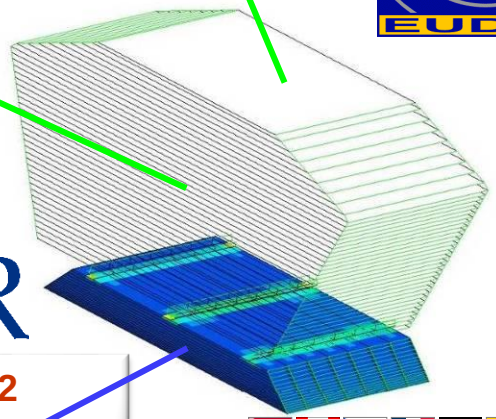
SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
Jun07, Jun08, Mar10, Sept11
Feb15, Feb 16



HARDROC2 and MICROROC
Semi Digital HCAL (sDHCAL)
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept06, Jun08, Mar10, Feb14, Feb15



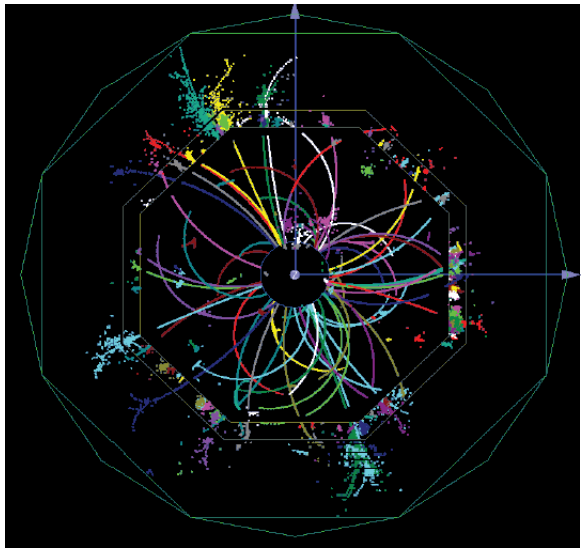
SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
Mar10, Feb16



ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (Eudet/Aida funded)

Requirements for electronics

- Large dynamic range (15 bits)
- Auto-trigger on ½ MIP
- On chip zero suppress
- **10^8 channels**
- Front-end embedded in detector
- **Ultra-low power : 25µW/ch**



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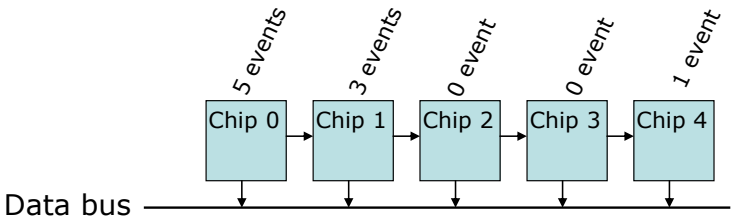
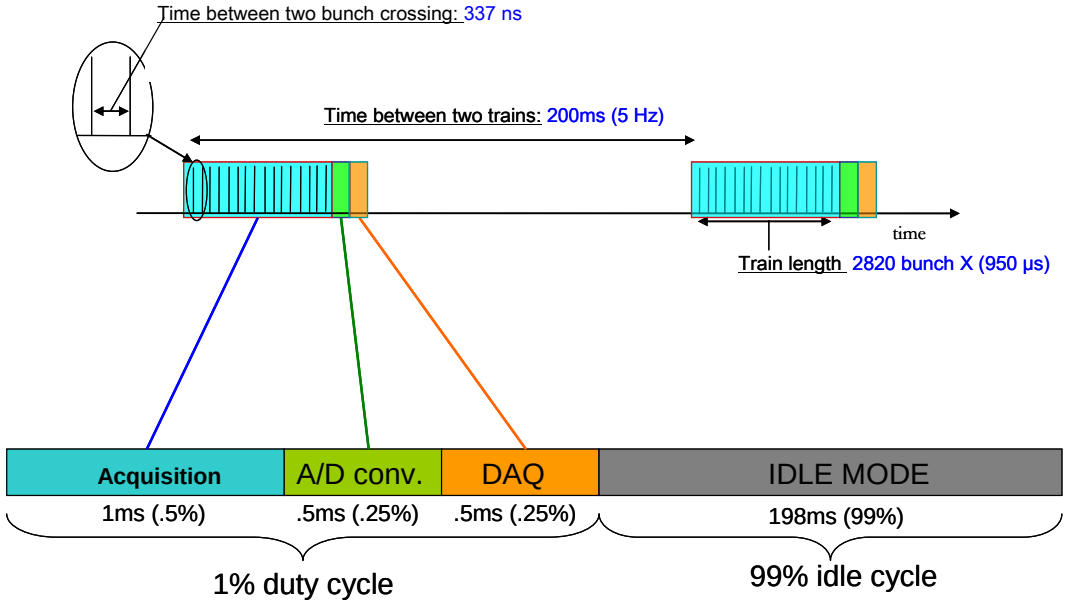
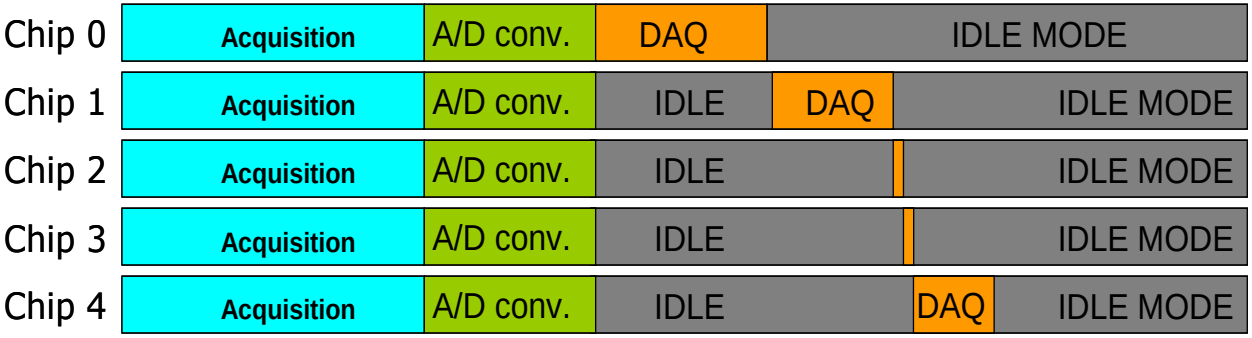
From 2nd generation…

- **2nd generation chips for ILD**
  - Auto-trigger, analog storage and/or digitization
  - Token-ring readout (one data line activated by each chip sequentially)
  - Common DAQ
  - Power pulsing : <1 % duty cycle

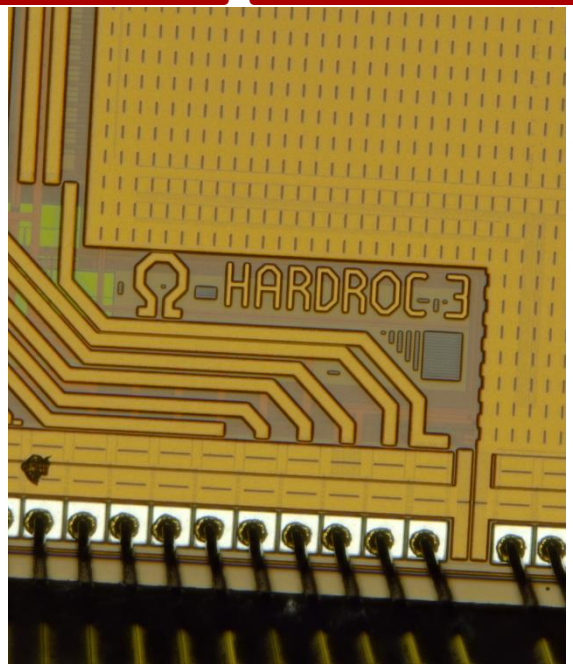




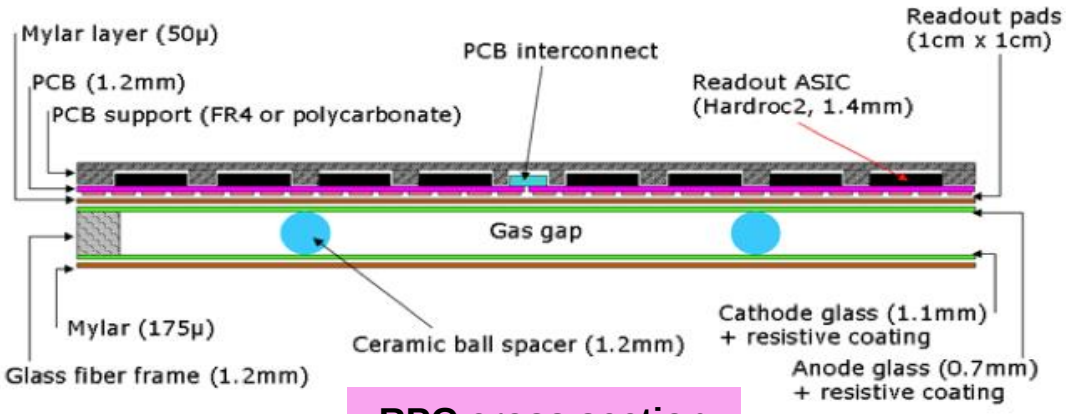


…To 3rd generation

- 3rd generation chips for ILD
  - Independent channels (zero suppress)
  - I2C link (@IPNL) for Slow Control parameters and triple voting
    - configuration broadcasting
    - geographical addressing



- HARDROC3: 1st of the 3rd generation chip to be submitted
  - Received in June 2013 (SiGe 0.35µm) (AIDA funded)
  - Die size ~30 mm² (6.3 x 4.7 mm²) - Packaged in a QFP208



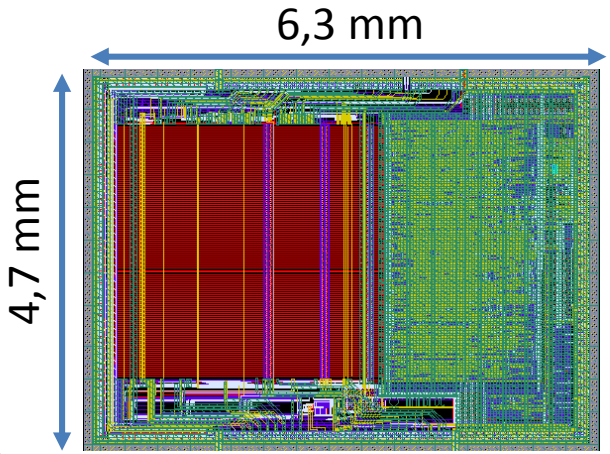
RPC cross section

1m² RPC [IPNL]

HARDROC3 : overview

HR3 main features:

- Independent 64 channels
- Zero suppress
- Extended dynamic range (up to 50 pC)
- I2C link with triple voting for slow control parameters
- Token ring ReadOut
- PLL
- All bias and reference voltage internal (w. power pulsing)
  - No decoupling capacitances required on bias and references voltages

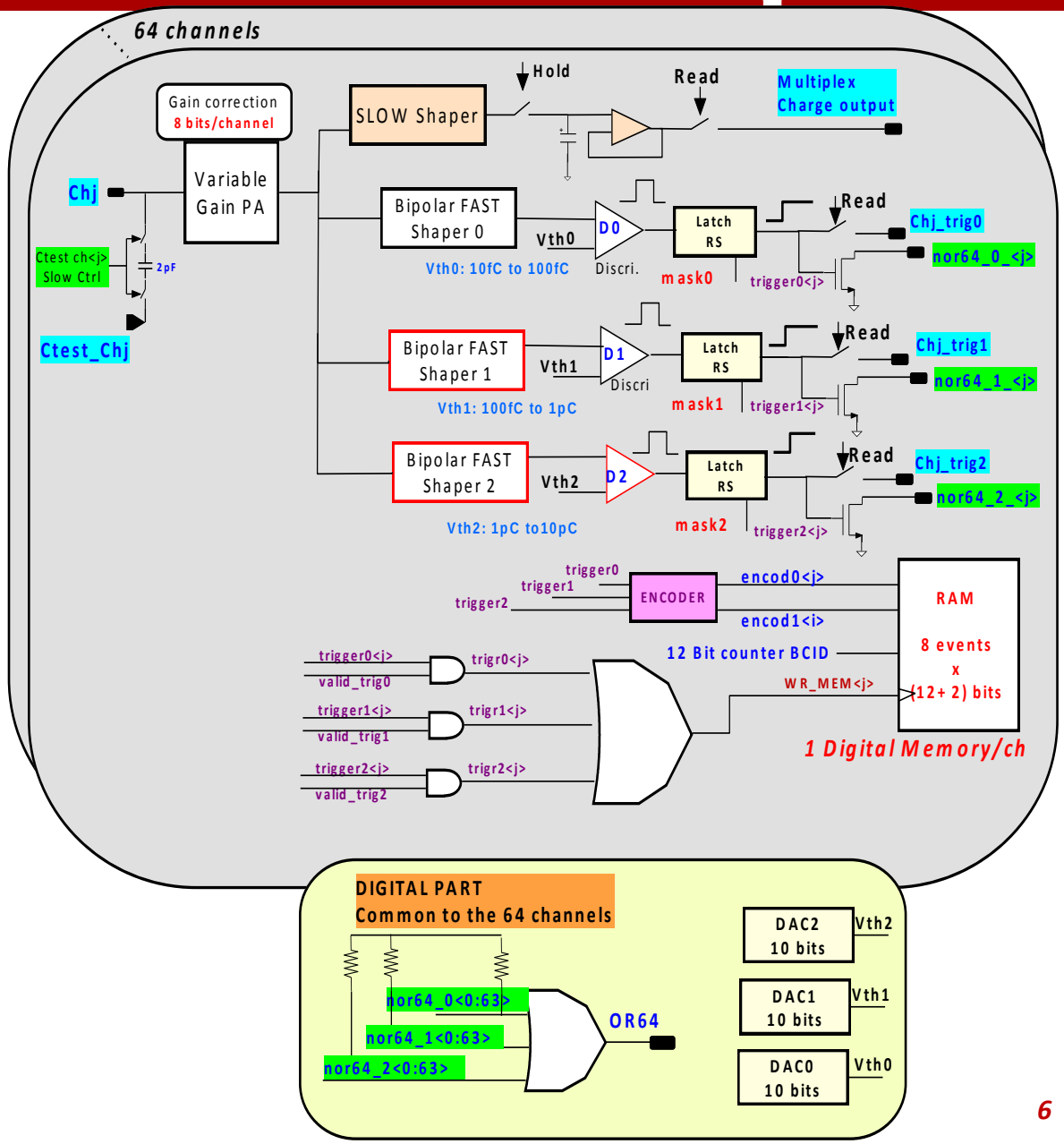


HARDROC3:

- Production run submitted February 2015 (AMS SiGe 0.35µm)
- Naked dies received mid-2015
- Chip packaged in a plastic QFP208
- Die size ~30 mm^2
- Around 800 chips were produced

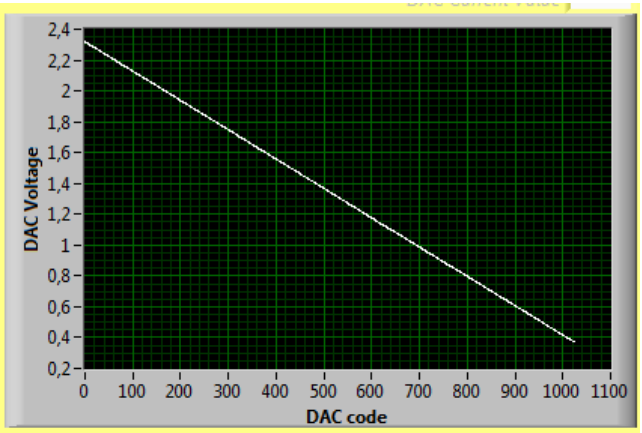
HR3: Simplified schematics

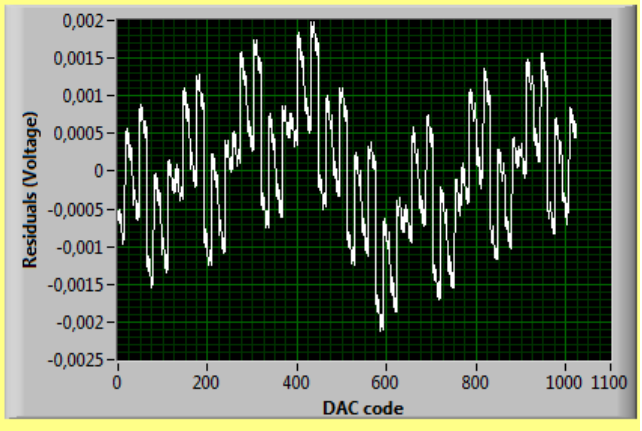
- 64 channels with current preamplifiers
- Trigger less mode (auto trigger 15fC up to 30pC)
- Gain correction (max factor 2)
- 3 shapers + 3 discriminators (encoded in 2 bits for readout)
- I2C link for Slow Control
- Independent channels with zero suppress
- Max 8 events / channel with 12-b time stamping
- Integrated clock generator: PLL
- Power pulsing mode

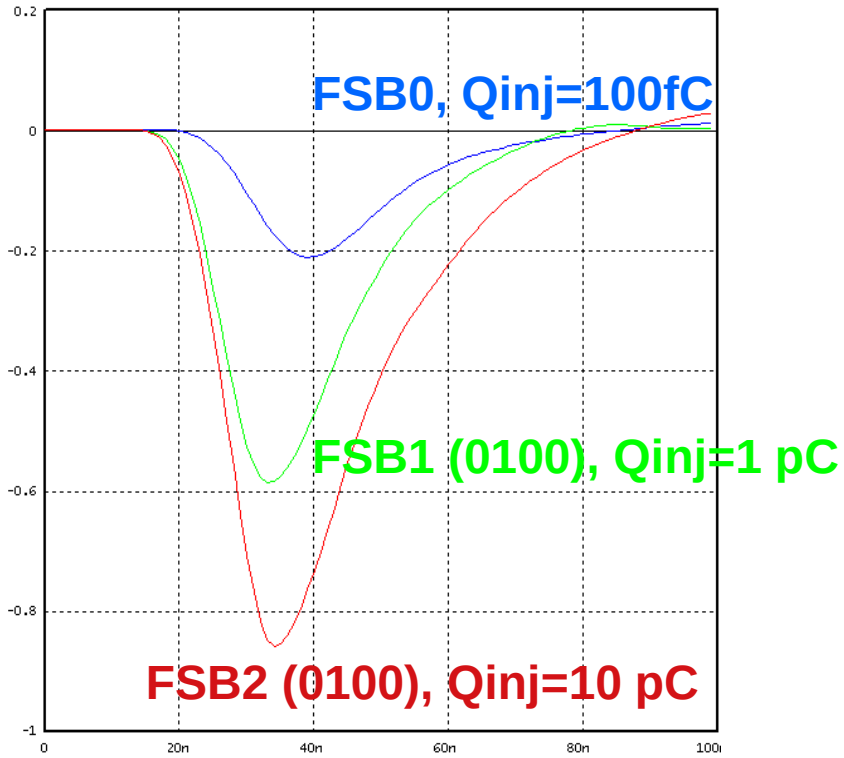


Trigger path : fast shaper and DAC

- Charge injected in one channel: 100fC
  - **Fsb0: Typically 2mV/fC** (variable by a factor 10)
- Scurves performed by varying the DAC value (Threshold)
  - 3 integrated DACs to deliver threshold voltages
  - Residuals within ±5 mV / 2.2V dynamic range. INL= 0.2% (2LSB)
  - **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**



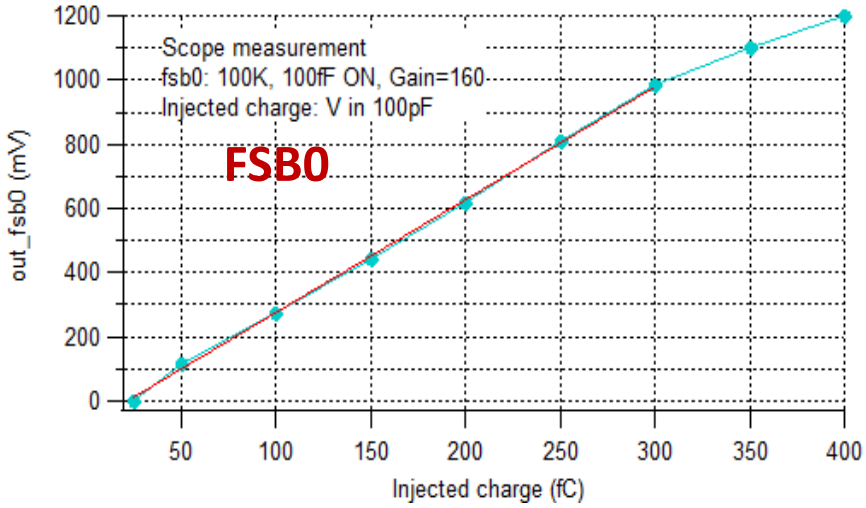


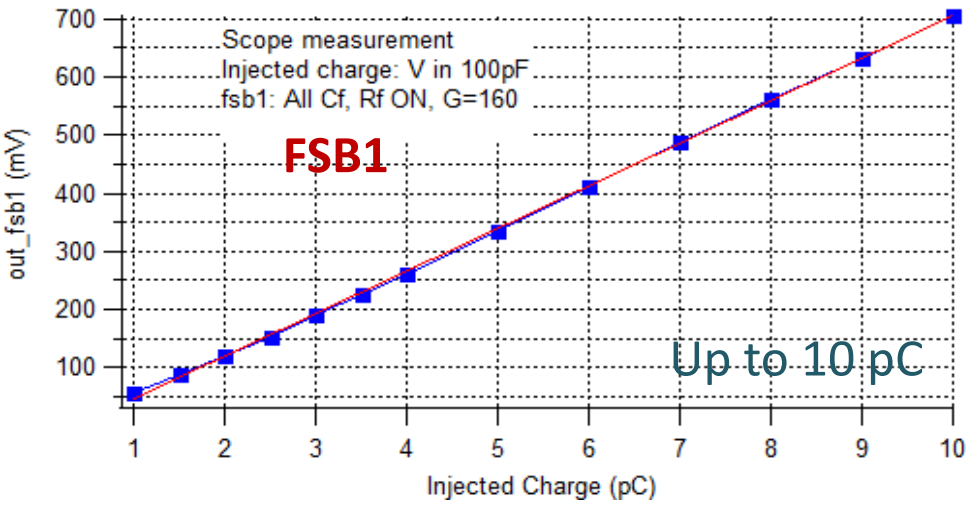


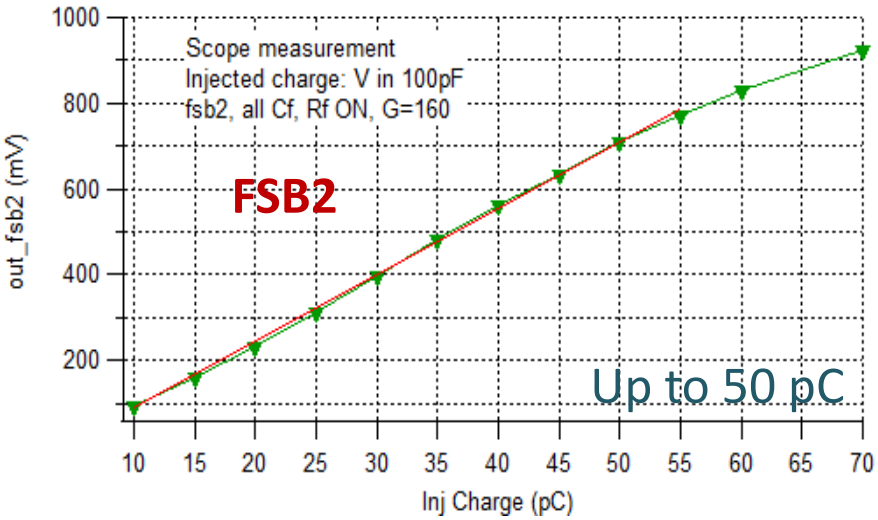
HR3: Analog linearity

Omega

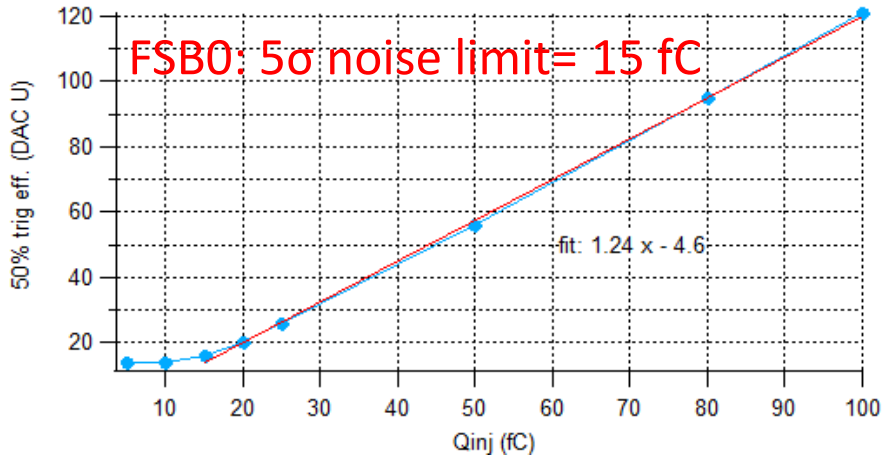
Fast shaper outputs (mV) vs Qinj (fC)







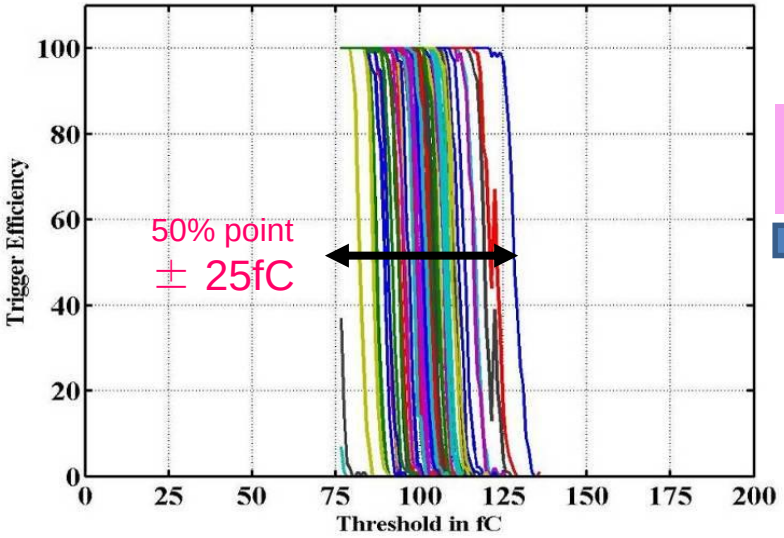
50% trig. Eff. (DAC units) vs Qinj (fC)



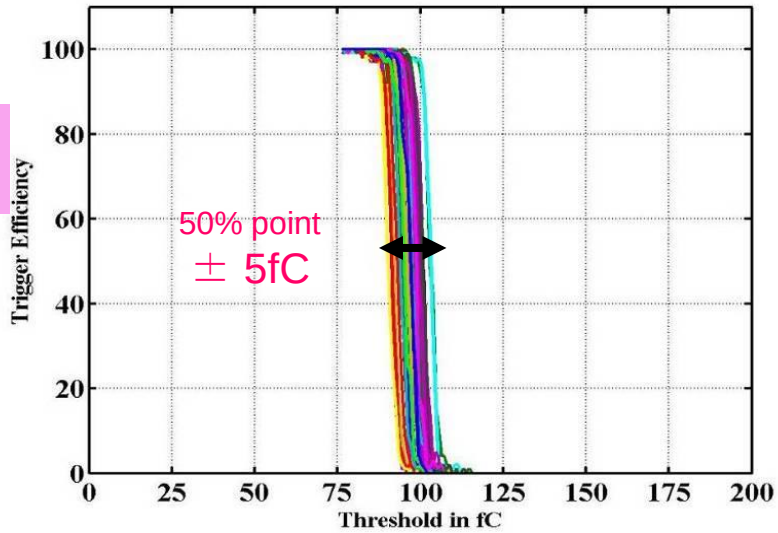
Dynamic range: 15fC - 50 pC

Gain correction / Scurves

Qinj=100fC



HR2 gain correction

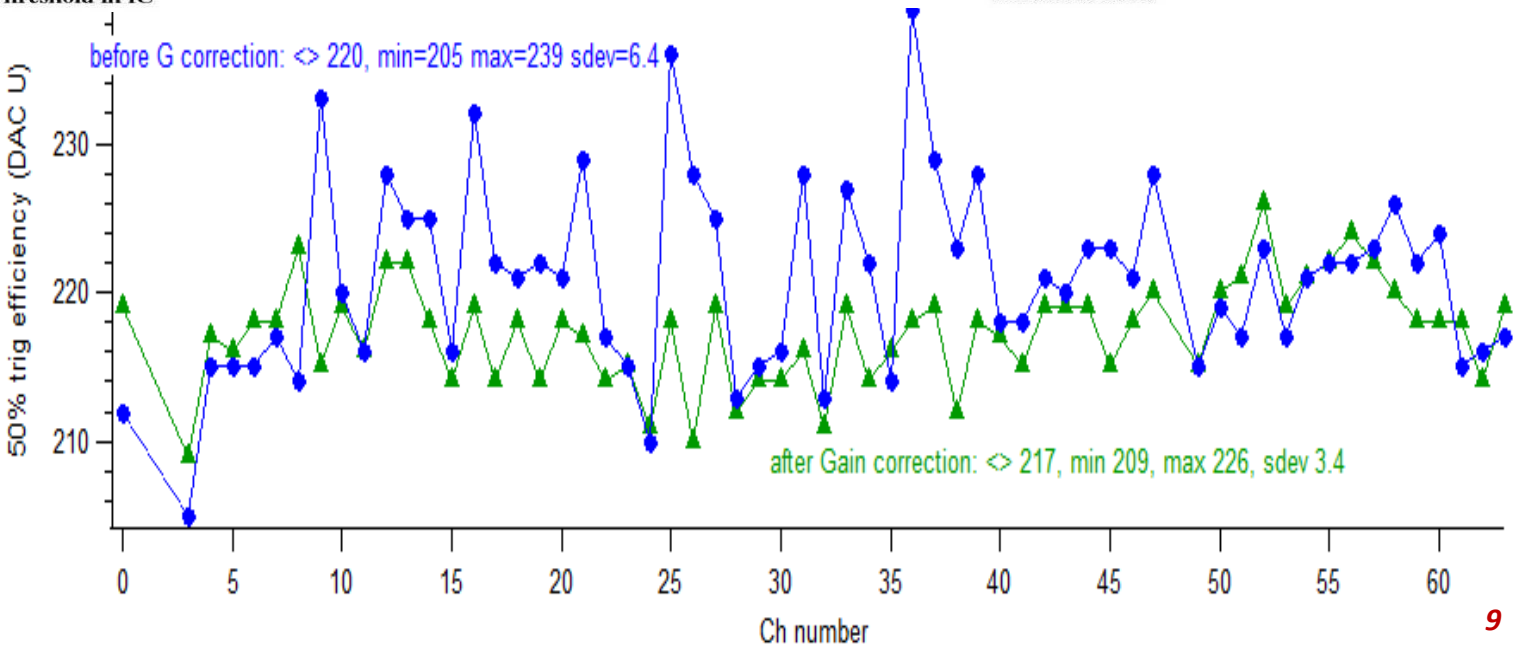


HR3: extracted 50% S-curves point vs Channel number

Before: ± 17 DACU

After: ± 8 DACU

(± 6 fC)

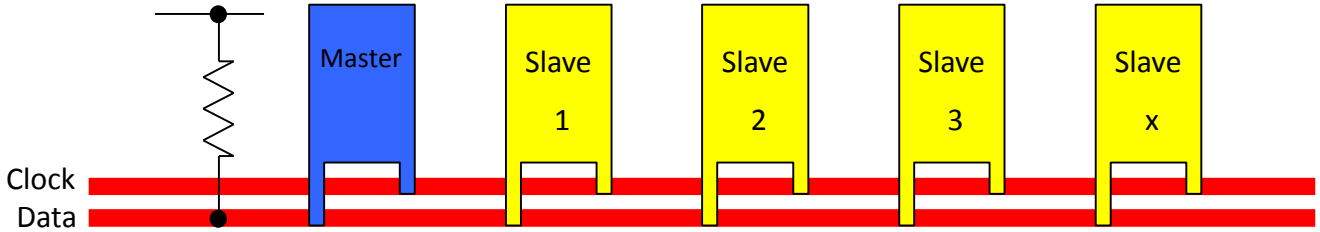


New Slow Control: I2C

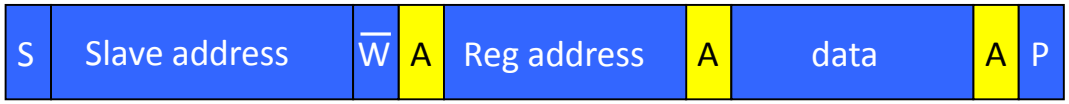
- I2C standard protocol access (max 127 chips / line)

- Possibility to broadcast a default configuration to all the chips
- Read and write access to a specific chip with its geographical address

- Triple voting for each parameter (redundancy)
- Read back of control bit (even if the chip is running / non destructive)



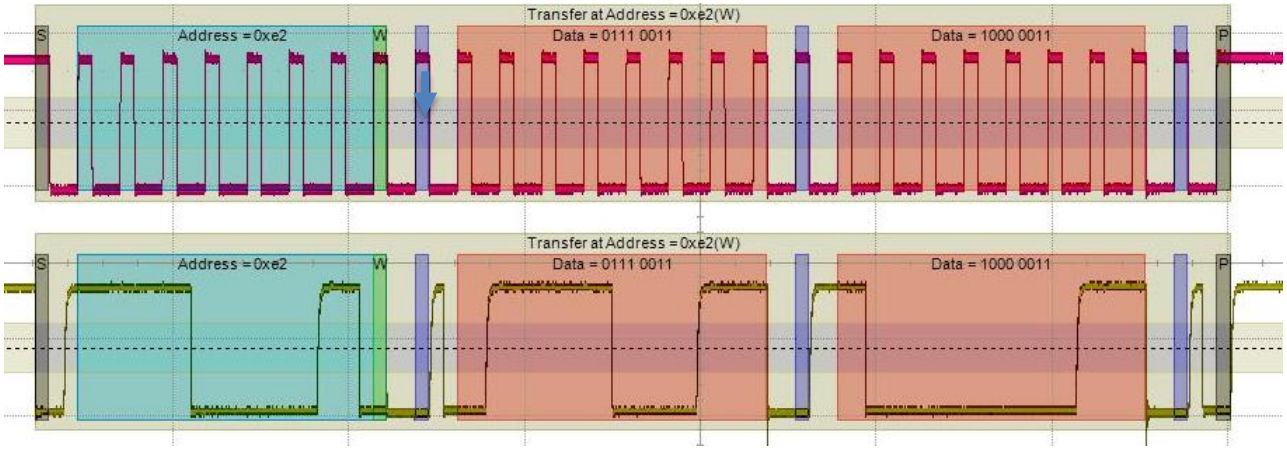
Write frame:



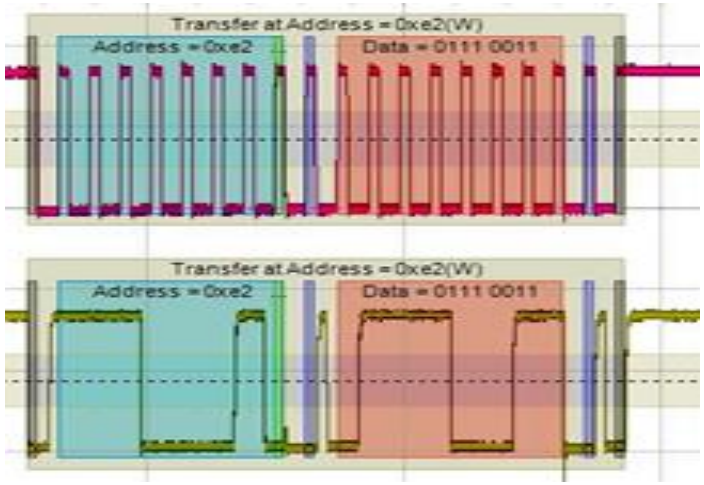
Read frame:

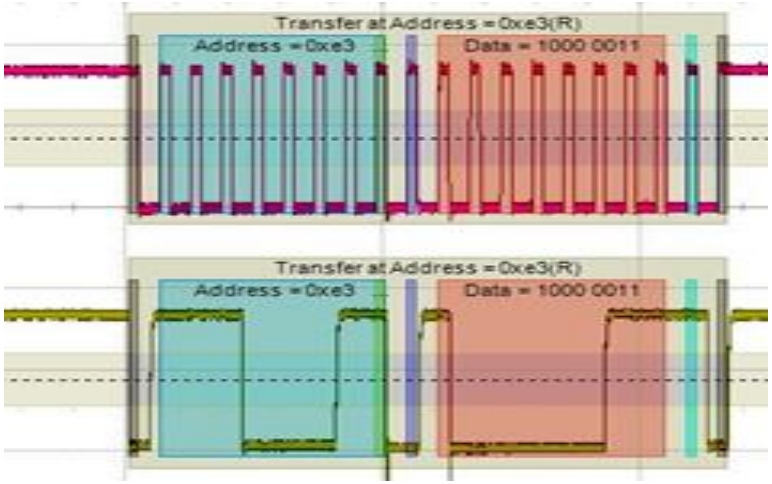
I2C measurements

- I2C Write access : Chip number (ID): 0xE2 / Reg @: 0x73 / WrData: 0x83



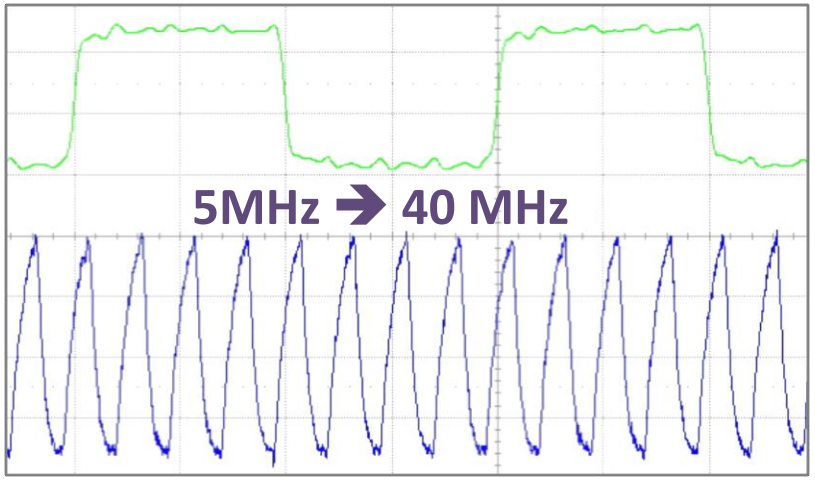
- I2C Read access : Chip number (ID): 0xE2 / Reg @: 0x73



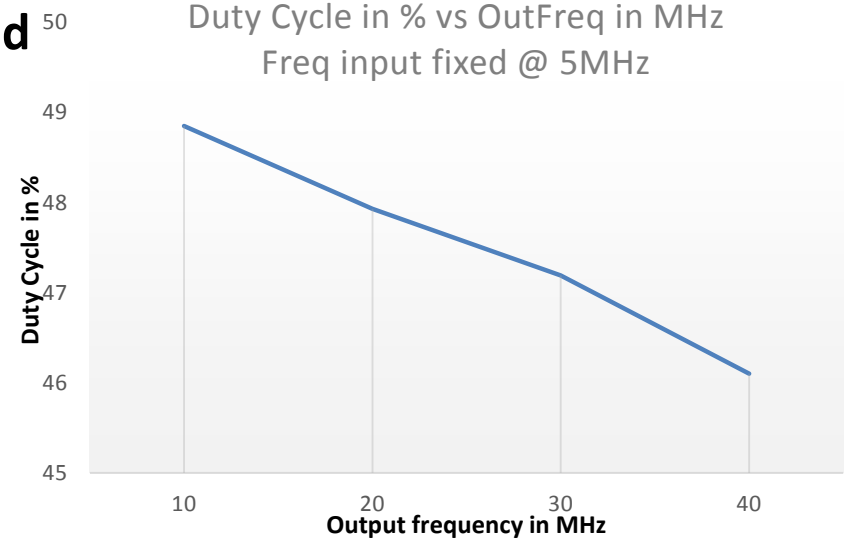


PLL measurements

- **2 clocks are needed to start the chip**
  - Slow Clock (1-10 MHz) related to the beam train (for Time stamping and data readout)
  - Fast clock (40-50 MHz) for internal the state machines



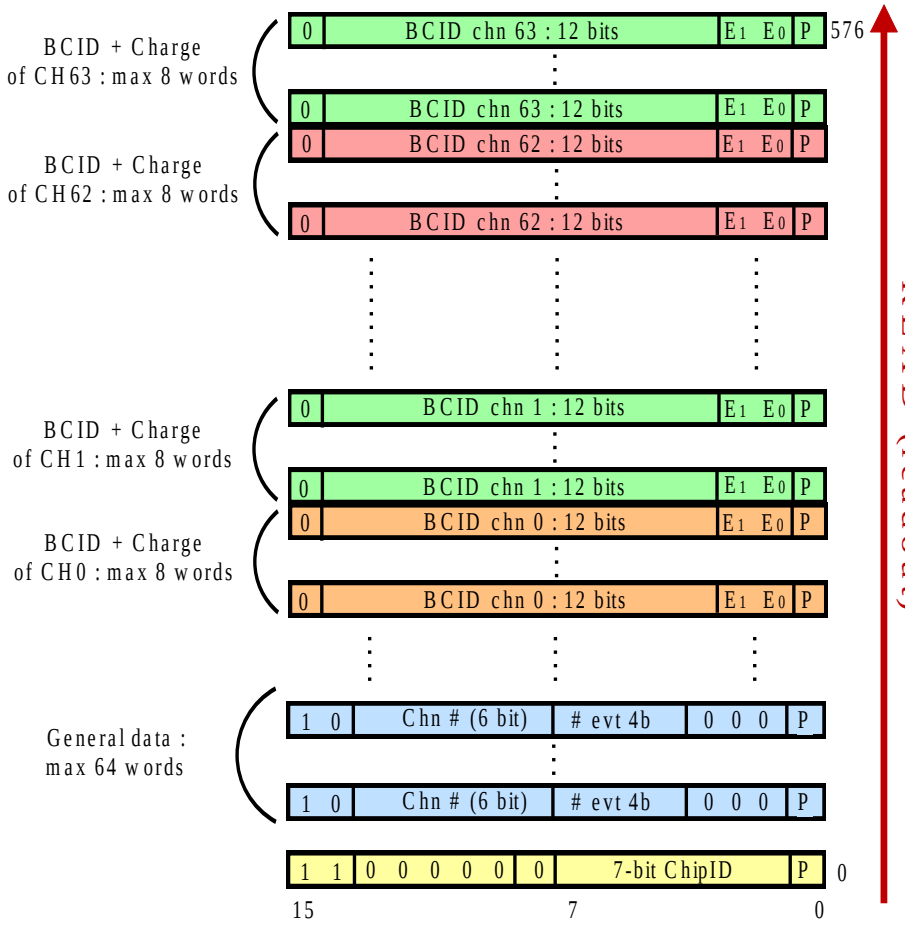
- **A PLL (clock multiplier) has been designed to generate the fast clock**
  - Multiplication factor is (N+1) / N is a SC parameter (1 to 31)
  - Full chain tested using PLL



Zero suppress: Memory mapping

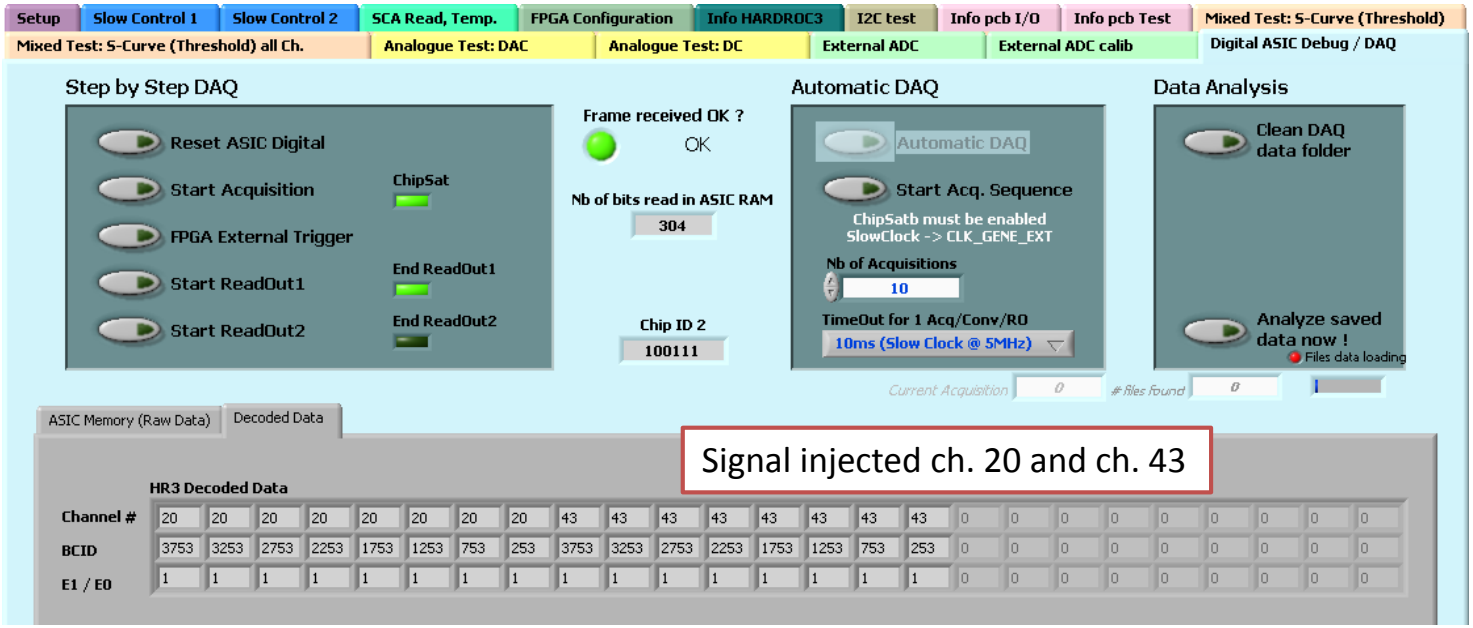
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch. number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



Zero suppress: Tests

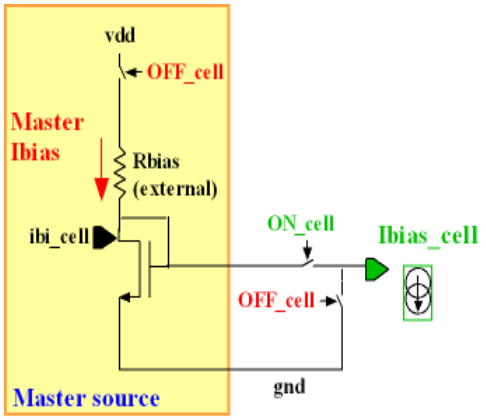
- Zero suppress (only hit channels are readout): test OK



- Roll mode SC : test OK
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : test OK
- "ARCID" SC (Always Read Chip ID): test OK
  - If ARCID = 0 ➔ Backward compatibility: No event ➔ No readout
  - If ARCID = 1 ➔ New behavior: No event ➔ Read CHIP ID

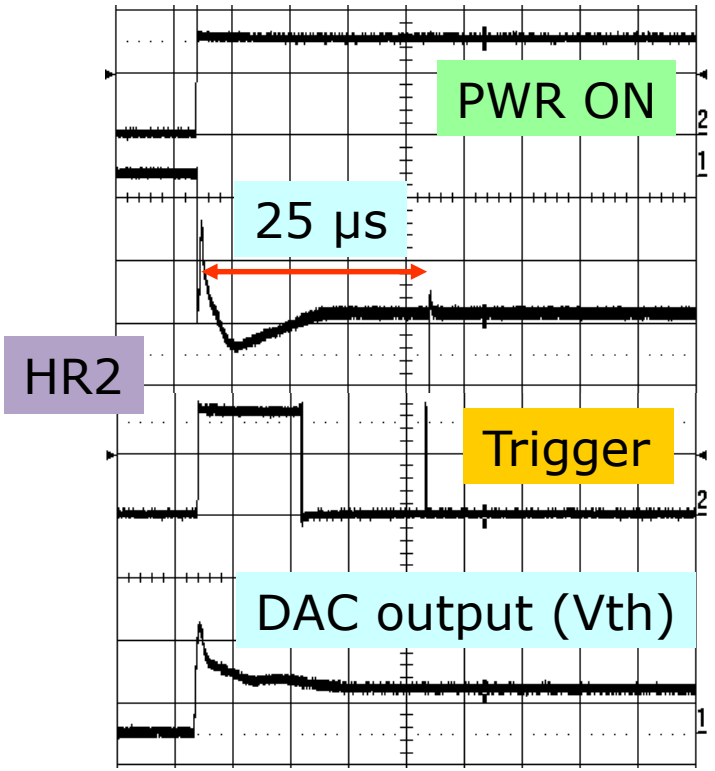
Power pulsing in HR chips

- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
  - No decoupling capacitance on bias and voltage references



- Compared to HR2, HR3 power consumption is higher due to:
  - The extended dynamic range (from 15pC to 50pC)
  - The integration of the zero suppress algorithm
- If the PLL is used, the power consumption is increased by 3% (due to the PLL VCO)

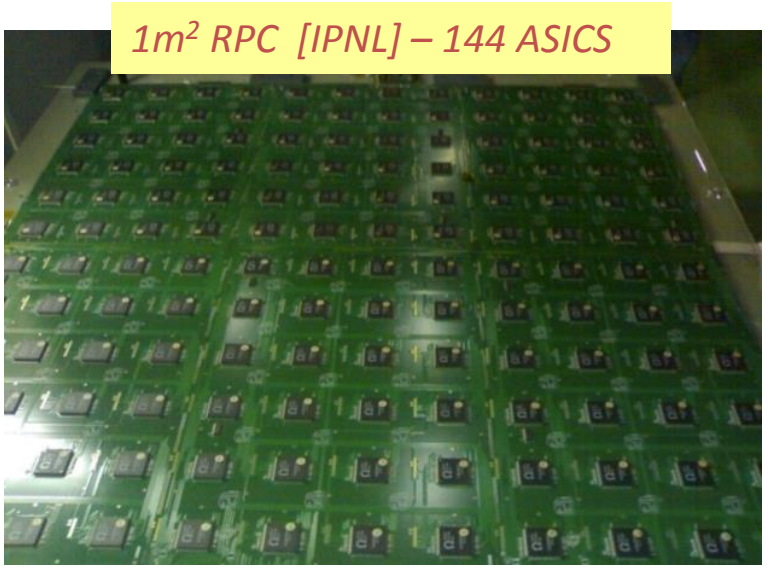
Power supply	HR3 with LVDS (5M + 40M) µW / channel	HR2 with LVDS (5M + 40M) µW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	**12,2**	**7,5**

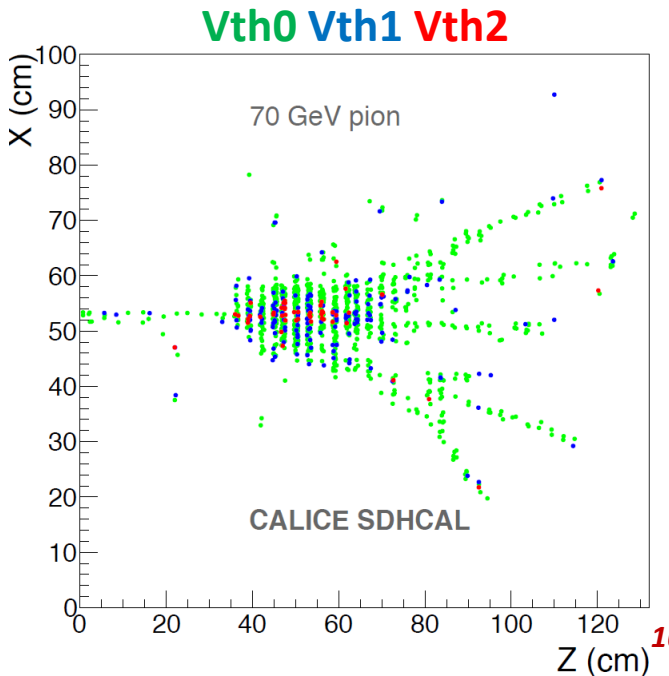


Power pulsing: Testbeam HR2

Omega

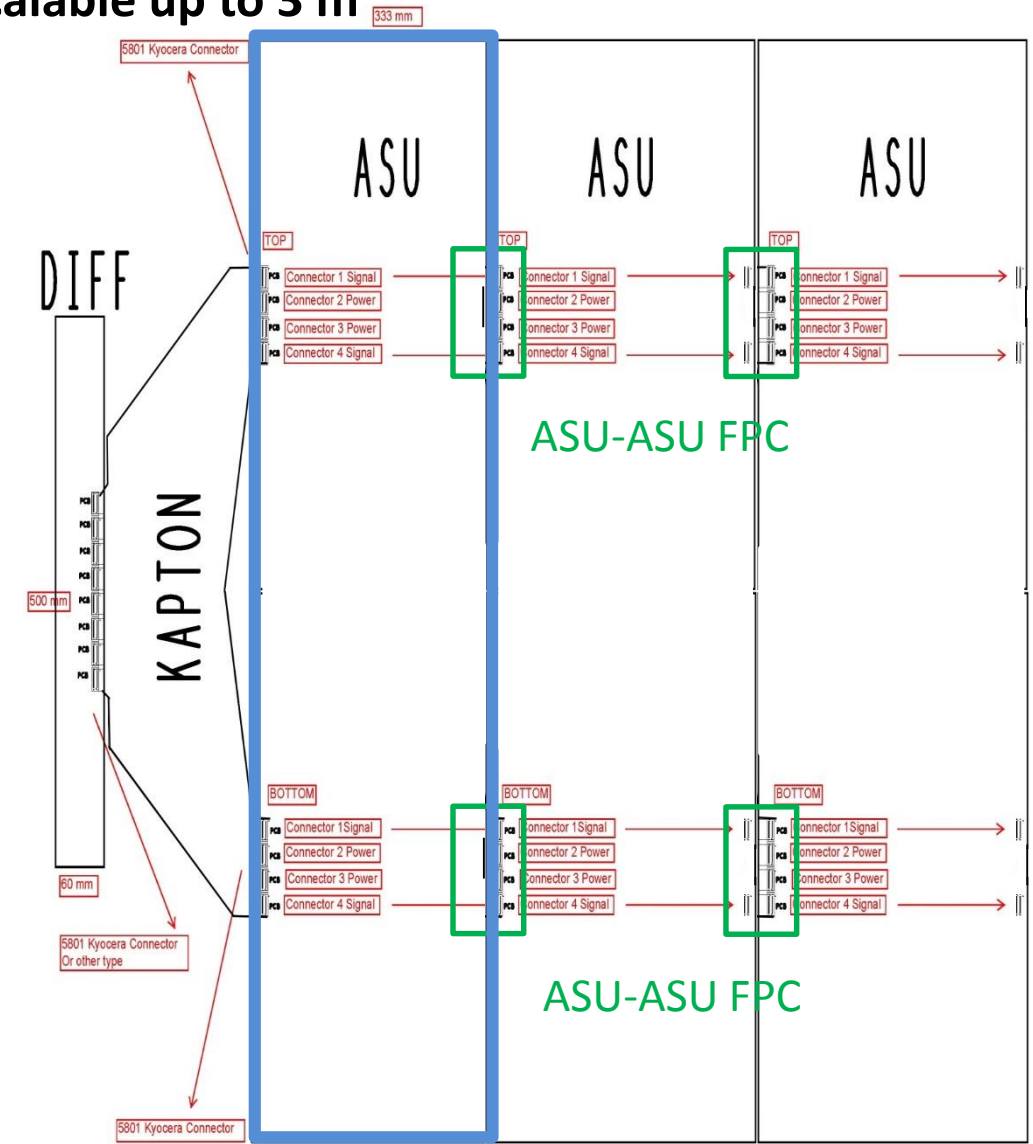
- SDHCAL technological proto with up to **50 layers** (7200 HR2 chips) built in 2010-2011.
  - High Granularity (PAD size : 1 cm x 1 cm)
- Scalable readout scheme successfully tested
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**

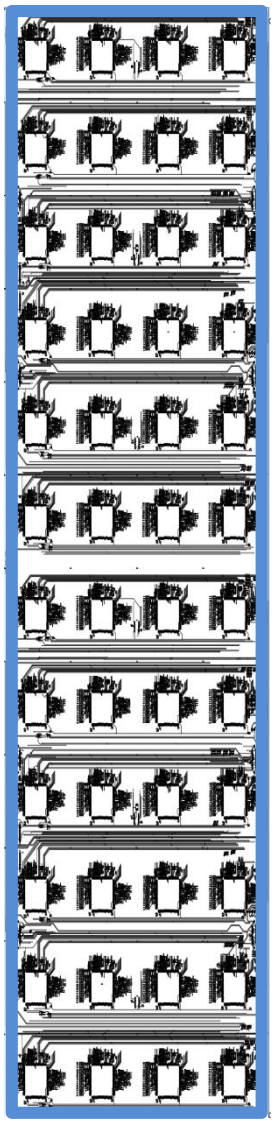




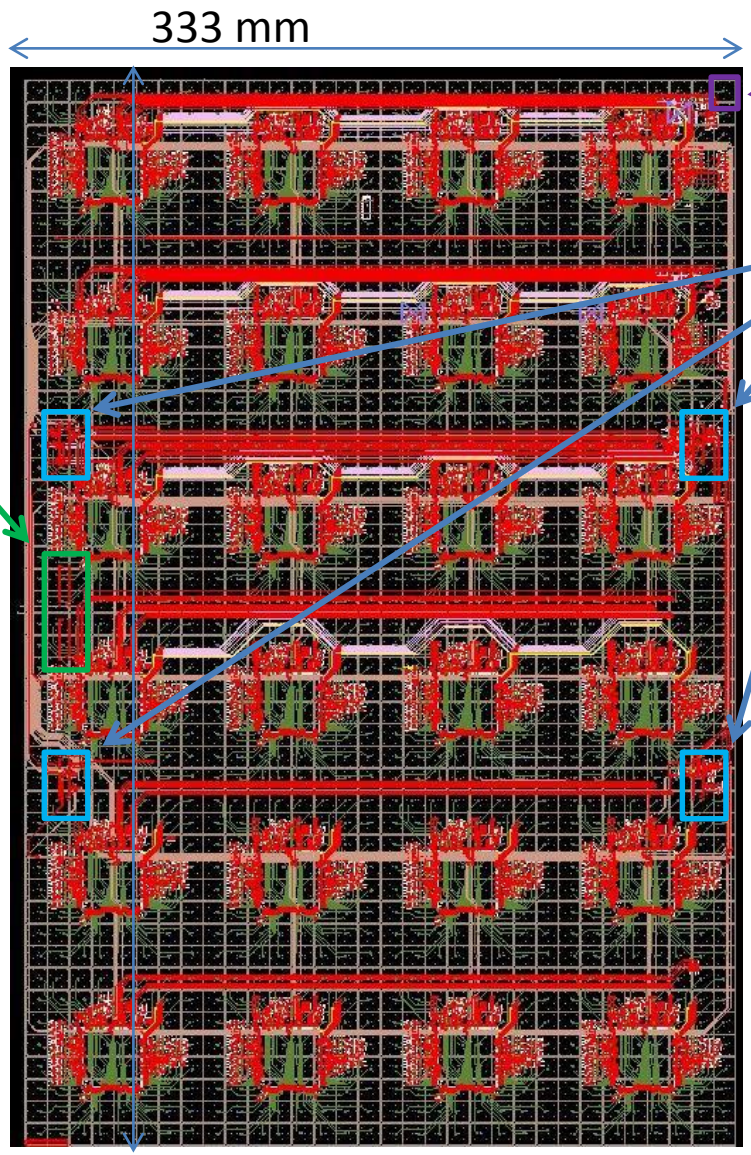
1 m² ASU architecture

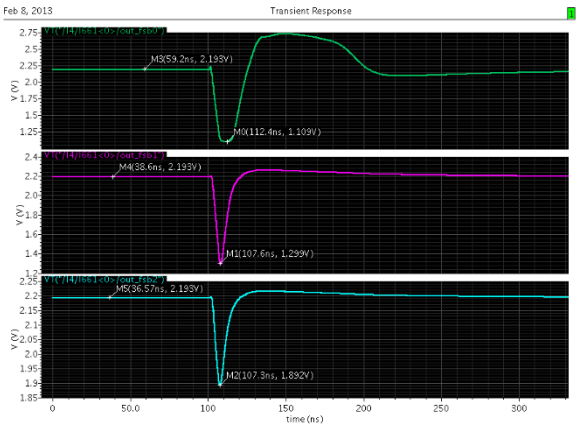
- 1 ASU is 1m x 333mm composed with 48 HR3 chips
- Scalable up to 3 m²

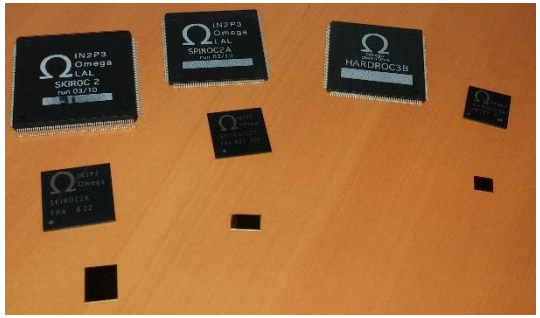




Half ASU Board Layout

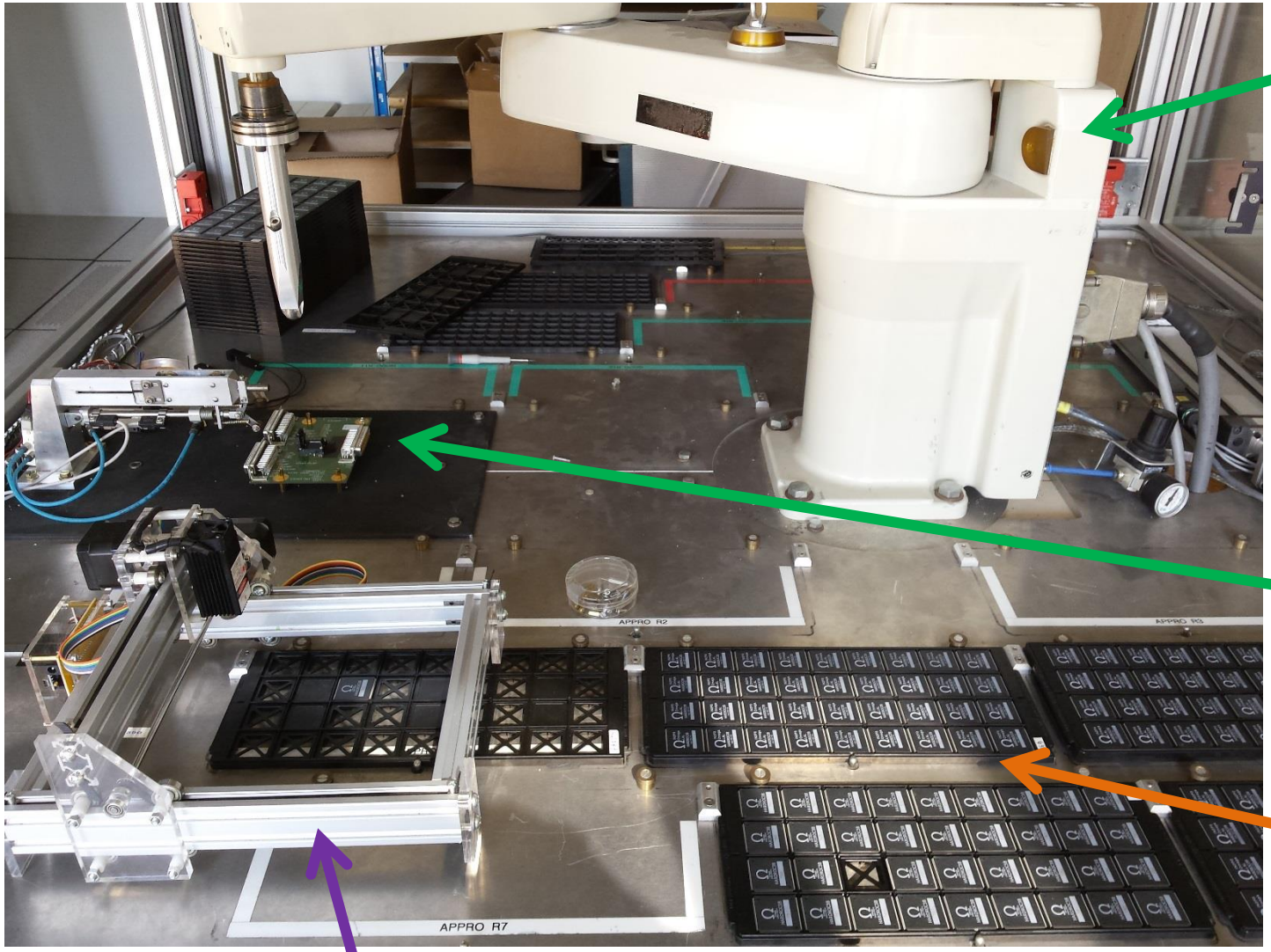






HR3 production tests setup

Omega



HR3 production tests

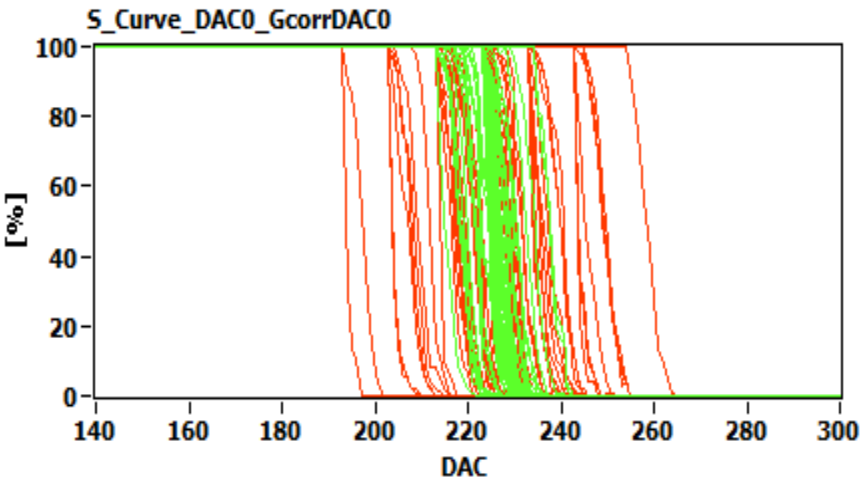
Laser engraving with a robot @ IPNL

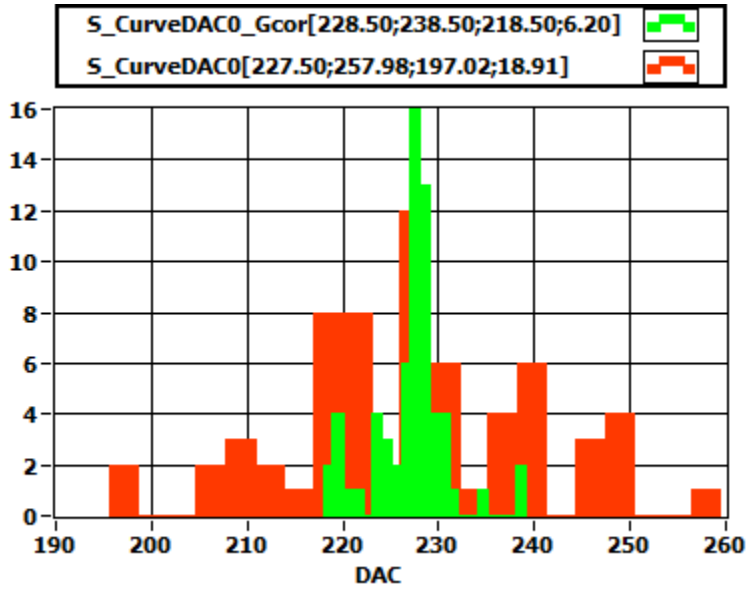
H3B TESTED : 786

Yield : 83.3 %

The majority of discharges :
Dead Channels

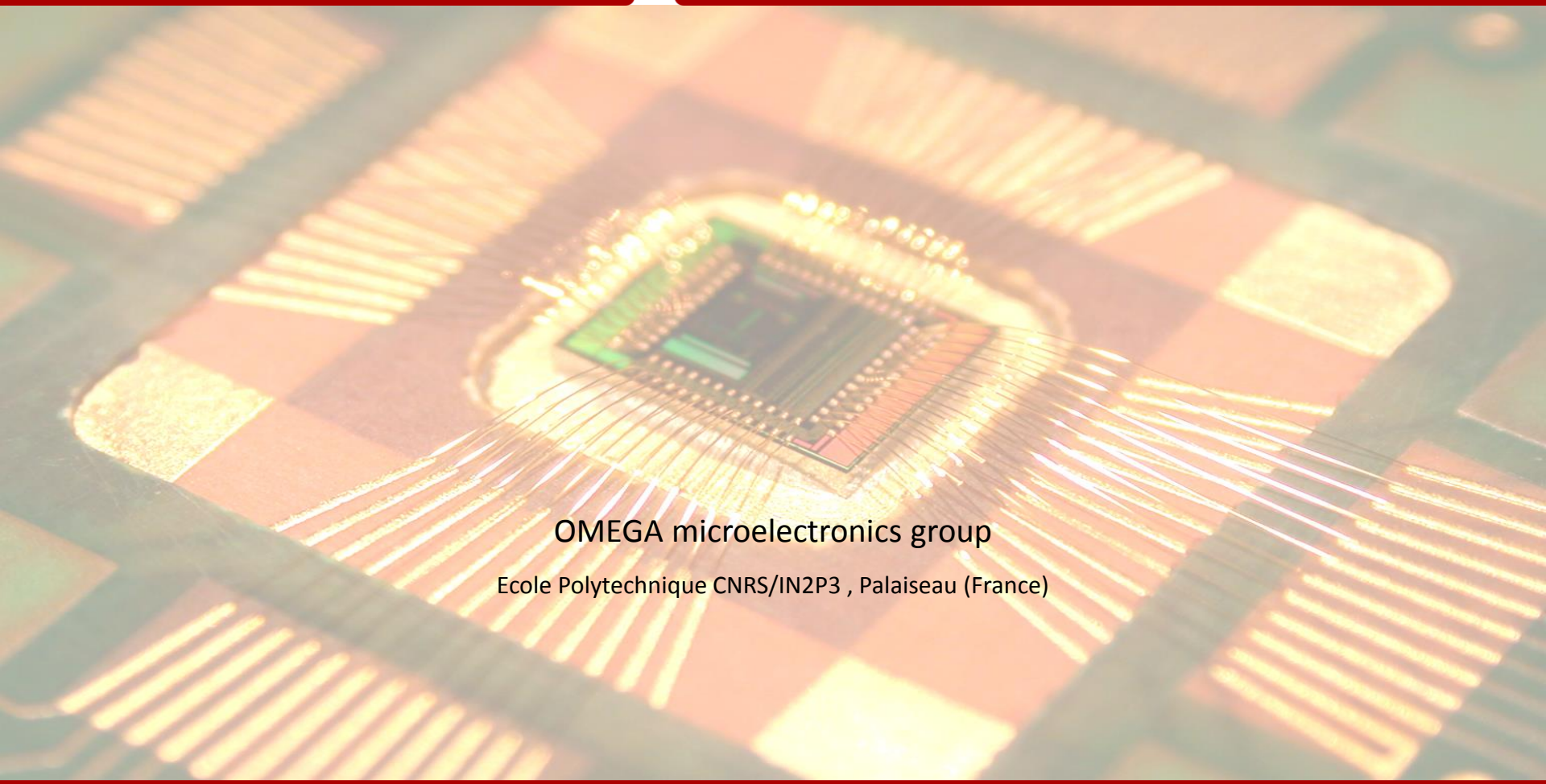
Injection : 100 mV on Ctest (64 Ch)
Gain = 144





Summary and next steps

- Good analog performances
  - Dynamic range extended up to 50 pC
  - Circuit is able to work with only 1 external clock (thanks to PLL)
  - New I2C tested successfully
- New digital features validated on testboard
  - Zero suppress, roll mode, ARCID mode and Noisy event mode
  - External trigger available to be able to check the status of each channel
- Next steps
  - 2-3m long RPC chambers will be built and equipped with HR3 by the end of this year
- OMEGA website: http://omega.in2p3.fr/



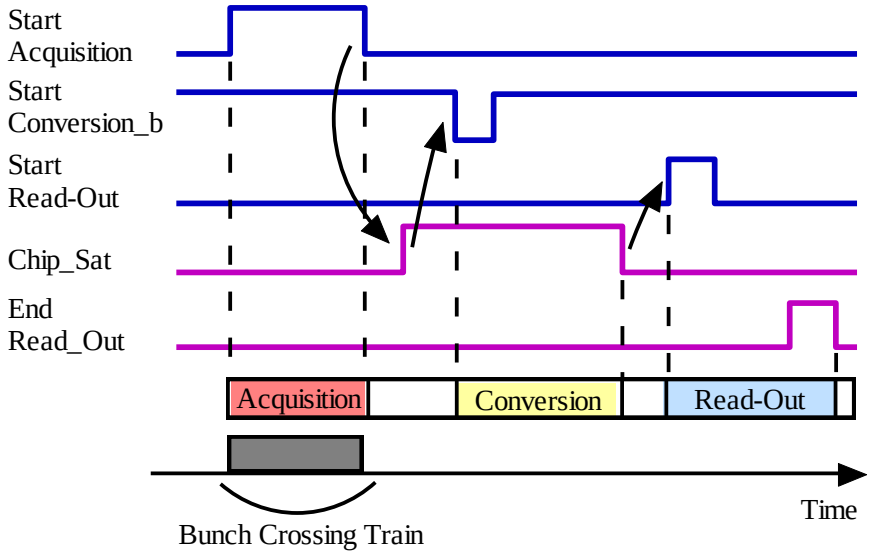
OMEGA microelectronics group

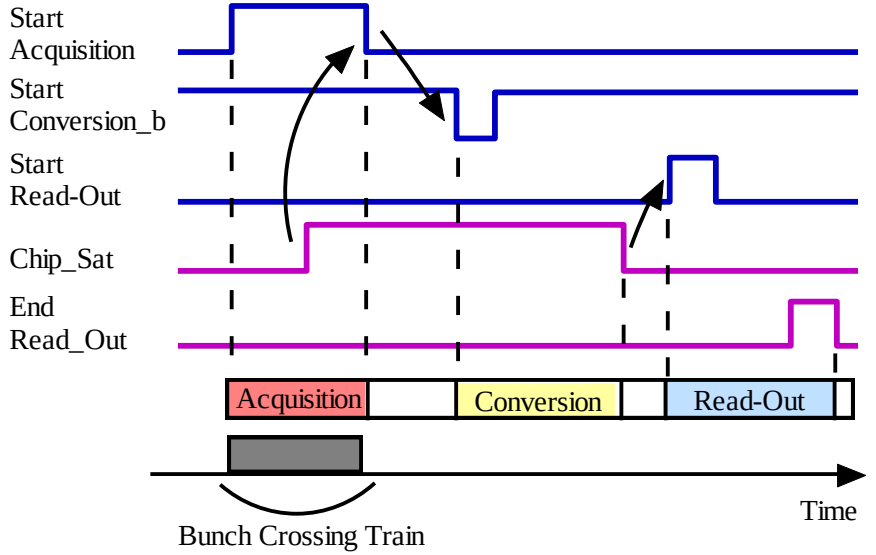
Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

Organization for Micro-Electronics desiGn and Applications

3Gen ROC chips: common features

- DIF sequencing (Acq, Conv and Readout):
  - Backward compatibility with 2Gen ROC chips sequencing
  - Use of ChipSat signal
  - Daisy chained chips for readout

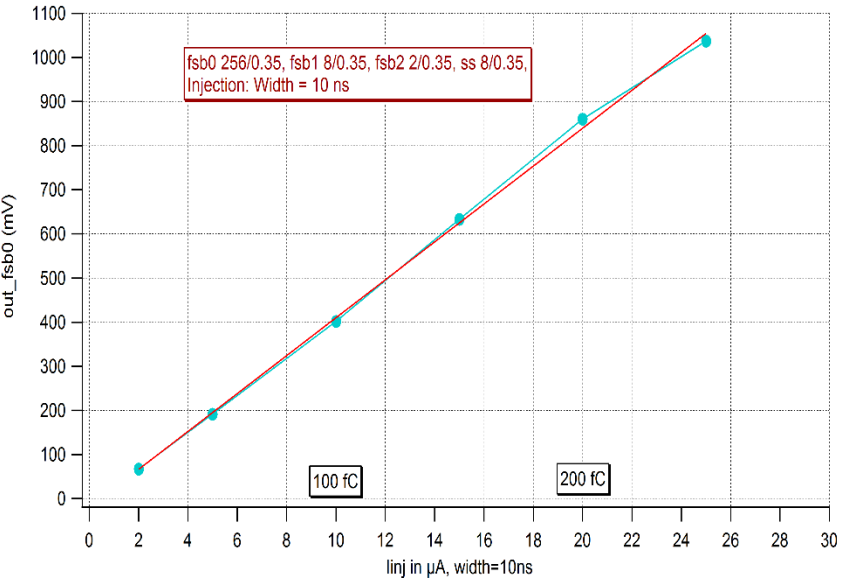


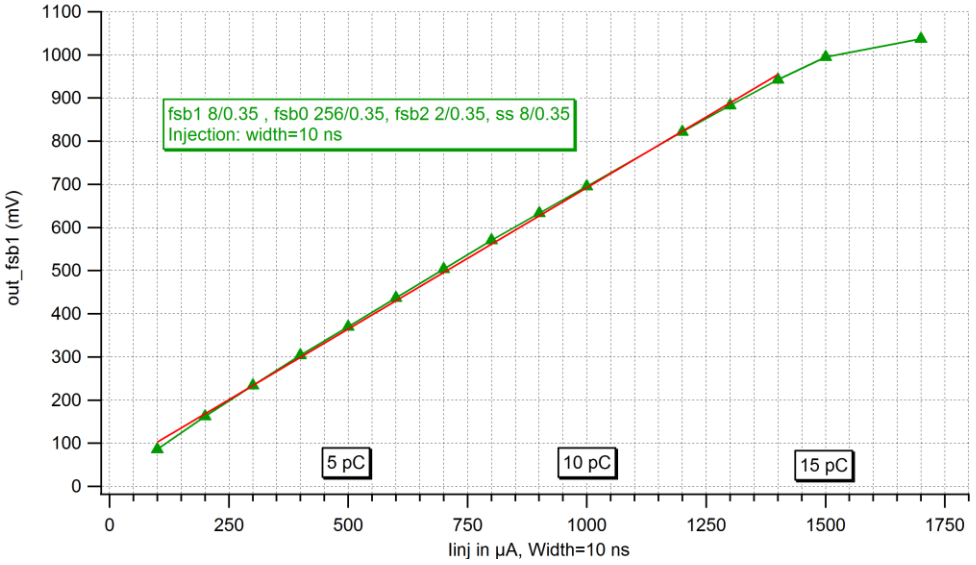


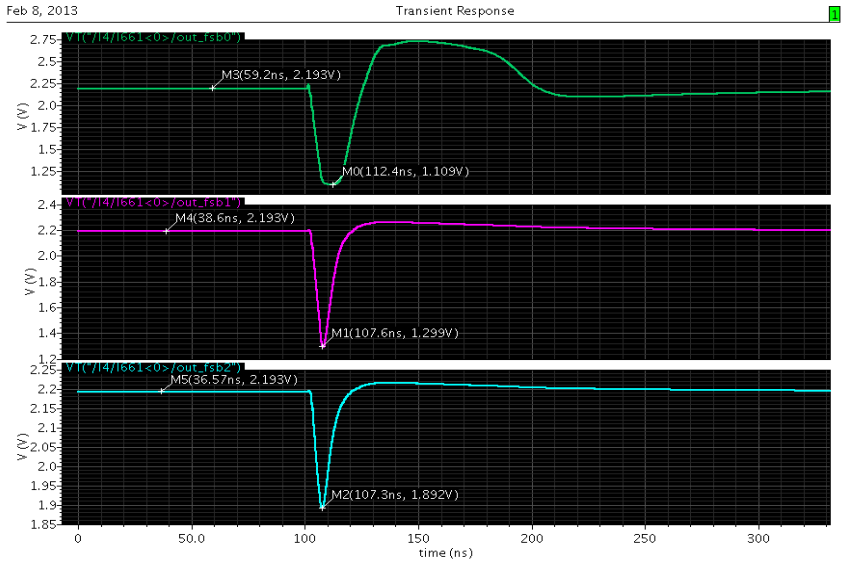
- Possibility to use Roll mode by Slow Control:
  - If RollMode = “0” ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = “1” ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored

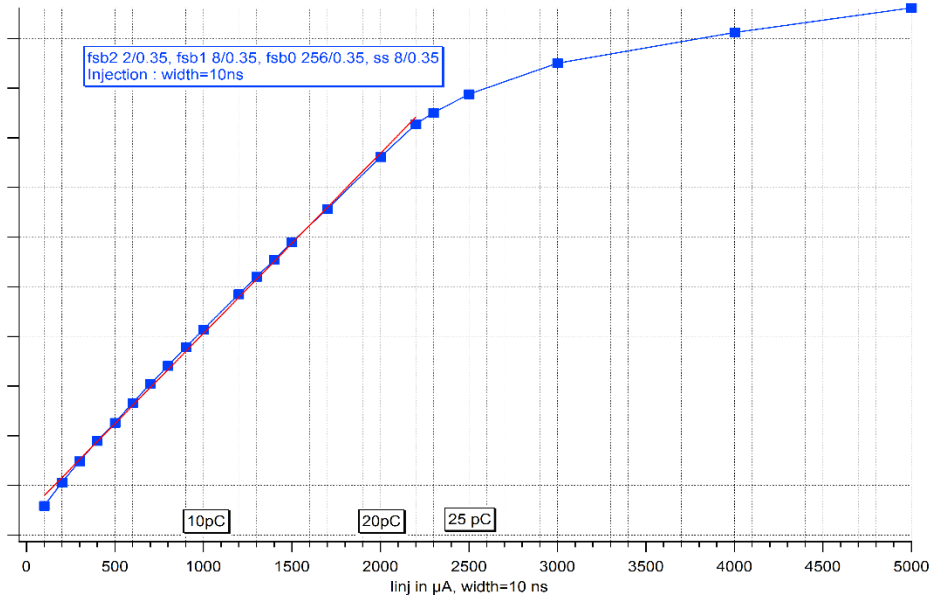
ANALOG PART (Simulations)

Omega









3Gen ROC chips: Slow Control

- Extra pin needed for I2C / SC:
- Possibility to choose between old SC registers/ New I2C link (Select_I2C_SRb available on one pin)

HR 2		HARDROC 3			
sr_in	1	sr_in	1		Standard SC
sr_out	1	sr_out	1		
sr_clk	1	sr_clk	1	Also for I2C	
sr_rstb	1	sr_rstb	1	Also for I2C	
		Loadb_sc	1		SC with triple voting
		SC_WR_RDb	1	Read back SC	
		Error_SCb	1	Triple V. error	
		Select_I2C_SRb	1	Selec old/new SC	I2C
		Select_I2C_Port	1	2 I2C ports	
		7-bit I2C: ChipID<0:6>	7	Pcb hardwired I2C address	
		2 x (I2C_clk / I2C_data)	4	2 I2C ports	
Total	4	Total	4+16		

SC parameters

- Old SC registers/ New I2C link: choice with Select_I2C_SRb

- Bank 1 (WR1, clk1, Load1):
  - 64x8 (gain preamps) + 64 Ctest = 576 bits

- Bank 2 (WR2, clk2, Load2):
  - 3x64 Mask= 192 bits

- Bank 3 (WR3, clk3, Load3):
  - 3 DACx(10 bits +pwr on +EN) + BG (EN+PP) + Temp sensor(EN, PP)=40 bits

- Bank 4 (WR4, clk4, Load4):
  - bias (10 digital and 39 analog) + trigger cell (12) +PLL + spare= 80 bits

DIGITAL PART

Acquisition :

Each channel contains a memory to store up to 8 events. For each event, 14 bits are written into the memory : 12-bit BCID counter + 2-bit encoded charge.

Readout :

The readout is in 3 phases :

- first phase : readout of Chip ID (I2C address on 7-bit)
- second phase : for each channels which contains events it sends general purpose data = channel number with its number of events stored
- third phase : readout of the memory in all the channels (only channels with events)

Clocks :

2 clocks are needed :

- fast clock for state machine (40-50 MHz)
- slow clock for BCID counter and readout (up to 10 MHz)

During acquisition : Fast and Slow clocks used (state machine and timestamps)
During readout : only slow clock is needed

I2C :

SDA / SCL lines duplicated for redundancy (SDA1/SCL1 and SDA2/SCL2) selectable by the "SelectI2C" port
Maximum frequency : to be tested (not more than 1MHz)
Pull-up resistor for open-collector lines : to be tested, depends on frequency
The physical chip address is on 7 bits and hard wired on PCB
Register address inside chip is on 8 bits (115 registers of 8 bits in HR3)