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# HARDROC3, a 3rd generation ASIC with zero suppress for ILC Semi Digital Hadronic Calorimeter

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HARDROC is the very front end chip designed to readout the Resistive Plate Chambers foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider. The very fine granularity of the calorimeter implies thousands of electronics channels per cubic meter which is a new feature of "imaging" calorimetry. Moreover, for compactness, chips must be embedded inside the detector making crucial the reduction of the power consumption down to 12 µW per channel. This is achieved using power pulsing and online zero-suppression.
Around 800 HARDROC3 were produced in 2015. The overall performance and production tests will be detailed.

## Summary

HARDROC (HAdronic Rpc Detector ReadOut Chip) is a very front end chip to readout Resistive Plate Chambers. It integrates a semi-digital readout with three thresholds which enables both good tracking and coarse energy measurement.
The first release of this chip (HARDROC2) was produced in large quantities (10 000 samples) to be able to equip around 50 GRPC layers. This chip was extensively tested with cosmics and also in testbeam at CERN to evaluate the performance and to validate the semi-digital electronics readout system in beam conditions.

Major modifications have been integrated in HARDROC3 to make the channels independent using a zero-suppress architecture. Only hit channels are read out to optimize the data rate and to lower the power consumption. Moreover, the dynamic range has been extended up to 30 pC (10pC in HARDROC2). HARDROC3 is the first 3rd generation chip designed within the CALICE collaboration.

The chip integrates 64 independent channels and also an I2C link (designed by IPNL Lyon) to load the slow control parameters. Each of them has been triplicated for redundancy with triple voting cells.
Each channel is made of a variable gain current preamplifier with a low input impedance to minimize the crosstalk. This variable gain is used to reduce the dispersion between channels thanks to a tuning going up to a factor 2 with an accuracy of 1% over 8 bits. This gain tuning is also convenient to switch off a noisy channel.

The amplified current feeds then two paths:

- A slow shaper path for debug which consists of a CRRC2 shaper and a Sample and Hold buffer. It stores the charg
- Three variable fast shapers (Peaking time  20ns) followed by 3 discriminators. The 3 thresholds are set by 3 i

For each channel, the 3 trigger outputs are OR wired to generate a signal to start the memorization of the encoded trigger outputs as well as the Bunch Crossing IDentification (BCID) delivered by a 12 bit counter. Therefore, there is one memory per channel ensuring the independence of each channel.

The power consumption is 2.5mW/channel and can be minimized down to 12µW/channel thanks to a power pulsing mode (0.5% duty cycle).

A temperature sensor has been integrated as well as a PLL to generate fast clocks internally if needed.

A production of HARDROC3 was launched in 2015 to be able to equip large RPC detectors (1m2). Around 800 chips were successfully tested with a robot.

The overall performance of this new HARDROC3 will be described with detailed measurements of all the characteristics. The improvements compared to the previous chip will be highlighted.

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