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A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC

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This paper describes a readout ASIC prototype designed by CHIPIX65 project, part of RD53, for a pixel detector at HL-LHC. A 64x64 matrix of $50x50\mu m^2$ pixels is realised. A digital architecture has been developed, with particle efficiency above 99.5 % at 3GHz/cm^2 pixel rate, 1MHz trigger with 12.5μsec latency. Two analog front end designs, one synchronous and one asynchronous, are implemented. Charge is measured with 5-bit, analog dead-time below 1%. IP-blocks (DAC, ADC, BandGap, SER, sLVS-TX/RX) and very front ends are silicon proven, irradiated to 600Mrad.

Summary

The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. Major experimental challenge resides in inner tracking detectors: here the dimension of sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes a readout ASIC in 65nm CMOS with a matrix of 64x64 pixels each of dimension 50x50 μm^2, designed by CHIPIX65 project, part of RD53 Collaboration. It is a demonstrator of a Pixel Phase 2 chip, with compact design, low power and in-time threshold below 1000e$^-$. All IP-blocks and analog front ends are designed by CHIPIX65 project in the framework of RD53 Collaboration: they have been produced, tested and several have already proven to be radiation hard up to 5-800 Mrad.

The chip implements two different analog front end designs, one with asynchronous the other with synchronous comparator designs, but with main common characteristics: compact design; ENC below 100 e- for 50 fF input capacitance; below 5 μW/pixel power consumption; fast rise time, allowing correct time-stamp; signal digitisation using Time Over Threshold; leakage current compensation up to 50nA per pixel.

All global biases and voltages are programmed in the chip periphery, for each value a 10-bits current steering global DAC is used; a band gap circuit provides a stable reference voltage. The adopted strategy is very robust, easily scalable and mismatch effects are kept to a negligible level. Bias voltages and current are monitored by a 12-bit ADC.

A novel digital architecture has been designed in order to maintain a high efficiency (above 99%) at pixel hit rate of 3 GHz/cm^2 , trigger of 1 MHz rate and latency of 12.5μsec. The digital architecture is organized into pixel regions: in order to have a very compact and low power architecture, a large pixel region consisting of 4x4 pixels has been used. A 5-bit ToT charge is stored in a centralised latency buffer: at the arrival of a trigger, a matching logic selects eventually the right memory location and sends the data to the End of Column logic. The particle inefficiency due to this architecture is about 0,1% for an area occupation of of 65% and a low power consumption. The readout is obtained using a column drain protocol with a FIFO for each pixel region column, connected to a global dispatcher FIFO that after a 8b10b encoding splits the data into 20-bit trunks and sends them to a serialiser.

Data are sent out from the chip using a differential transceiver converting the CMOS into SLVS JEDEC 400mV standard. Given the small size of the chip, an output rate of 320 MHz for the serialised data can be used, but higher output rates are possible., since SER and sLVDS-TX are designed to sustain up to 1.2 Gb/s. Chip configuration is performed through

fully-duplex synchronous SPI-master/slave transaction.

CHIPIX65 demonstrator will be submitted in June 2016.

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