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Development of the ABCStar front-end chip for the ATLAS Silicon Strip Upgrade

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The ATLAS experiment will use an all-silicon tracker in the Phase II upgrade for the HL-LHC collider at CERN. For the Silicon Strip detector of the ITk, a new readout chip ABCStar is under design to meet the new requirements of higher trigger rates and lower latency. We summarize the status of this work and present the new features of the chip.

Summary

The ABCStar chip is a new generation of front-end readout ASIC for Silicon Strip Detector in ATLAS Phase II upgrade. This chip provides all functions required for processing the signals from 256 strips of a silicon strip detector in the ATLAS experiment employing the binary readout.

The architecture chosen for ABCStar allows a multi-trigger data flow control retaining the Beam Crossing synchronous pipeline transfer signal (L0 here) from previous versions, an asynchronous Regional Readout Request (PR here) and a second level asynchronous data readout intended for a global readout (LP here).

Besides the essential front-end and power regulation, the main functional blocks of the digital part are: Mask and Edge Detection, pipeline, event buffer, cluster finder, readout logic, command decoder, threshold and calibration control.

The signals from the detector are first processed by the front-end which contains 256 analogue preamplifier-shapers followed by discriminators with individual threshold trimming capabilities. The binary output of the discriminator are sampled at the bunch crossing clocking rate and stored in the pipeline after "edge detection" process. At the reception of L0 signal, the data in the memory that were stored at some fixed latency time before the L0 signal are extracted from the pipeline and transferred to the event buffer and stored as events tagged with an appropriate L0ID number. If a PR or LP signals are received with the corresponding L0ID number, the event is extracted from the event buffer and processed through the cluster finder. The cluster finder block acts as a data reduction circuit, creating a "cluster"byte for channels found with hits. The readout block does formatted packets with the event identification and the associated cluster bytes. The data is transmitted serially to the following HCC chip with point to point connection.

In order to meet the new requirement of higher trigger rates and lower latency, the ABCStar differs from ABC130 and its predecessors, especially in the digital part. It employs the edge detection circuit in front of the pipeline to adapt to the possible consecutive L0s, this also simplify the control logic of the two step memories. A cluster finder block with new algorithm was designed, which is much faster to fulfill the latency requirement in PR readout mode. Other features like the hit counter based calibration mode, L0-tag are also considered to add to the logic design of ABCStar.

At present, we have built up the whole data path for the digital design, and the protocol of ABCStar command and control from the companion chip HCCStar is still in definition phase. The functional verification for the whole digital part using the Universal Verification Methodology (UVM) is also under progress.

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