SKIROC2_CMS

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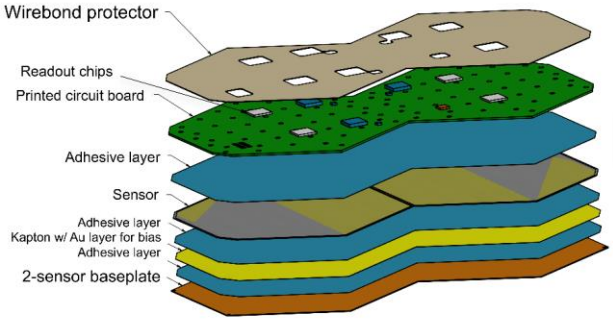
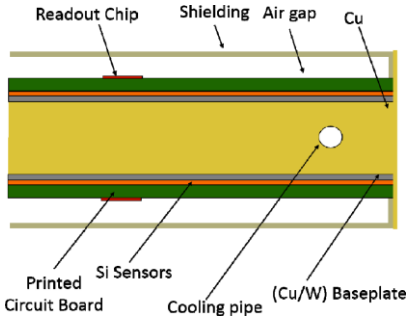
Organization for Micro-Electronics desiGn and Applications

HGCAL calorimeter for phase 2 (technical proposal)

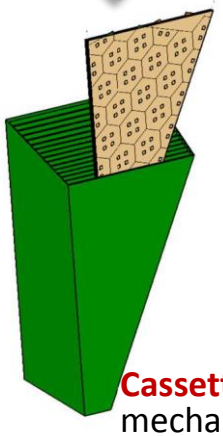
Modules
With 2x 6 - 8" Hexagonal Si sensors,
PCB, FE chip, on W/Cu baseplate



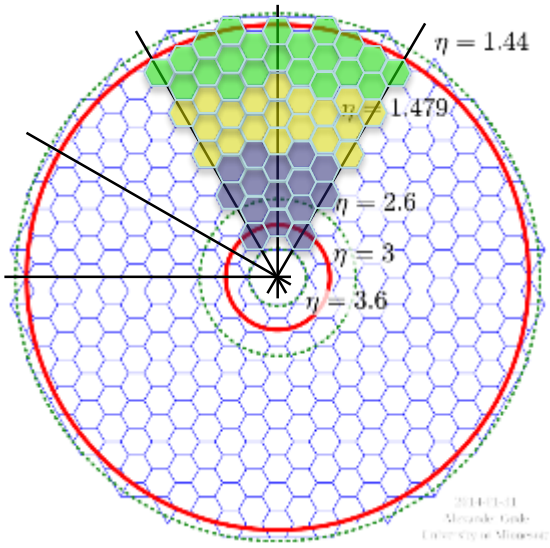
Modules mounted on Cu Cooling plate
with embedded pipe
=> **Cassettes**

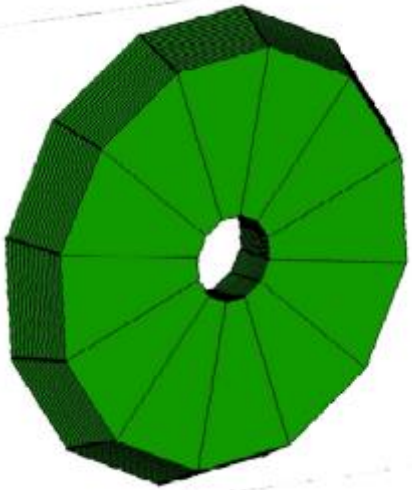


Final design still under develoment

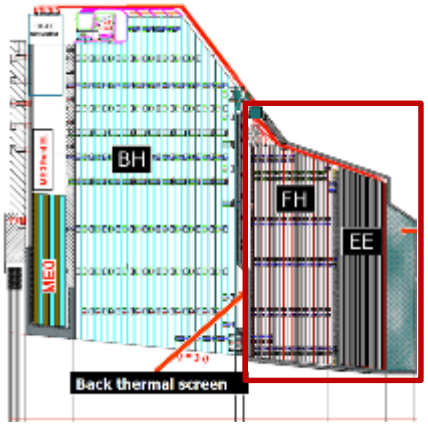


Cassette inserted in mechanical structure (containing absorber)





12 **Cassettes** mounted together to form the **ECAL (EE)** **and** **Front HCal (FH)**

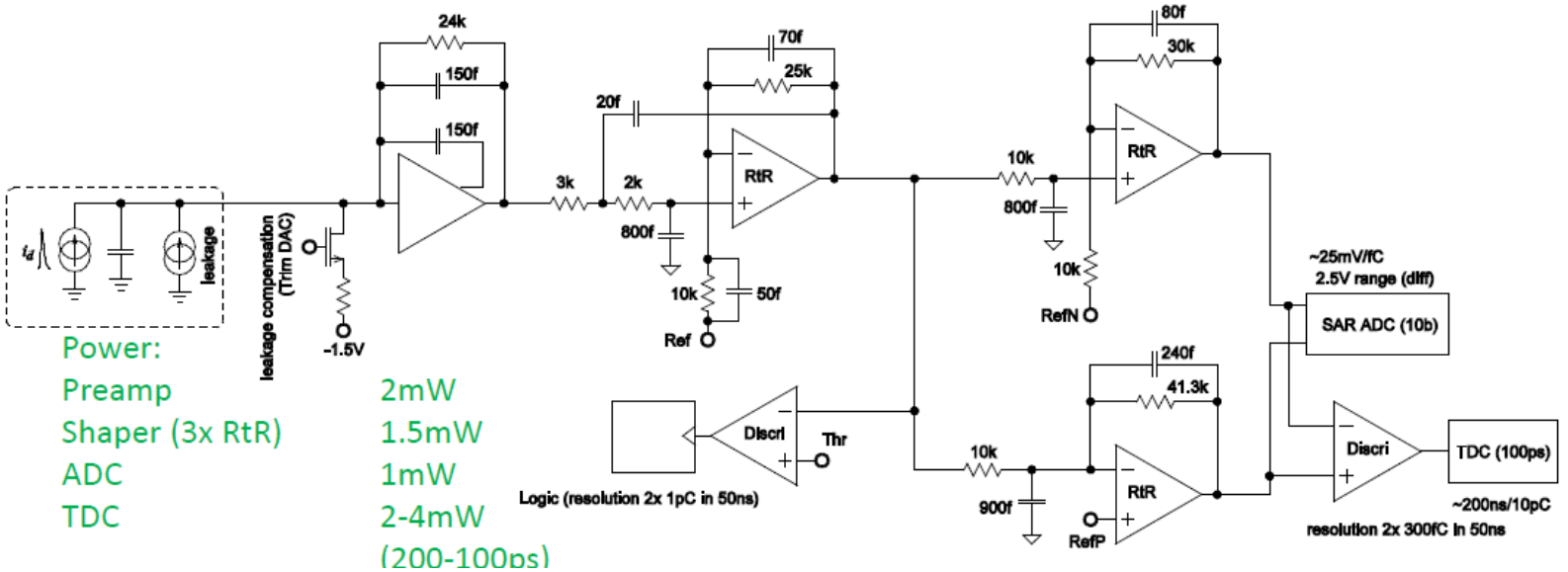


Replaced EndCap (maintained at -30°C

3 sensor active thicknesses 100-200-300 µm
0.5-1 cm^2 pads for 100(-00/300) µm
Capacitance ~30-50 pF

HGCAL Front-End electronics

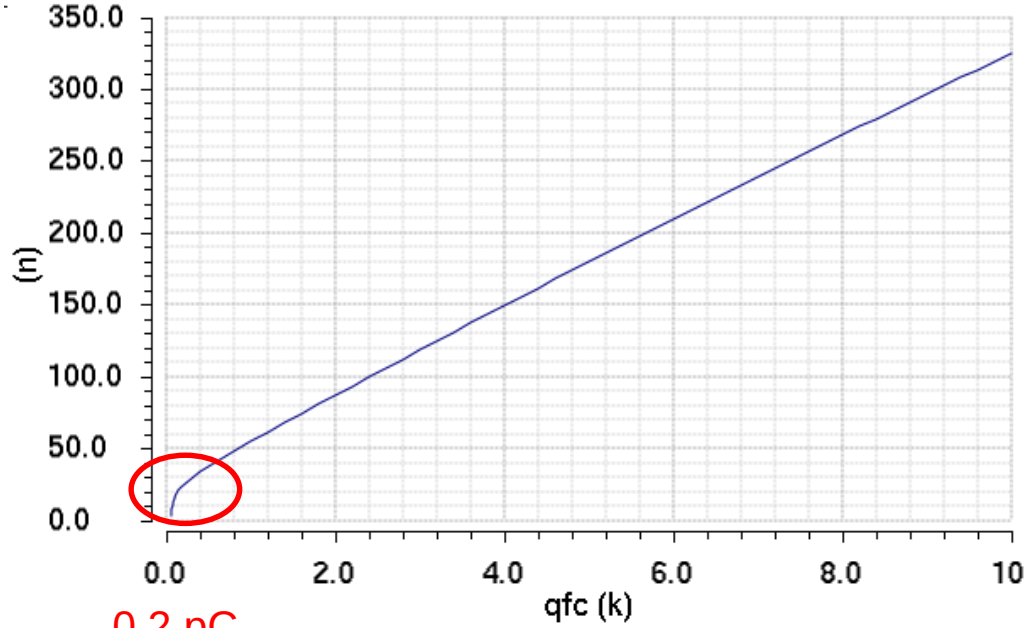
- Stringent requirements for Front-End Electronics
  - Low power (<10 mW), low noise (<2000 e-), high radiation (200 Mrad, $10^{E}16$ N)
  - System on chip (digitization, processing…), high speed readout (5-10 Gb/s)
  - ~92,000 FE chips
- Baseline : charge + ToT [J. Kaplon CERN]
  - Charge readout 0-100 fC (0-50 MIP) 10 bits
  - Time over Threshold (0.1-10 pC) (40-2000 MIPs) : 12 bits
  - In addition : timing information to 50 ps accuracy
  - Variants : more classical readout (bi-gain) or switched feedback [Omega]



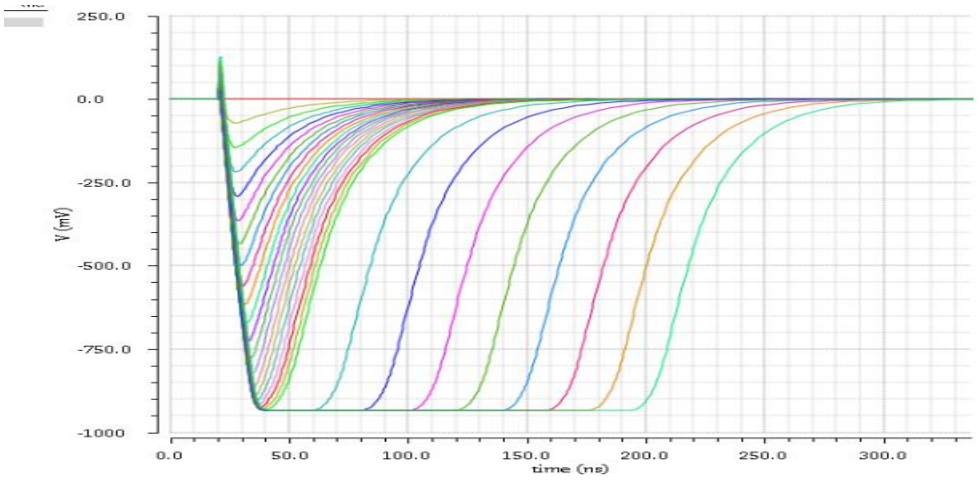
VFE architectural issues

- key issues to be studied :
  - Noise
  - Resolution
  - Stability
  - Linearity
  - Accuracy
  - Calibration
  - crosstalk
  - Radiation
  - Timing
  - Systematic effects

- And also
  - 65/130 nm
  - System issues
  - Trigger path



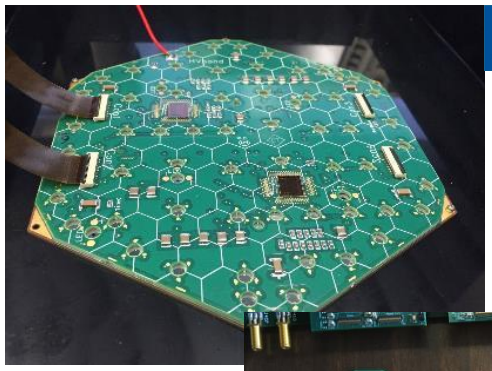
0.2 pC
~100 MIPS

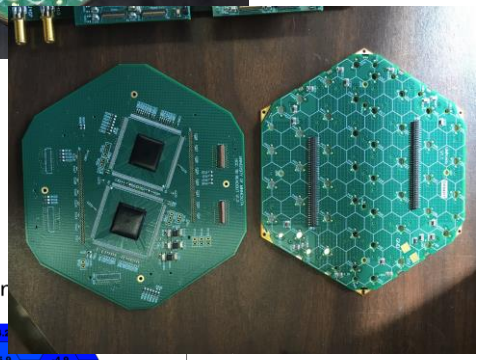


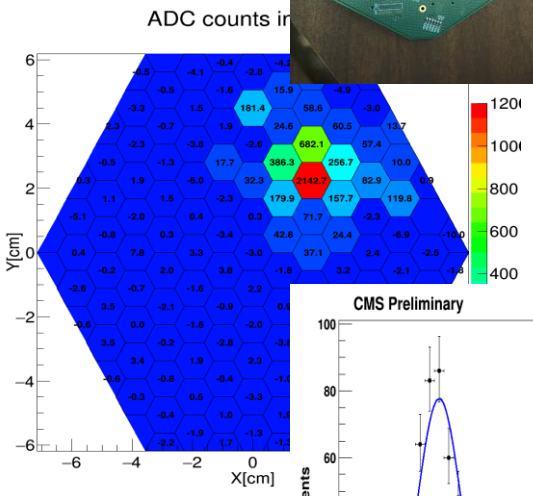
SKIROC2-CMS: Electronics for testbeam

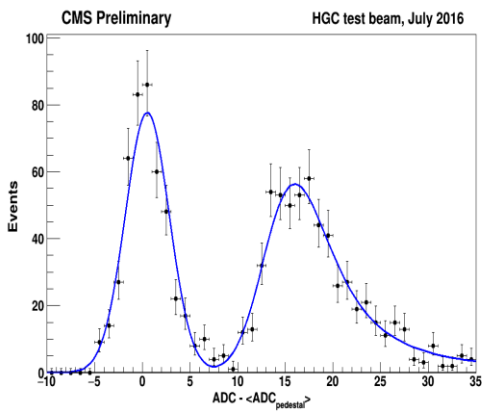
- Testbeam electronics
  - Use SKIROC2 from CALICE to exercise system issues (low noise, large range)
  - Complex front-end boards designed at UCSB and FNAL and CERN
  - Evolutive readout designed at FNAL

- Development of **SKIROC2-CMS**
  - Optimized version for CMS test beams, pin to pin compatible
  - Dual polarity charge/current preamplifier
  - Faster slow shaper (25ns instead of 200ns)
  - SCA in roll mode (sampling of slow shapers @ 40MHz, depth = 300ns)
  - ToT for high input charge
  - TDC (TAC) for ToA (~20 ps binning, ~50ps jitter)
  - Will replace SKIROC2 on modules for **timing and ToT studies**



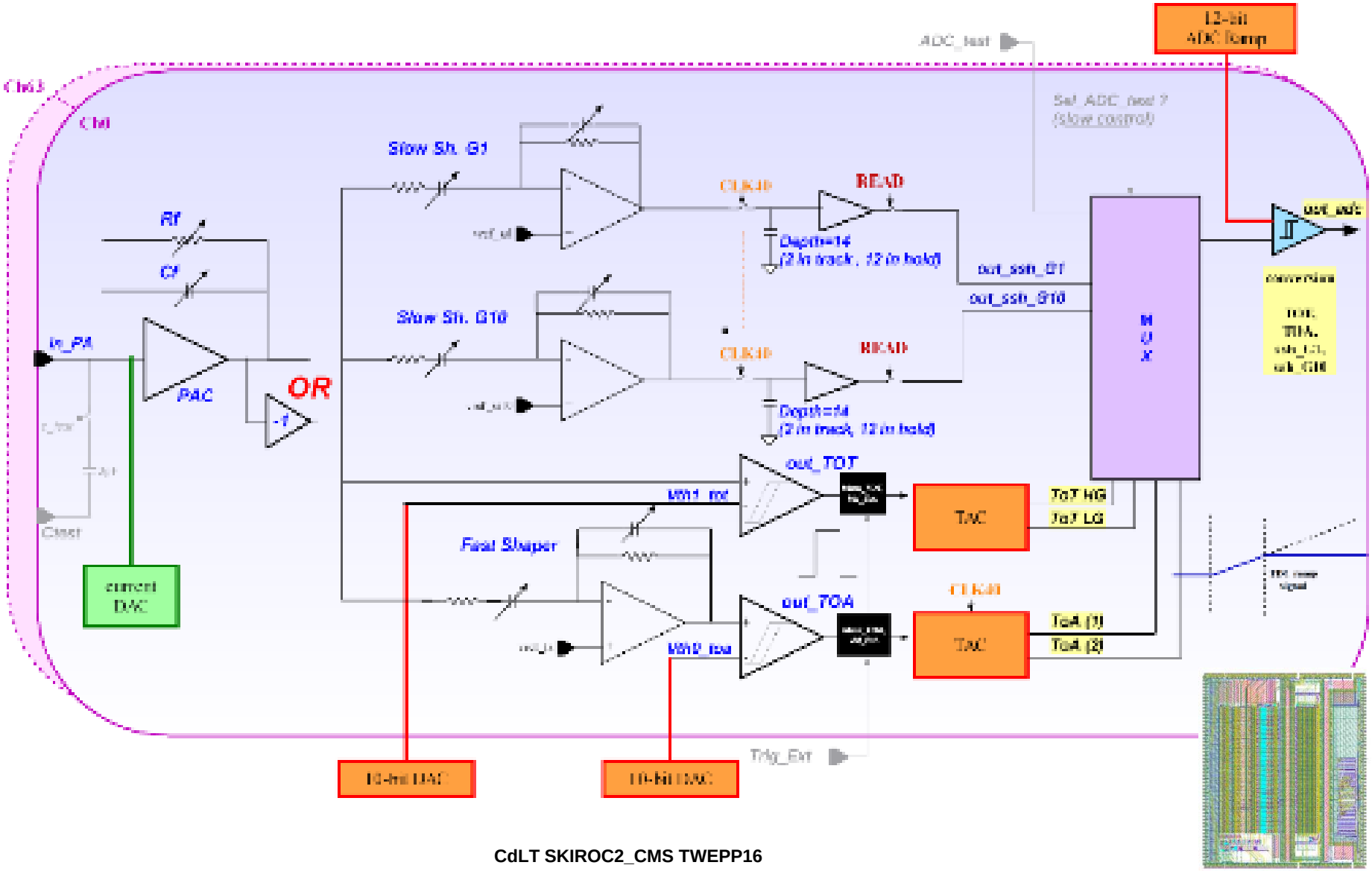






Overview of SK2_CMS

- 64 channels versatile Si calorimeter readout based on CALICE SKIROC2



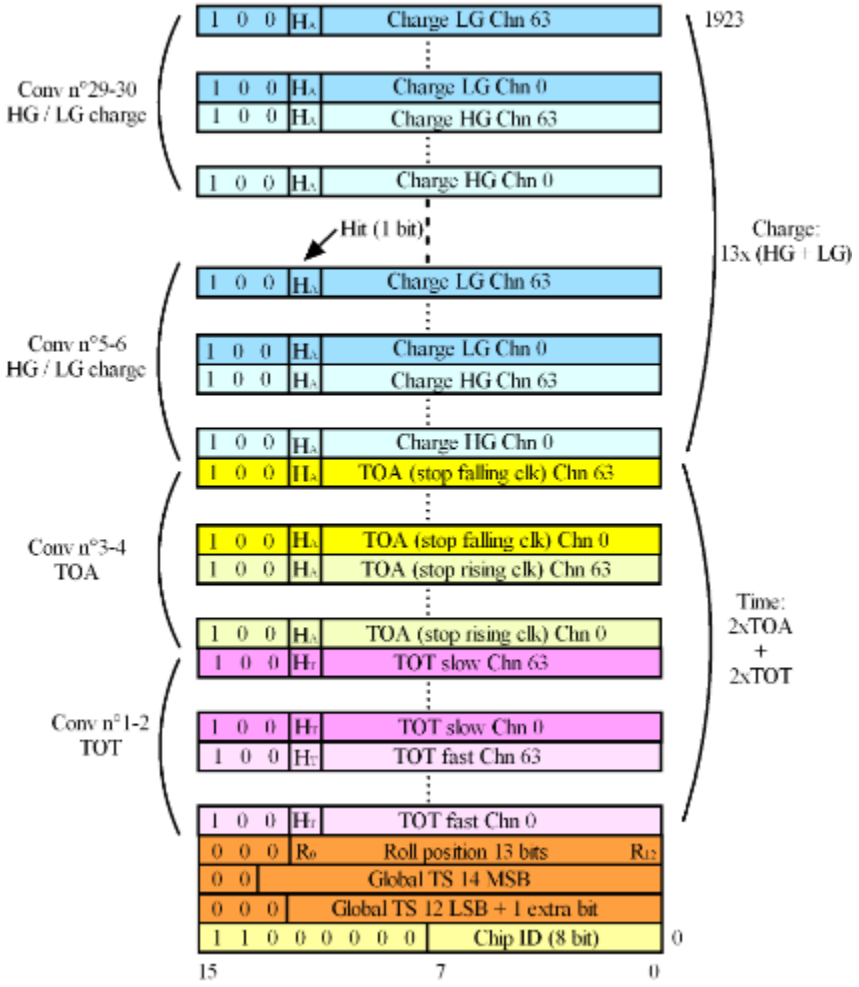
Digital readout scheme

- Based on Calice chips readout scheme

- Roll mode @ 40MHz
- depth 12x25ns=300ns

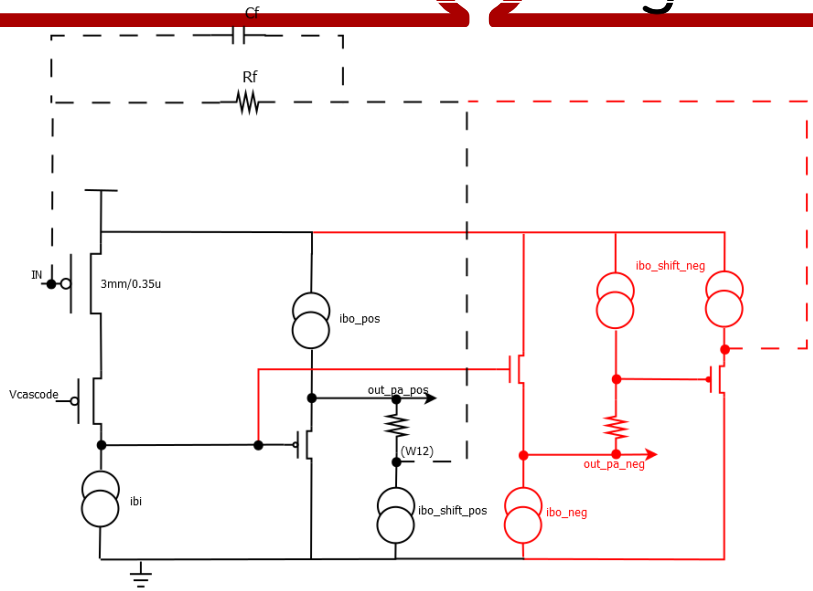
- 12-bit Wilkinson ADC, starts on external Trigger
- 2 ToT (fast & slow); 2 ToA; 2x13 HG & LG Charge
- Duration (worst case)=2^{12} x 25n x 30 = 3 ms

- OC @ 5MHz (SK2) to LVDS @ 40MHz (SK2-CMS)
- Cst. 1924x16x25 = 770µs



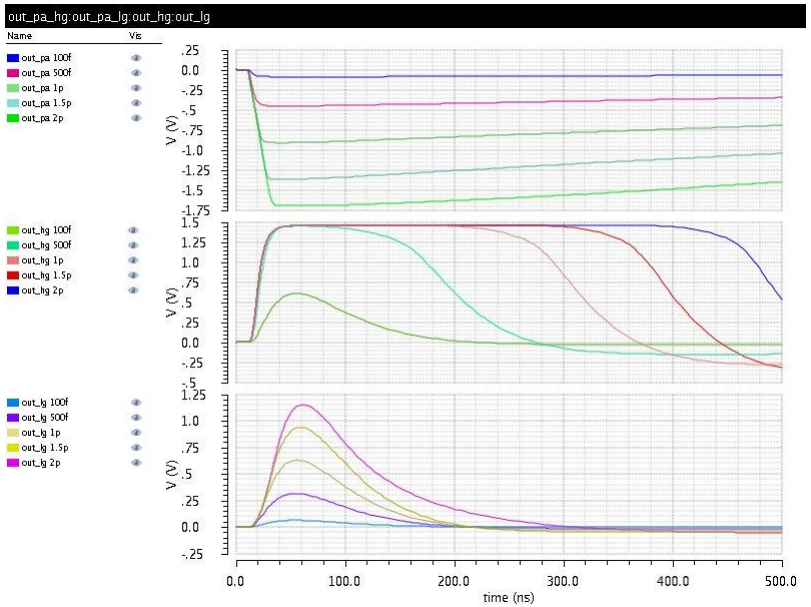
Preamp architecture

- PMOS input Id=1 mA, direct cascode
- Variable Rf 20k-2M, Cf=0.06-4p (4 bits)
- Level shifter for negative polarity

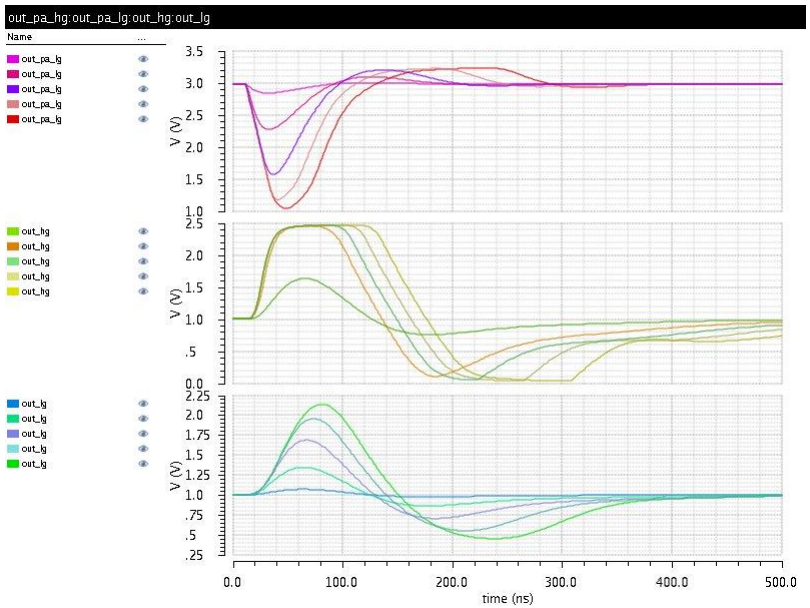


ENC	Rf=1M, Cf=1pF	Rf=20k, Cf=500fF
Positive input	0,2fC (1250 e-)	0,25fC (1560 e-)
Negative input	0,23fC (1440 e-)	0,3fC (1875 e-)

Preamp: Rf=1M, Cf=1pF

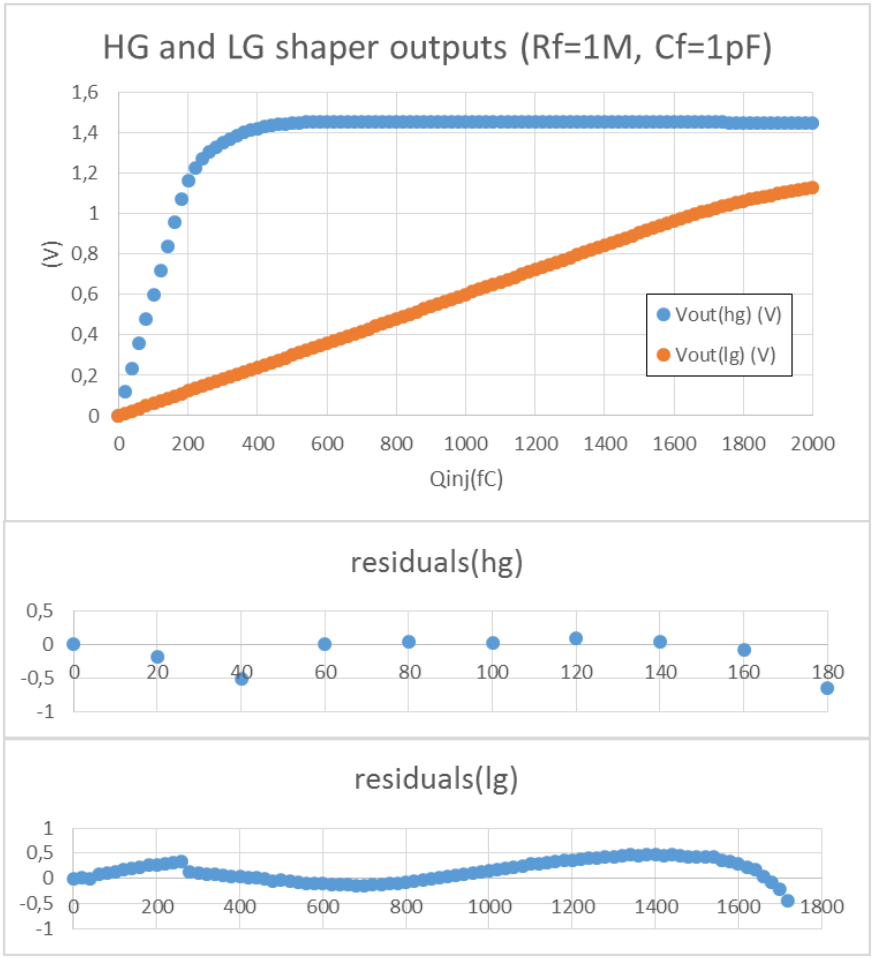


Preamp: Rf=20k, Cf=500fF



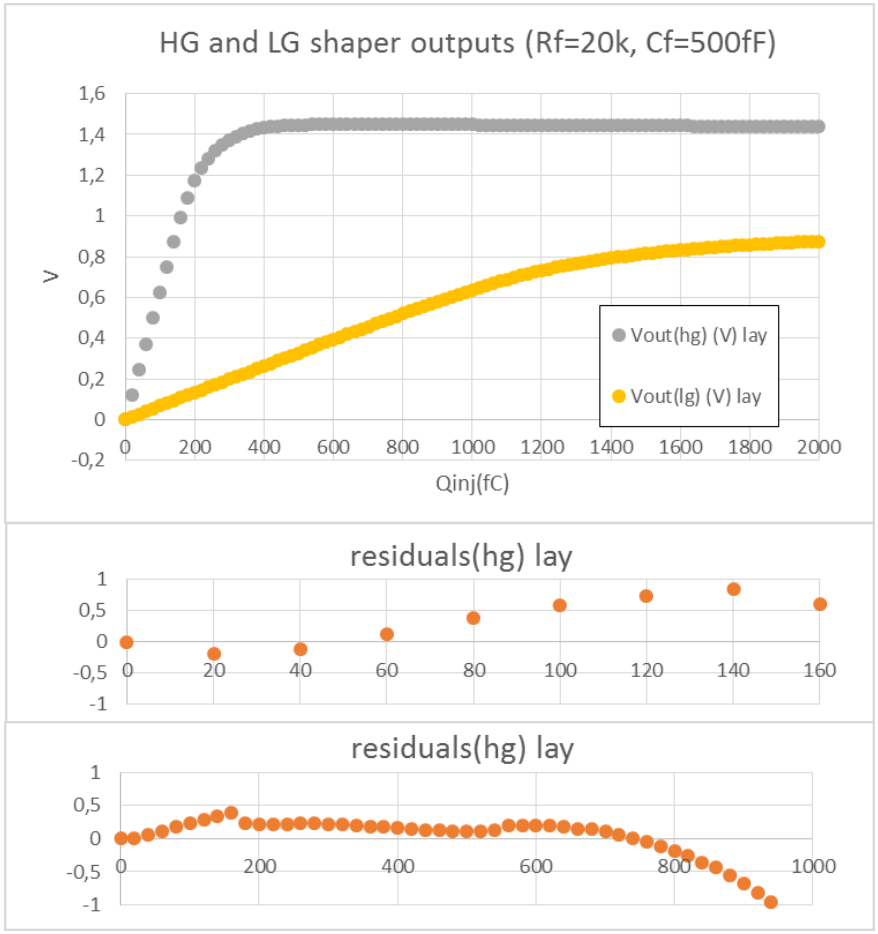
Positive input: HG and LG linearity post-layout simulations

Preamp: Rf=1M, Cf=1pF



- HG linearity: from 0 to 180 fC
- LG linearity: from 0 to 1700 fC

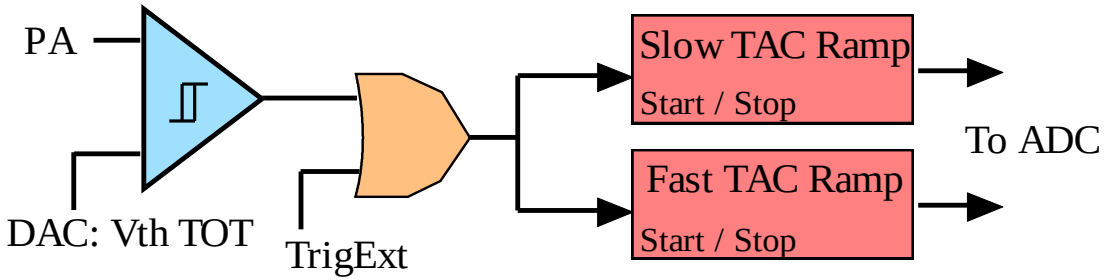
Preamp: Rf=20k, Cf=500fF

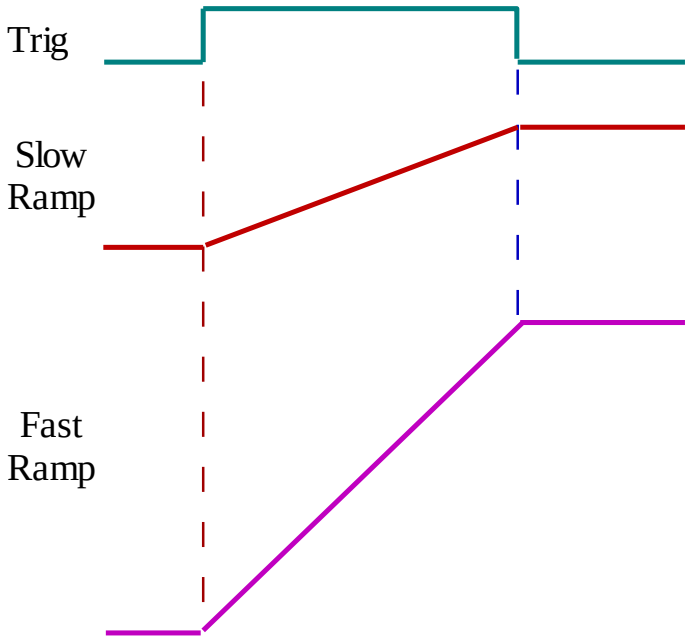


- HG linearity: from 0 to 160 fC
- LG linearity: from 0 to 950 fC

Time over Threshold principle (TOT)

- TOT based on a Time to Amplitude Converter (TAC):
  - 2 analog ramp / channel
  - Slow ramp to validate TOT mode (~0-500 ns)
  - Fast ramp to characterize non-linear region (~0-50 ns)
  - 1 global TrigExt available to calibrate TOT



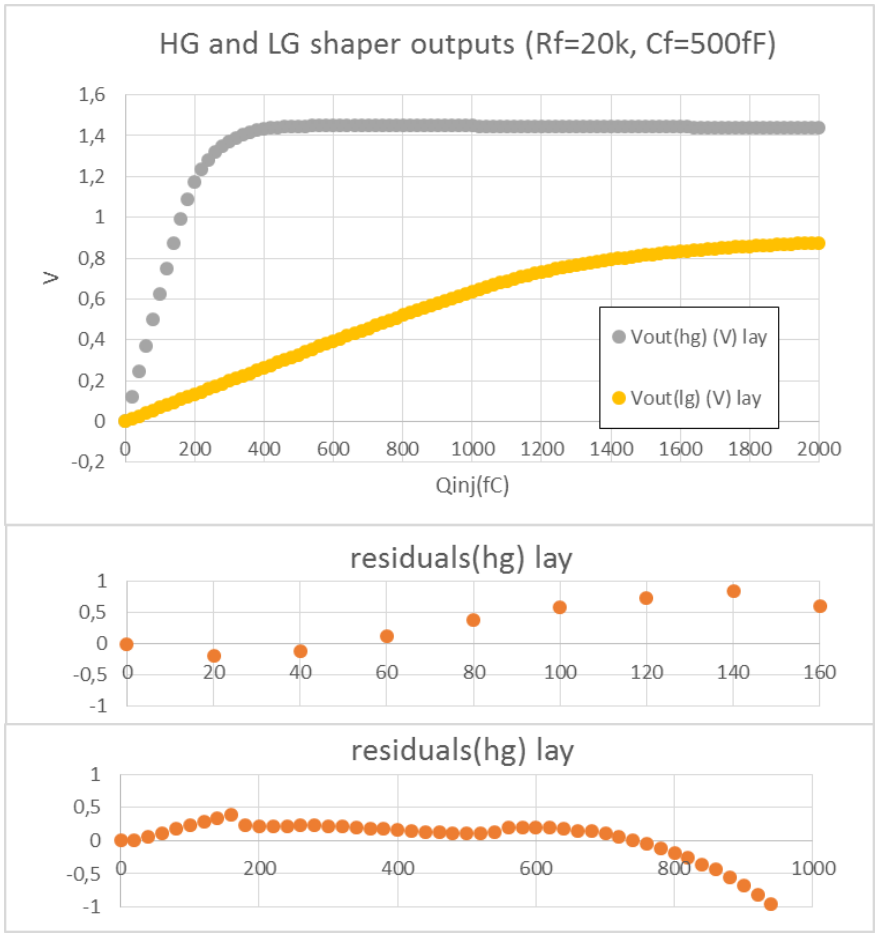


- Channel with TOT data are marked with Hit bit
- Relevant data in memory mapping:
  - Digitized TAC ramp (fast / slow)
  - Hit bit (H_T)

1 0 0	H_T	TOT slow Chn 0
1 0 0	H_T	TOT fast Chn 0

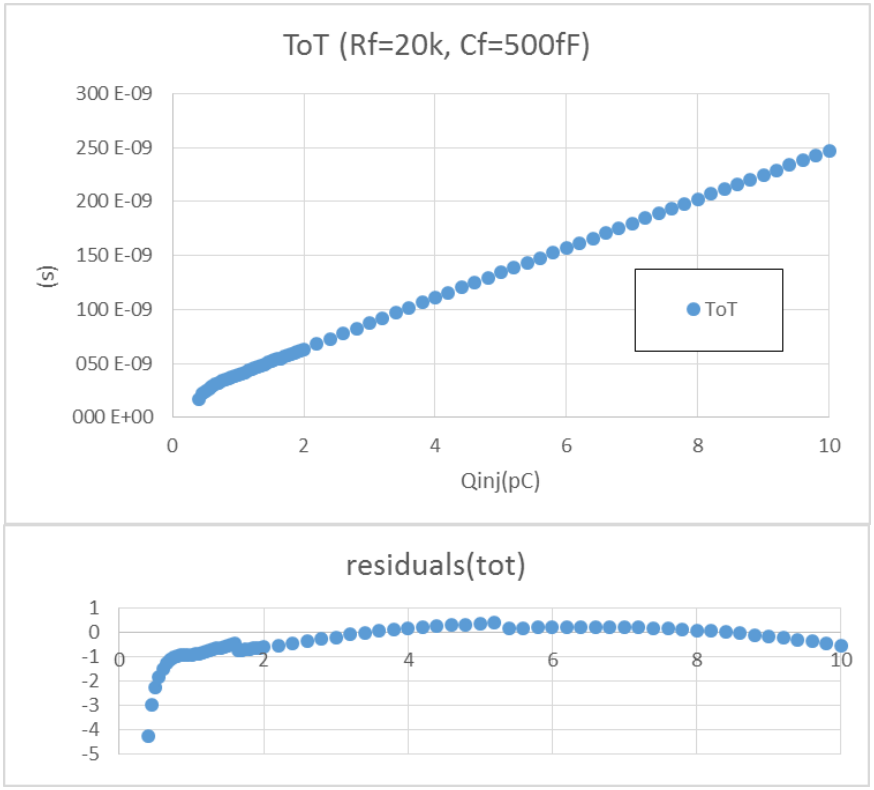
Positive input: ToT post-layout simulations

Preamp: Rf=20k, Cf=500fF



- Threshold @ 700 fC
- ToT linearity: from 800 fC to 10 pC

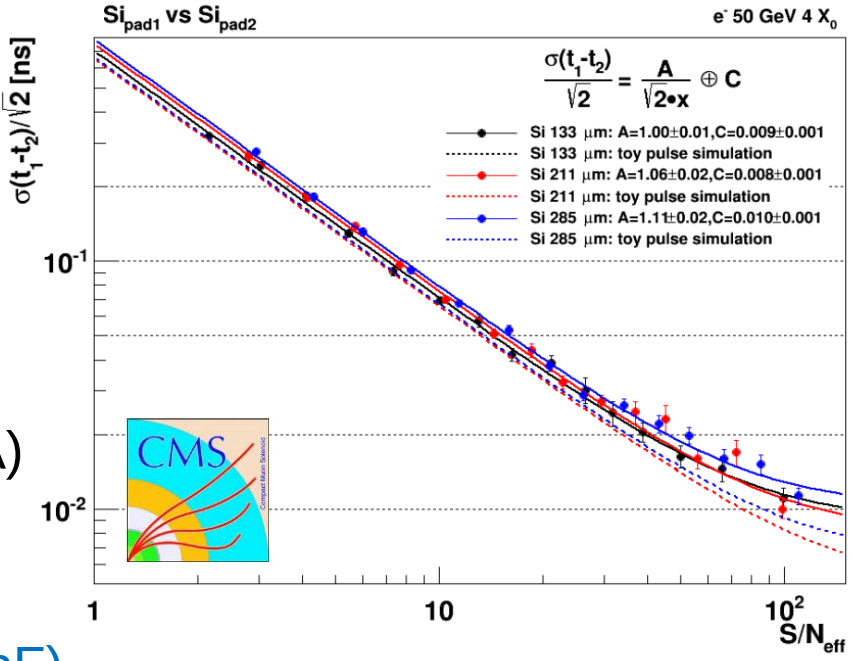
Preamp: Rf=20k, Cf=500fF

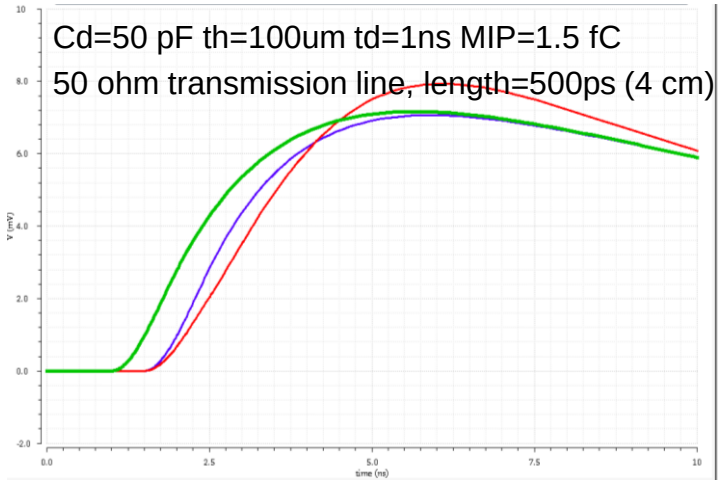


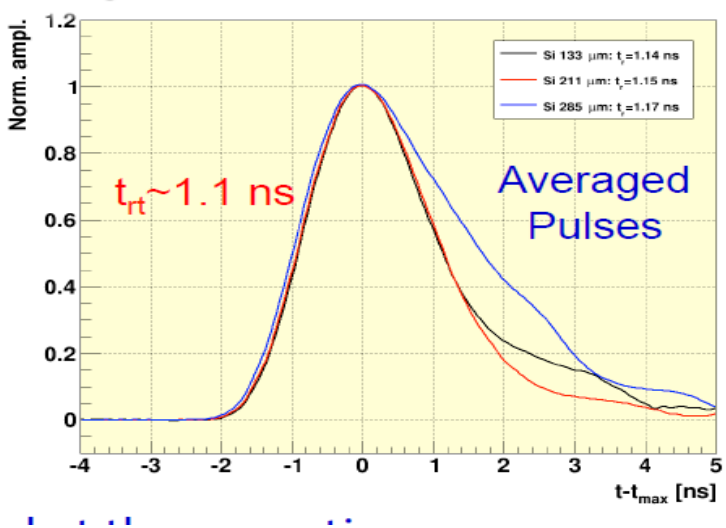
- Threshold @ 450 fC
- ToT linearity: from 1,7 pC to 10 pC

Timing studies

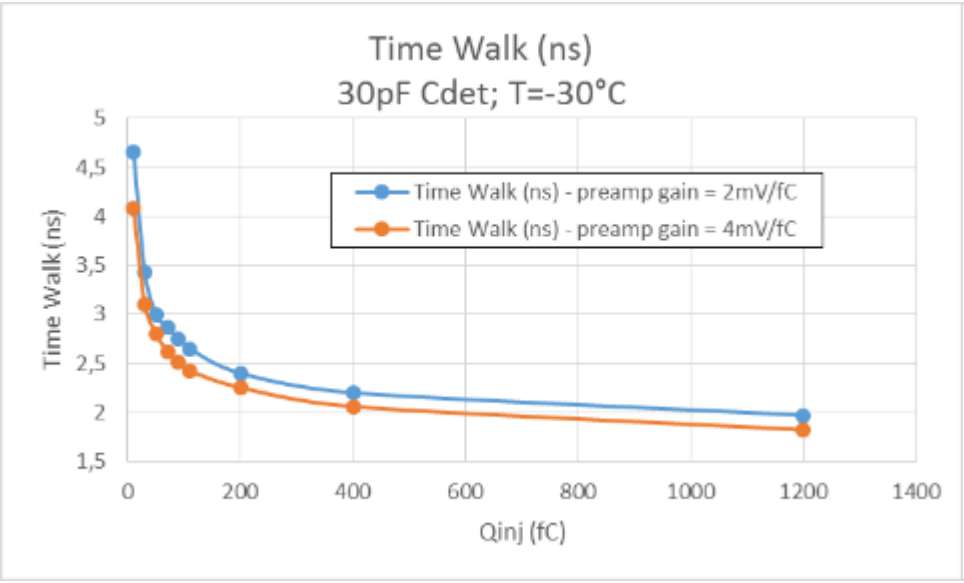
- Timing tests *[M Mannelli et al. ACES2016]*
  - 700ps/(S/N) (+) 20 ps
  - But 2 GHz BB amps
  - 5 Gs/s digitization
- Theory : $\sigma_t^J \approx \alpha . C_d \sqrt{\frac{t_d}{g_m}}$
- But different readout electronics (CSA)
  - Different S/N, Reflections in PCB ?
  - Time walk corrections
- Expect ~ 3-4 ns/fC (+) 50 ps (Cd=50pF)

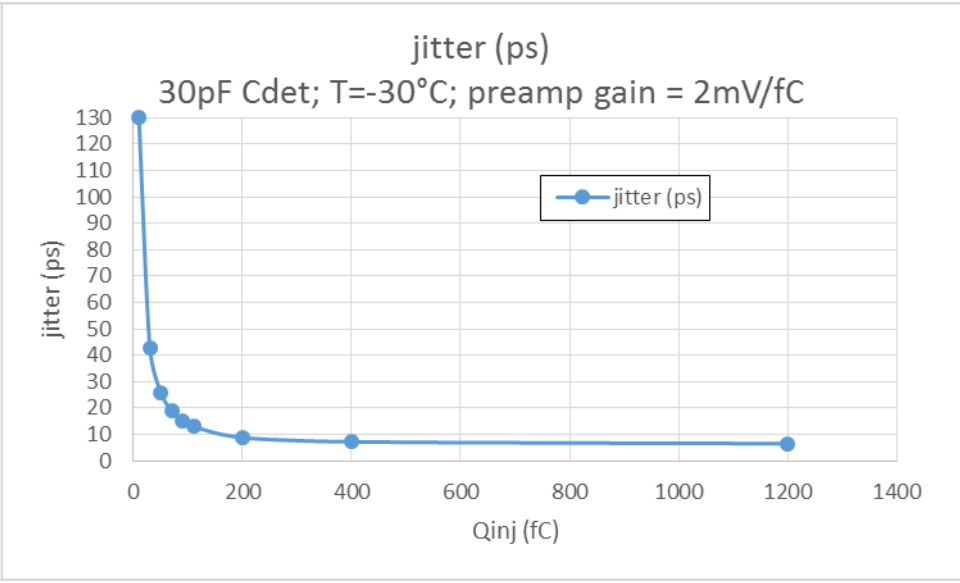


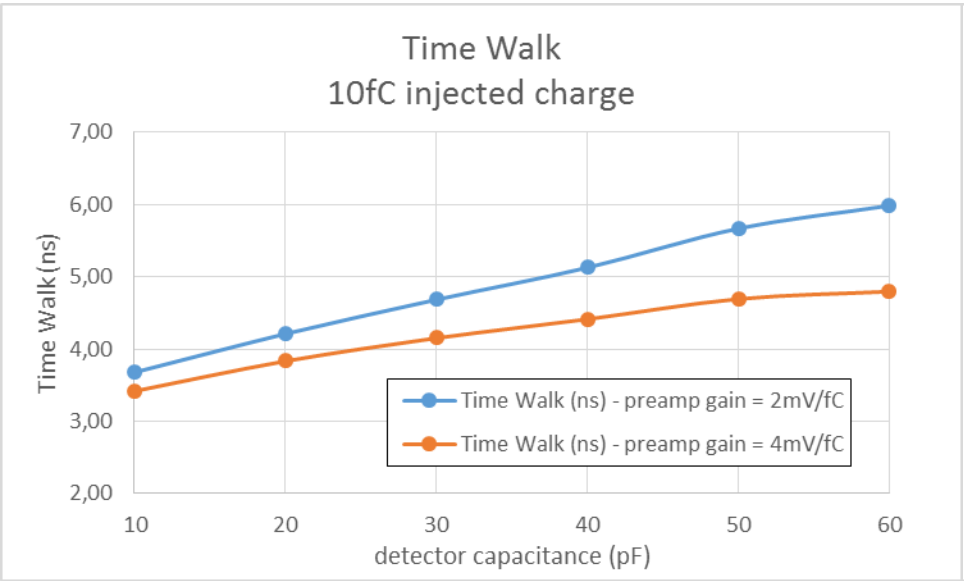


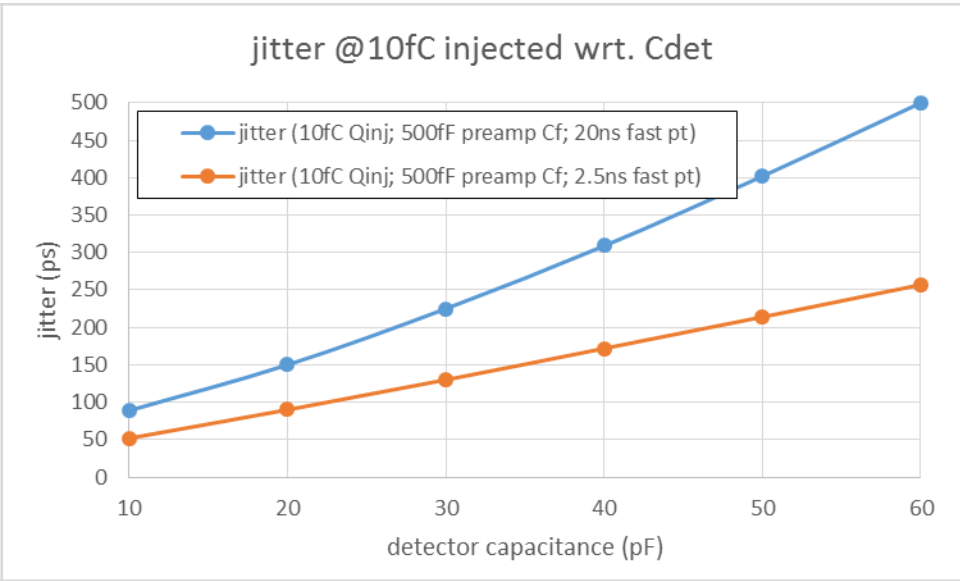


Some time performance simulations



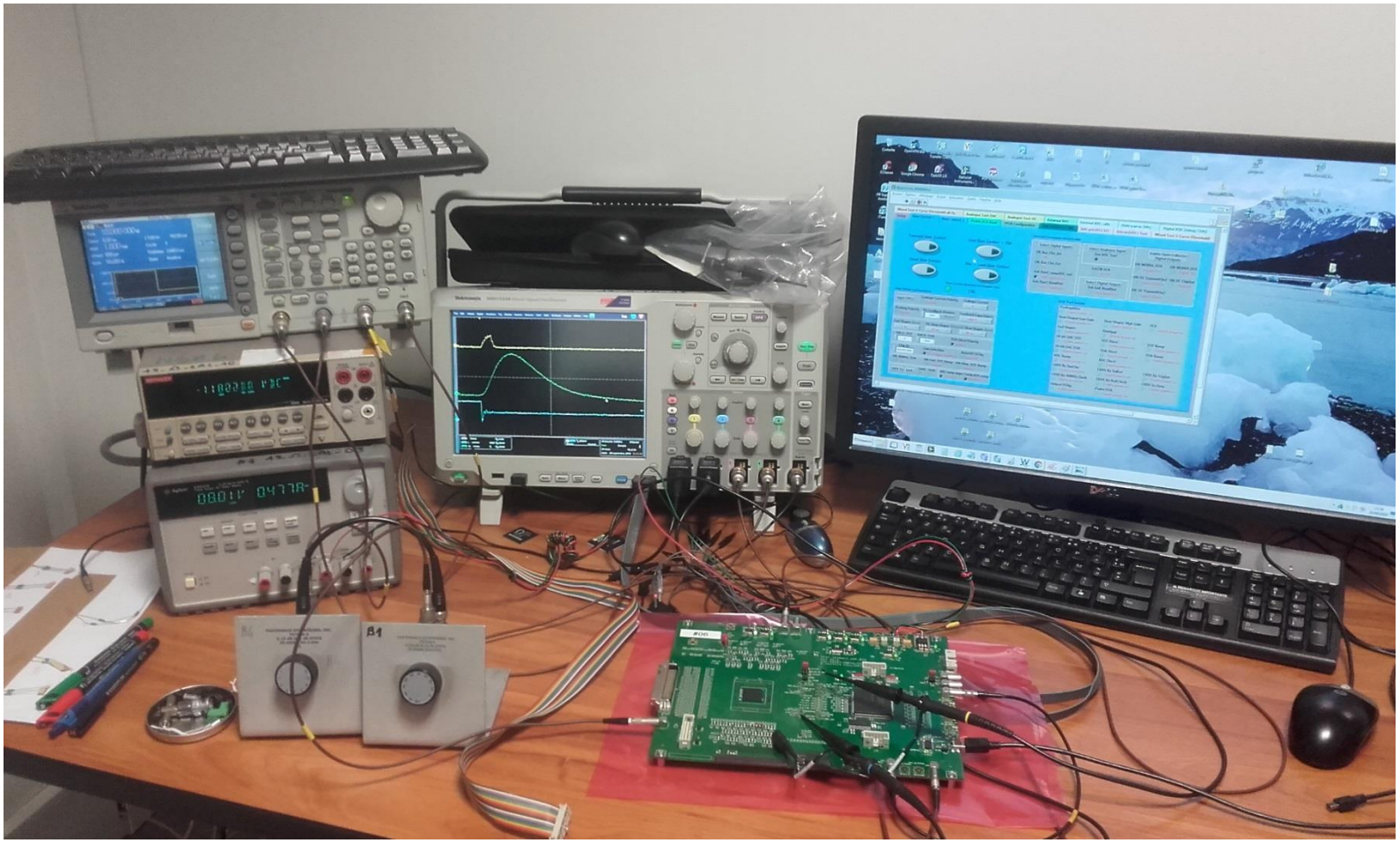






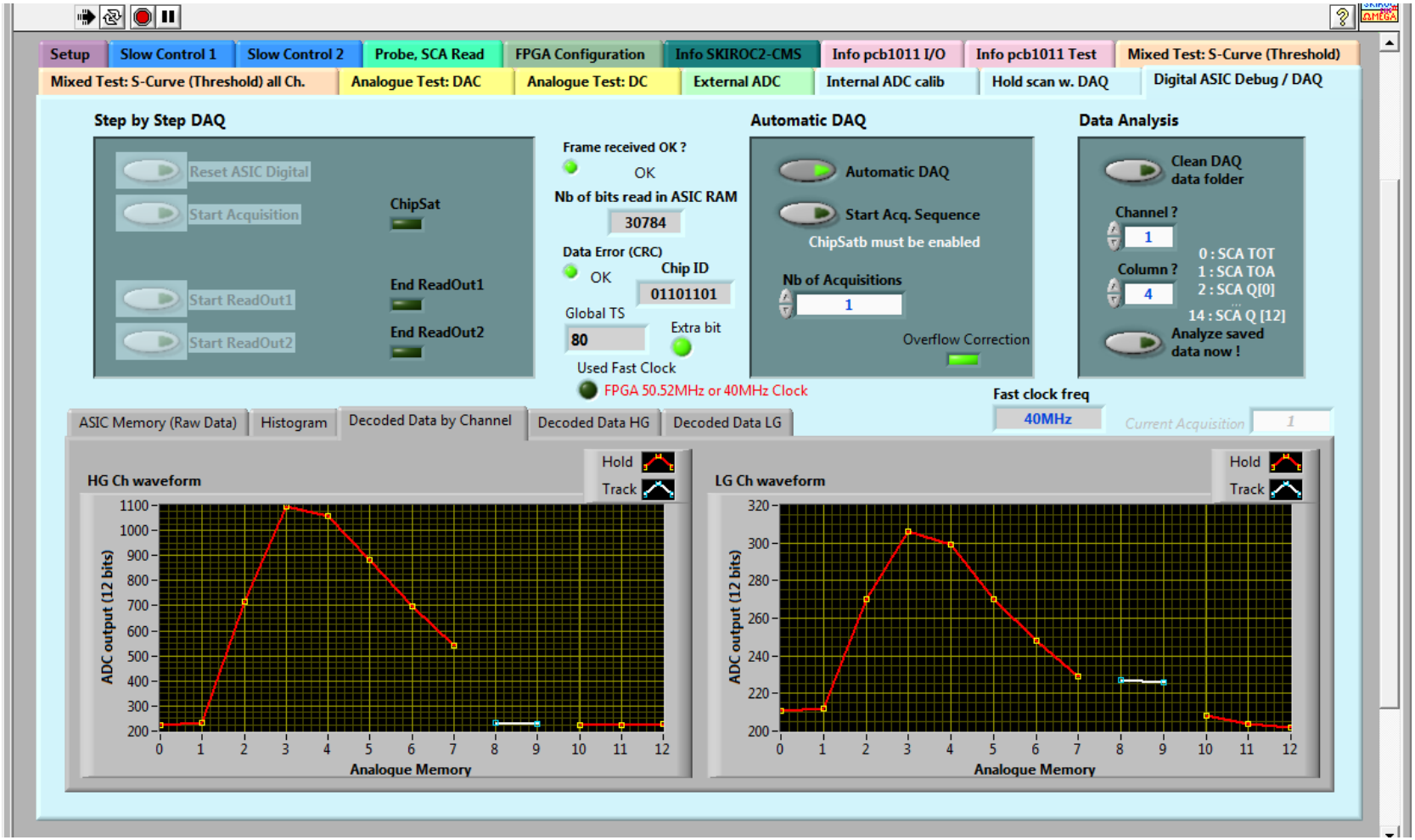
Experimental measurements

- Chips packaged in BGA for testboards
- Tests carried out at Imperial College, Univ Split and OMEGA



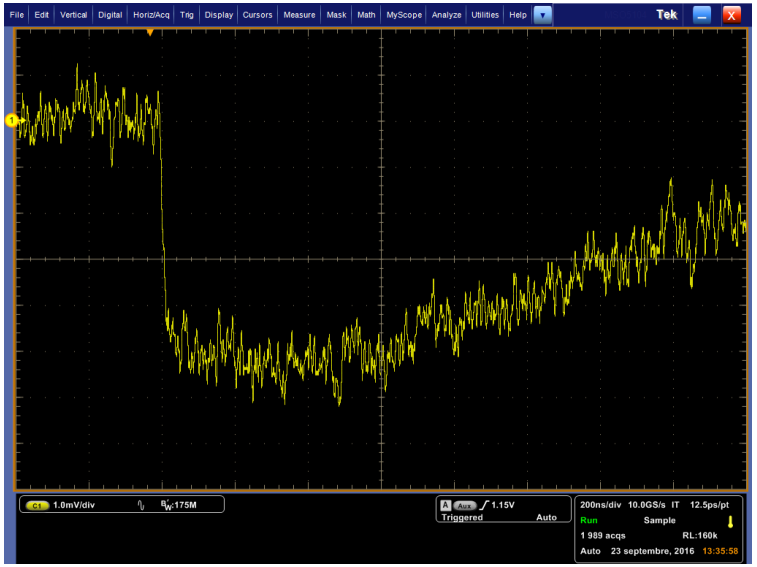
SCA operation

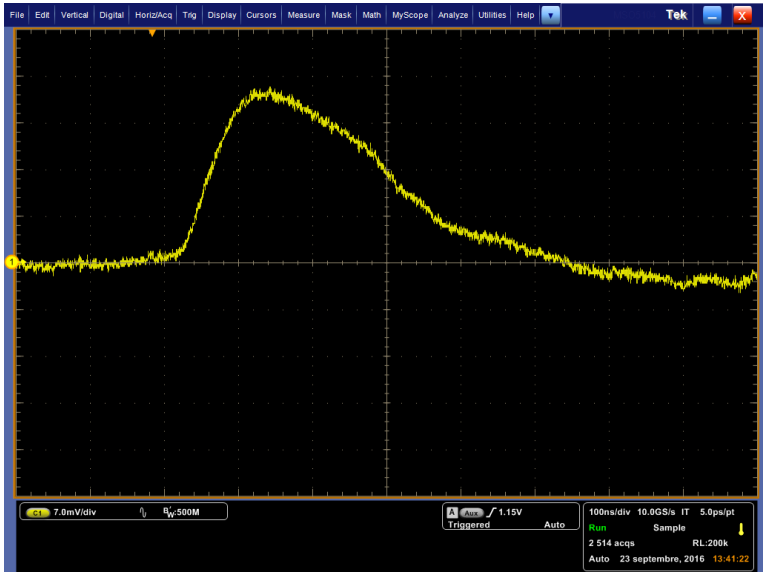
- 40 MHz circular analog memory. 13 cells in store and 2 in track
- Allows ~300 ns trigger latency

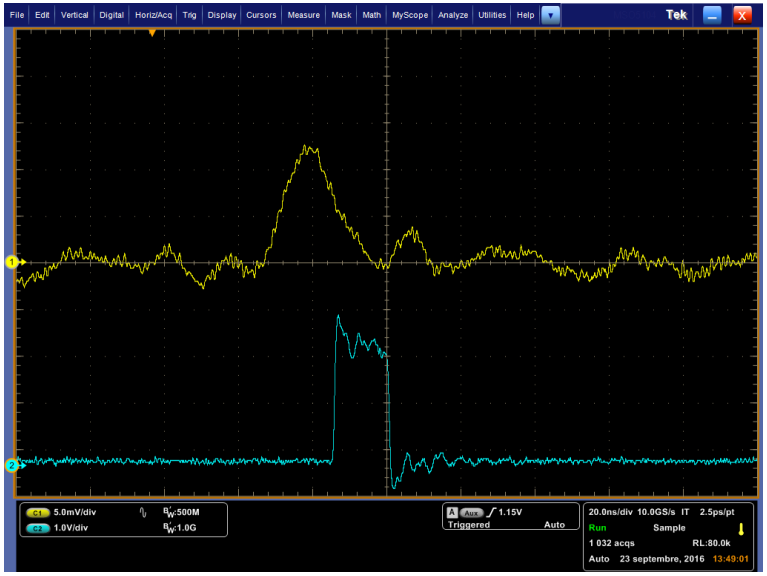


Waveforms with 1 MIP injection

- 3 fC test pulse injection ~1 MIP
- Preamp Cf = 0.5 pF Rf = 2.5MΩ Cd=0
  - Vout = 5 mV N = 0.4 mV
- HG shaper tau = 20 ns
  - Vout = 15 mV N = 1.2 mV
- Fast shaper tau = 5 ns
  - Vout = 12 mV N = 1.4 mV







Reconstructed waveforms CSA config

- Charge sensitive configuration : Rf = 2.5 MΩ Cf = 0.5pF
- Hi Gain / Lo Gain positive/negative configurations

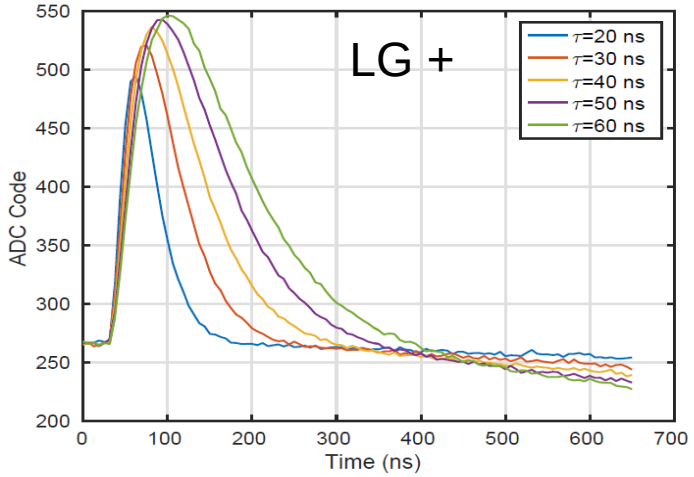
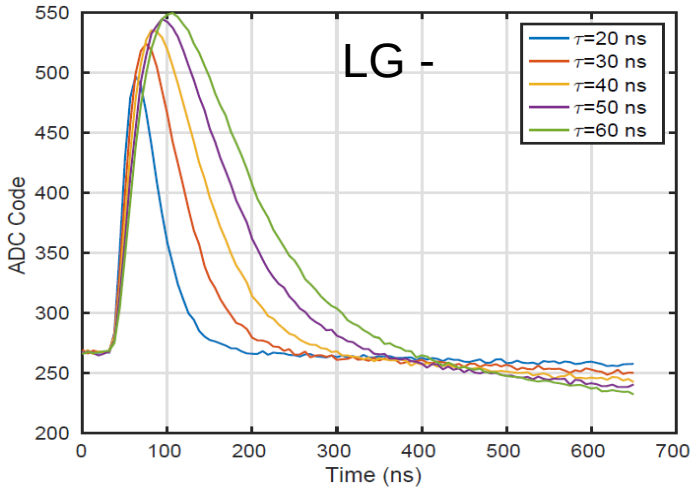


Figure 29: Shaper response for different tau, Low-gain, positive polarity



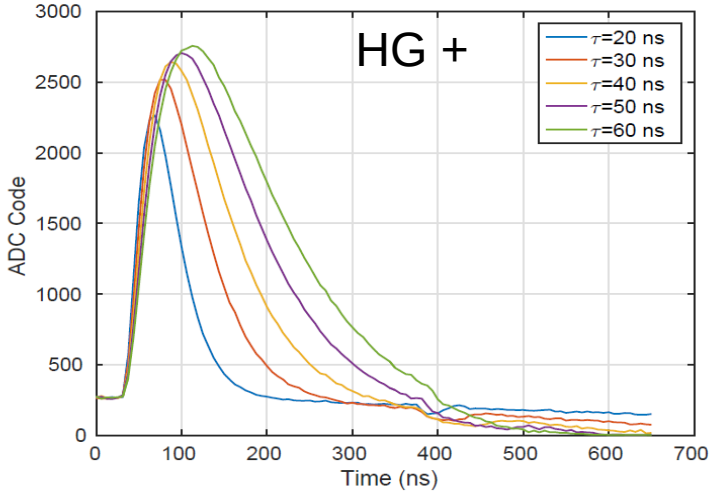


Figure 30: Shaper response for different tau, High-gain, positive polarity

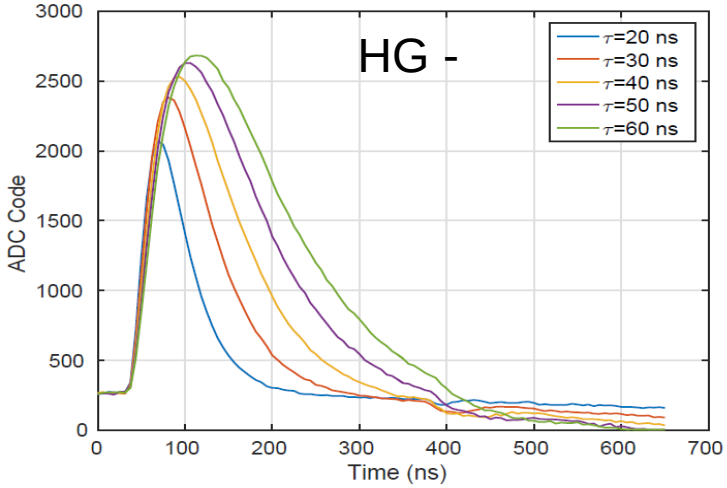


Figure 32: Shaper response for different tau, High-gain, negative polarity

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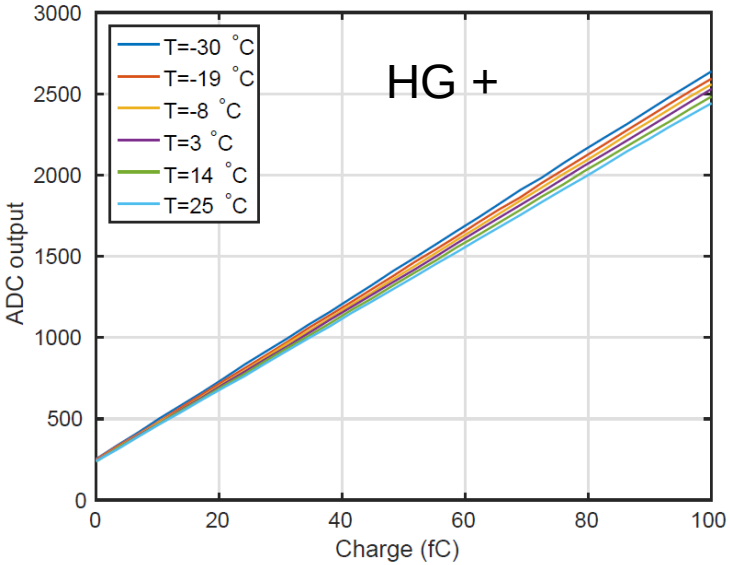
Linearity

- Linearity < 1%, temperature sensitivity ~0.1%/K



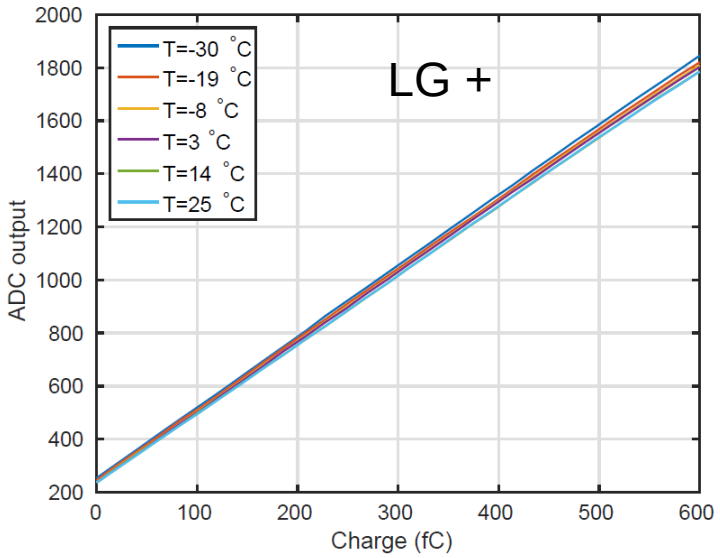
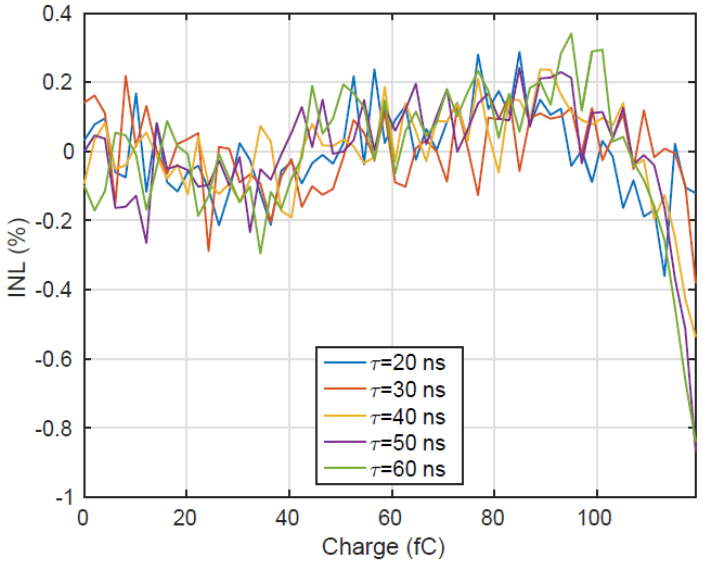
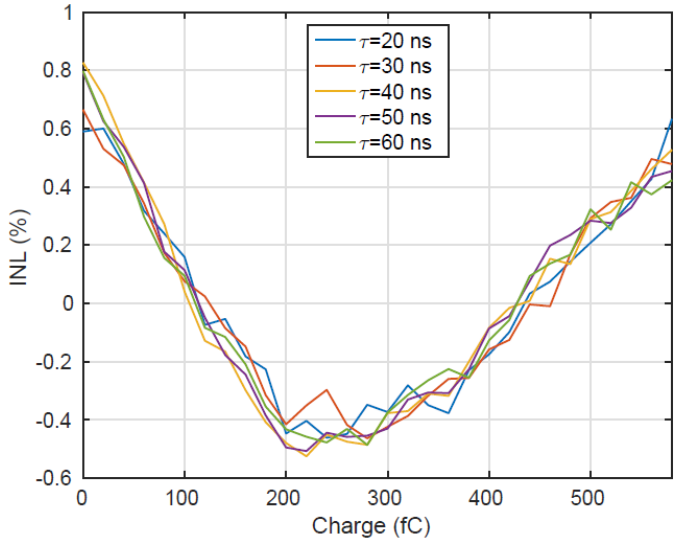


Figure 3: High-gain transfer function for different T, positive polarity, $\tau = 40ns$

Fig ns





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Uniformity, temperature stability

- Dispersion ~0.5% rms stability : 0.1%/K

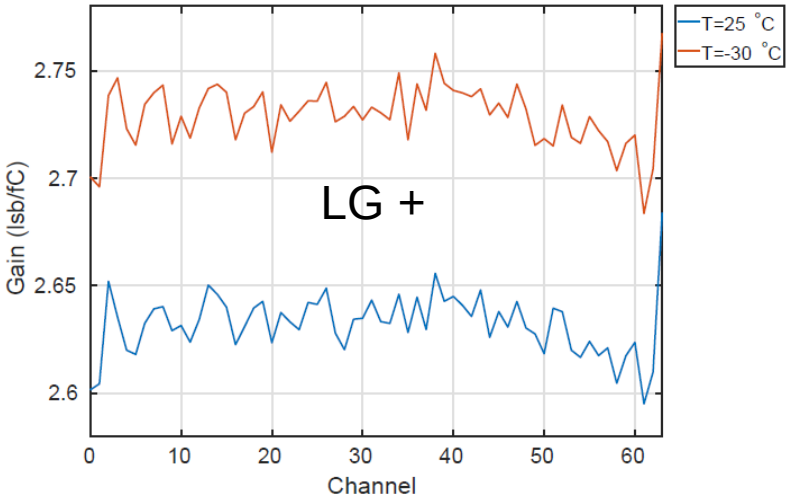

Figure 1: Low-gain gain of each channel, σ_{25}=0.014 (lsb/fC), σ_{-30}=0.014 (lsb/fC)

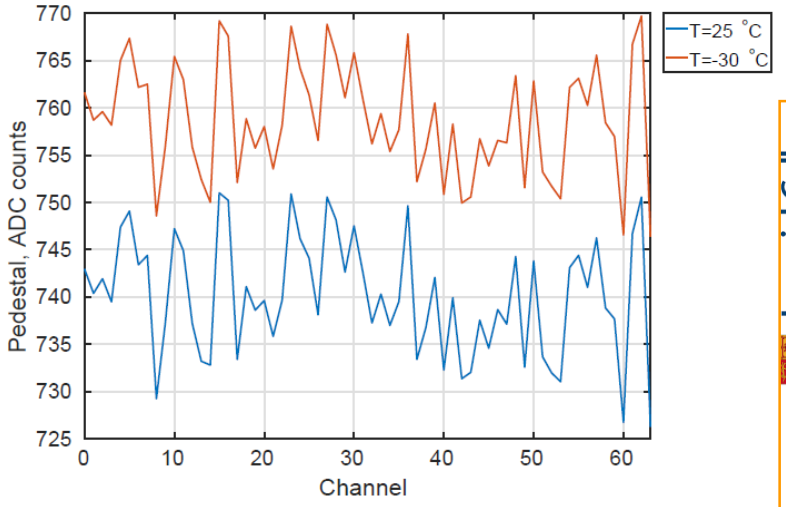

Figure 2: Low-gain pedestal of each channel in ADC units, σ_{25}=6.3 (lsb), σ_{-30}=6.0 (lsb)

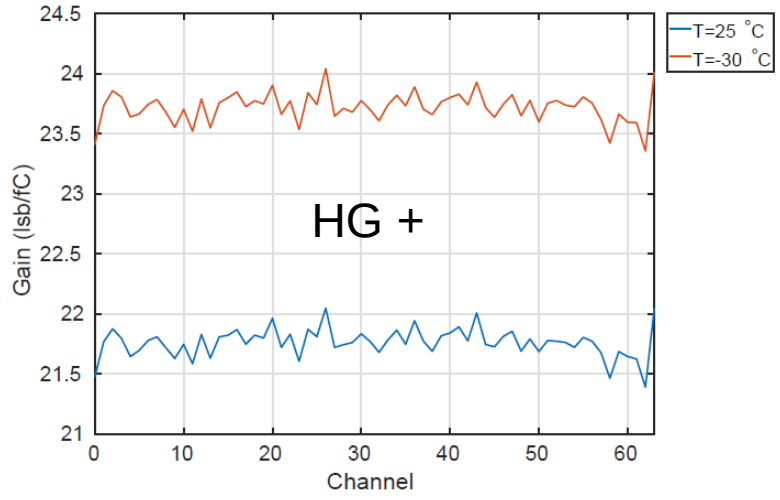

Figure 4: High-gain gain of each channel, σ_{25}=0.120 (lsb/fC), σ_{-30}=0.126 (lsb/fC)

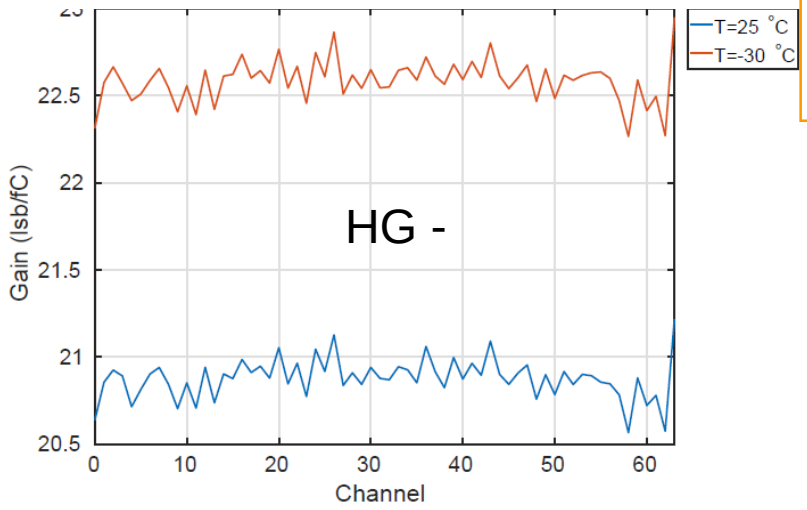

Figure 16: High-gain gain of each channel, σ_{25}=0.116 (lsb/fC), σ_{-30}=0.122 (lsb/fC)

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Noise

- Cd = 47 pF, positive and negative preamps
- Shaping time = 20-60 ns
- ENC = 0.3-0.4 fC = 2000-2500 e-
- Series-noise dominated, slightly worse for negative (as expected)

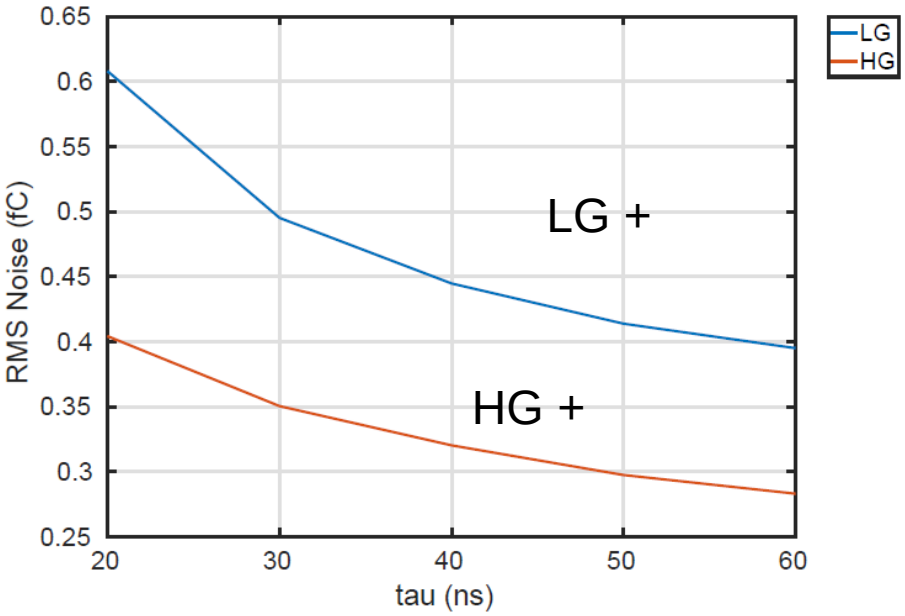

Figure 17: Noise vs shaper setting scaled based on Fig. 5

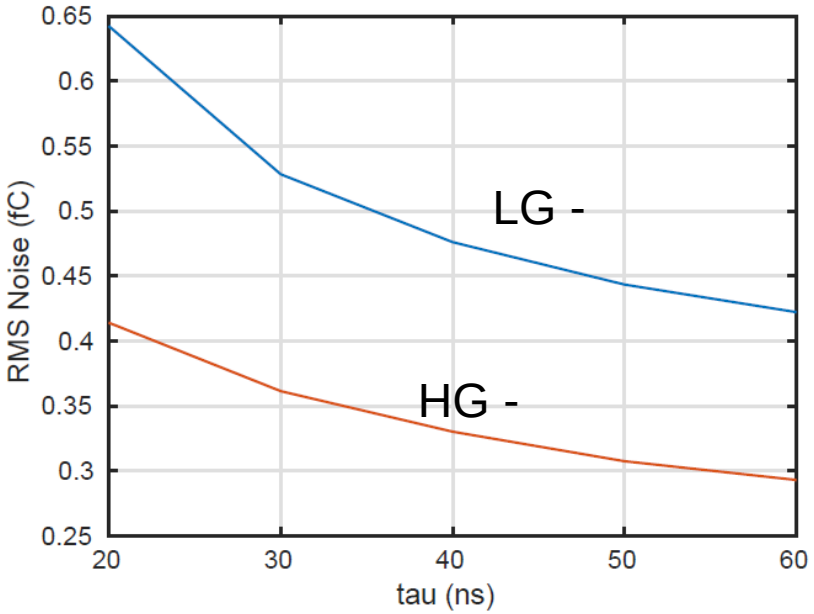

Figure 27: Noise vs shaper setting scaled based on Fig. 11

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Noise vs capacitance

- Linear fit of series noise gives e_n = 1.0 nV/√Hz
- Parasitic capacitance : Ca = 34 pF (10 pF chip 20 pF board)

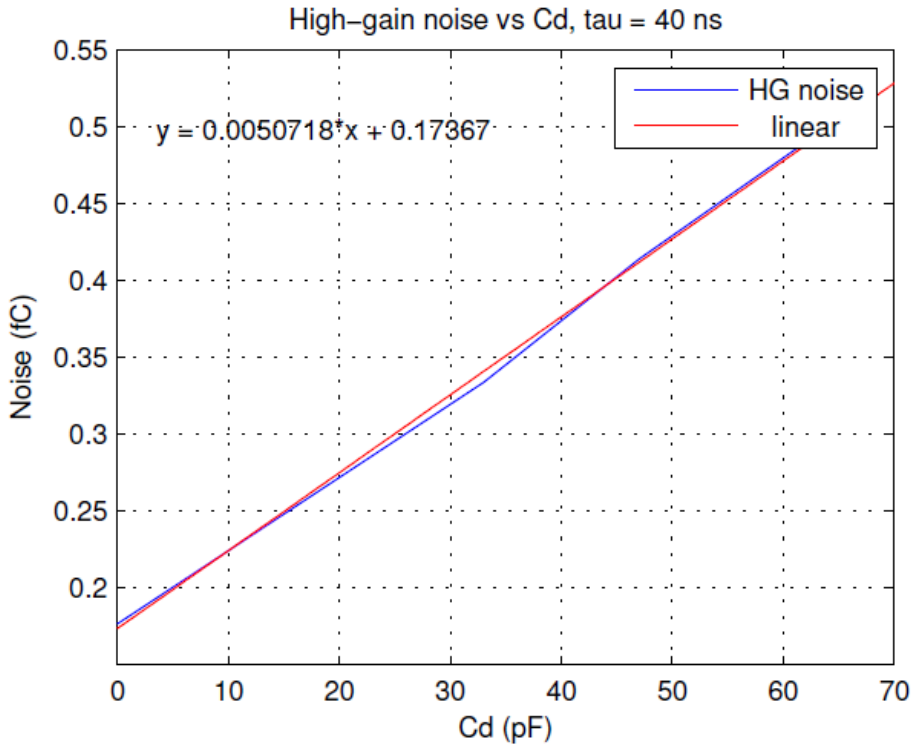


Figure 8: High-gain noise vs Cd, positive polarity, $\tau = 40$ ns. Least-squares linear fit: $y = 0.17367 + 50.718 \times 10^{-3}x$ (fC, pF), $y = 0$ yields $C = 34$ pF.

© D. Coko, T. Sculac U. Split

Noise autocorrelation function

- Series noise dominated at fast shaping
- Significant supply noise at slow shaping
- Removed with additionnal v_{DDA} filtering

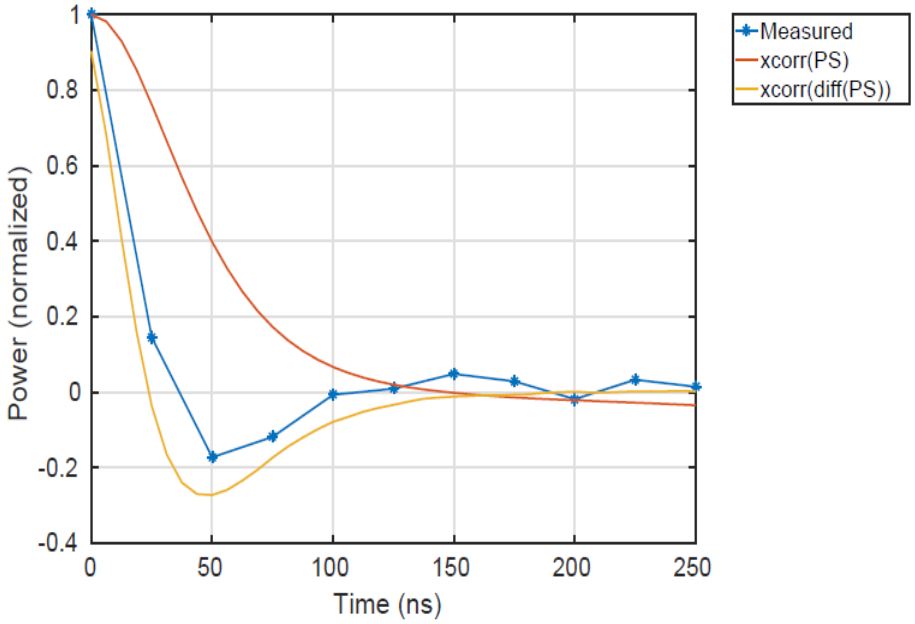
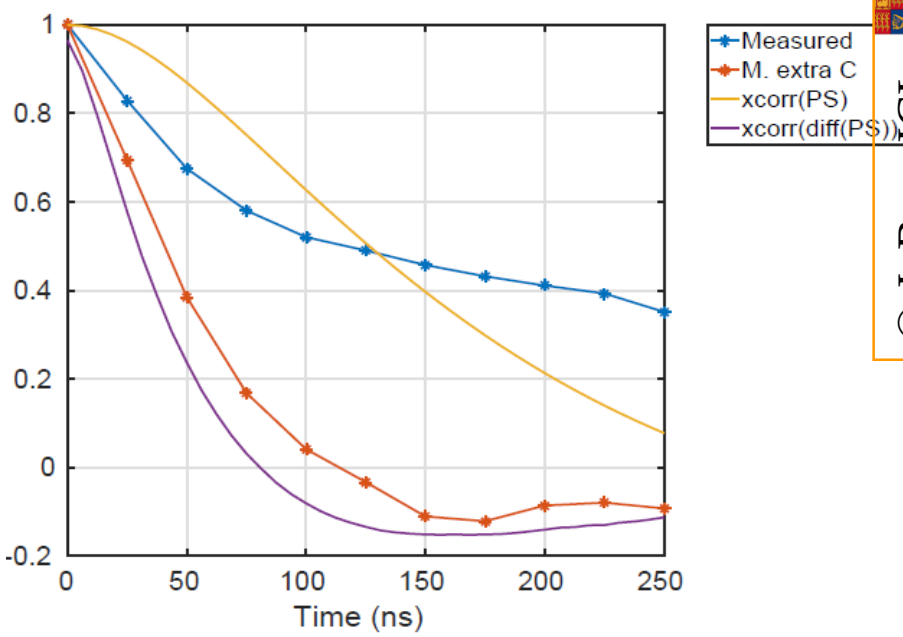


Figure 3: Normalized autocorrelation between bins, High-gain, τ=20 ns.



ıre 13: Normalized autocorrelation between bins, High-gain, τ=70 ns.

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Coherent and incoherent noise

- Using direct and alternate sums (DS and AS) on n channels (n=64)
- Incoherent noise IN=AS / √n
- Coherent noise : CN = $\sqrt{DS^2 - AS^2}$ /n
- Cohrent noise fraction : CNF = CN / IN ~10% at fast shaping.
- Measurement after v_{DDA} decoupling

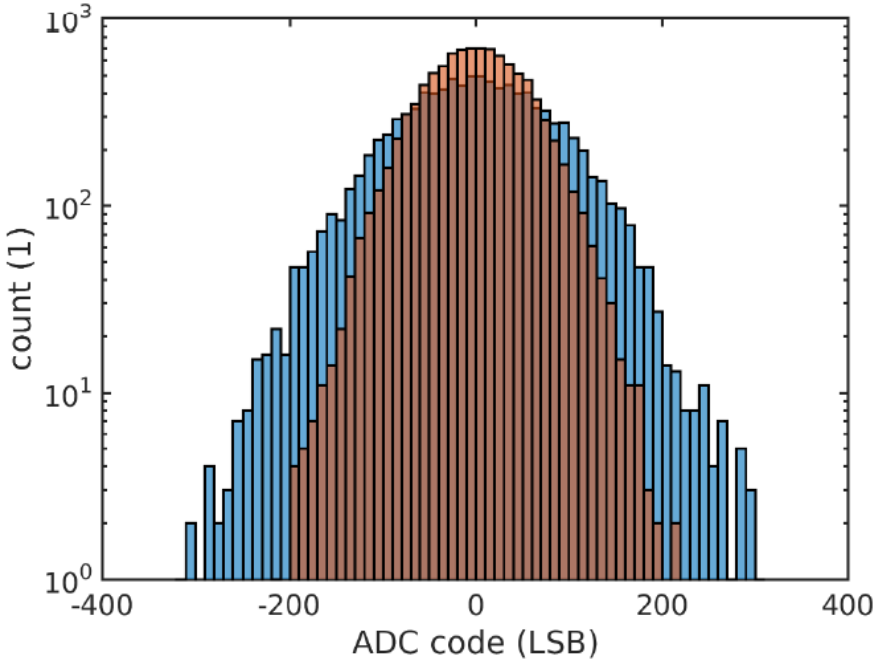

Figure 18: Histogram of direct and alternating sums, τ=40 ns, High gai

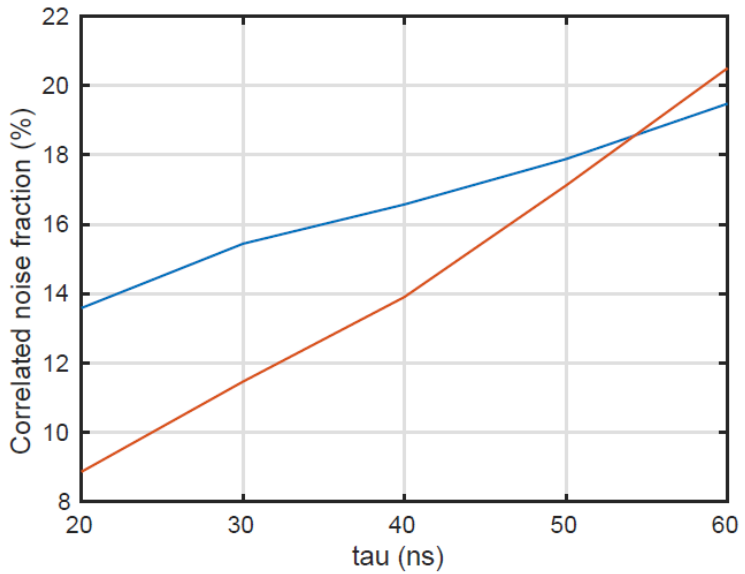

Figure 22: Correlated noise fraction (correlated/white)

Waveforms : ISA configuration

- Current sensitive configuration : Rf = 20 kΩ Cf = 0.5pF
- Hi Gain / Lo Gain positive/negative

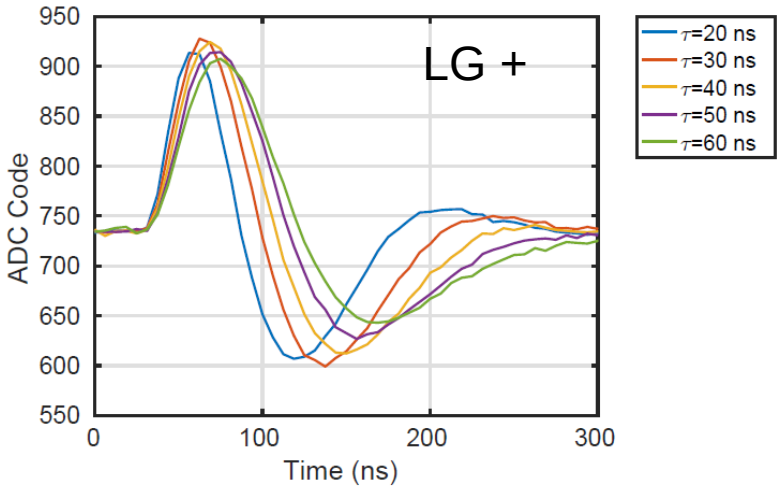

Figure 33: Shaper response for different tau, Low-gain, positive polarity

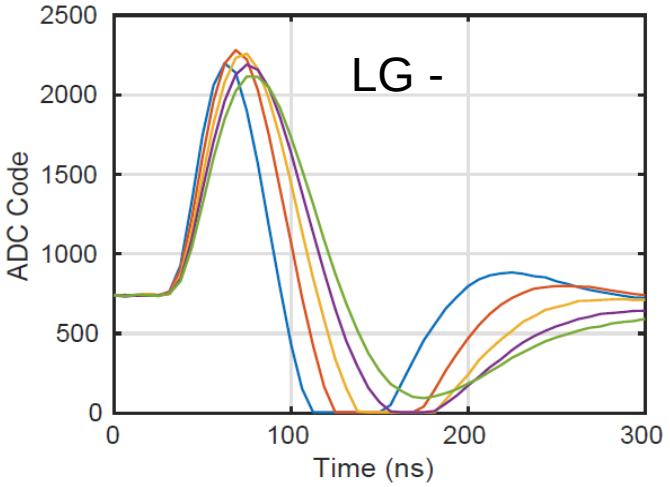

Figure 34: Shaper response for different tau, High-gain, positive polarity

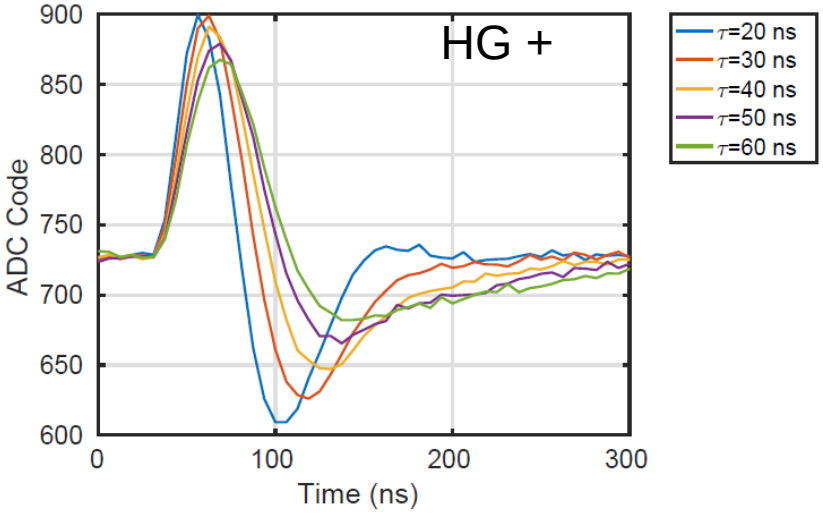

Figure 35: Shaper response for different tau, Low-gain, negative polarity

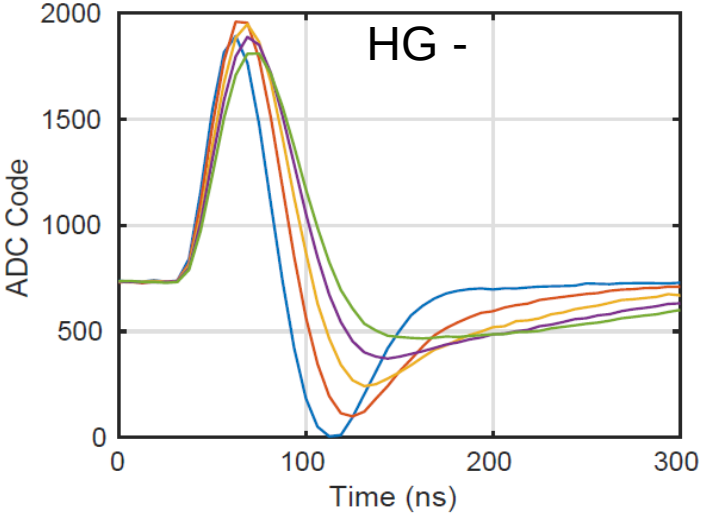

Figure 36: Shaper response for different tau, High-gain, negative polarity

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Trigger senstivity for ToT

- discriminator at preamp output
- Low Threshold 30 fC high threshold 100 fC
- ~ 0.7 DACU / fC
- Dispersion ~5 fC

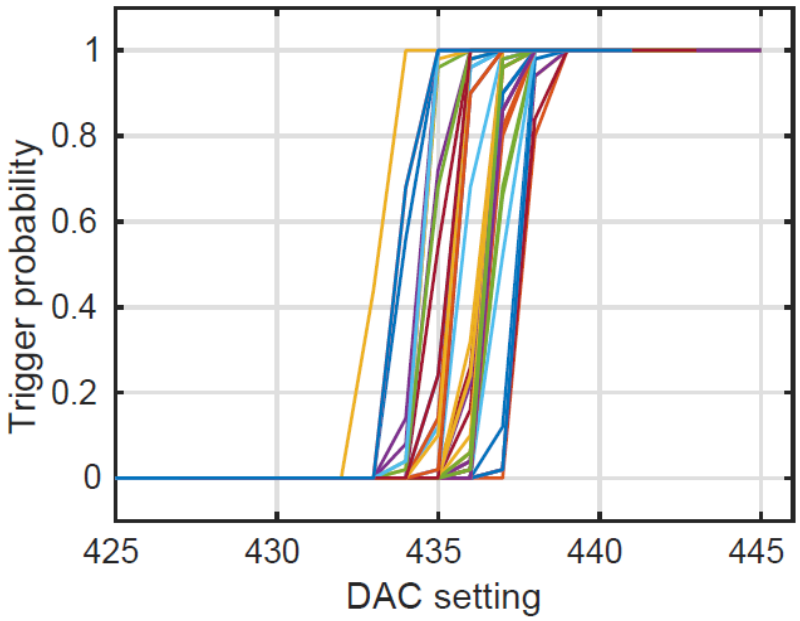

Figure 10: TOT S-curves at 10 fC

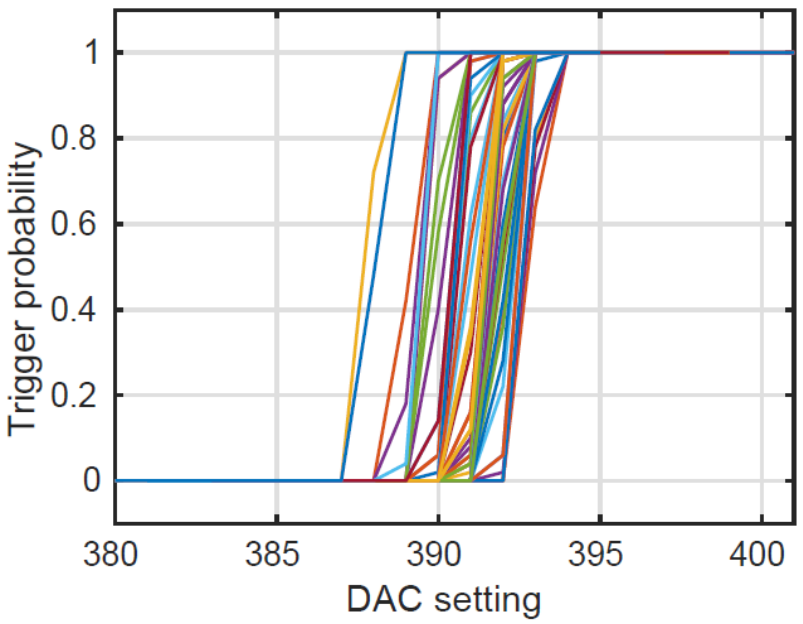

Figure 16: TOT S-curves at 100 fC

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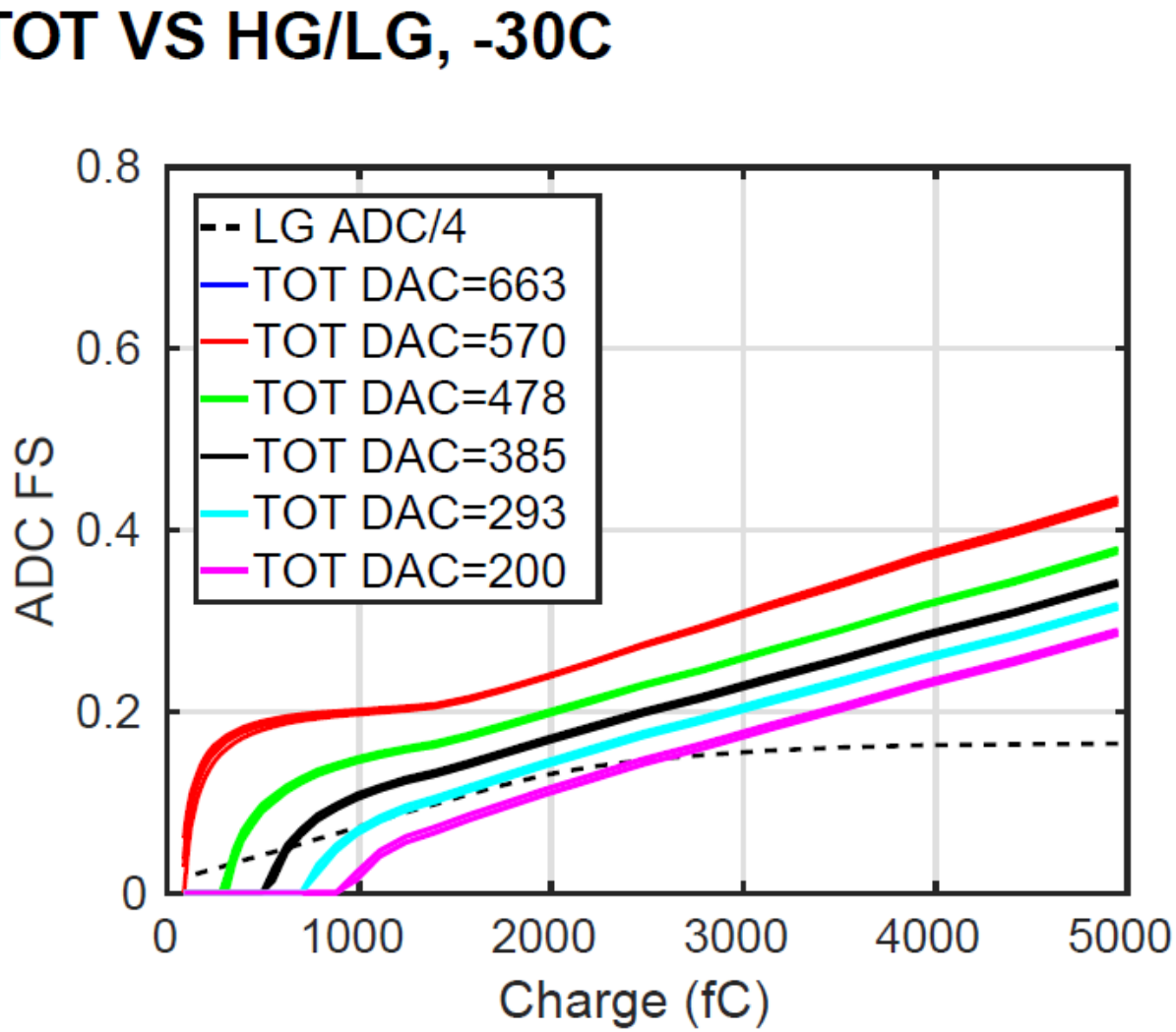
ToT measurements

- TOT measurements starting…



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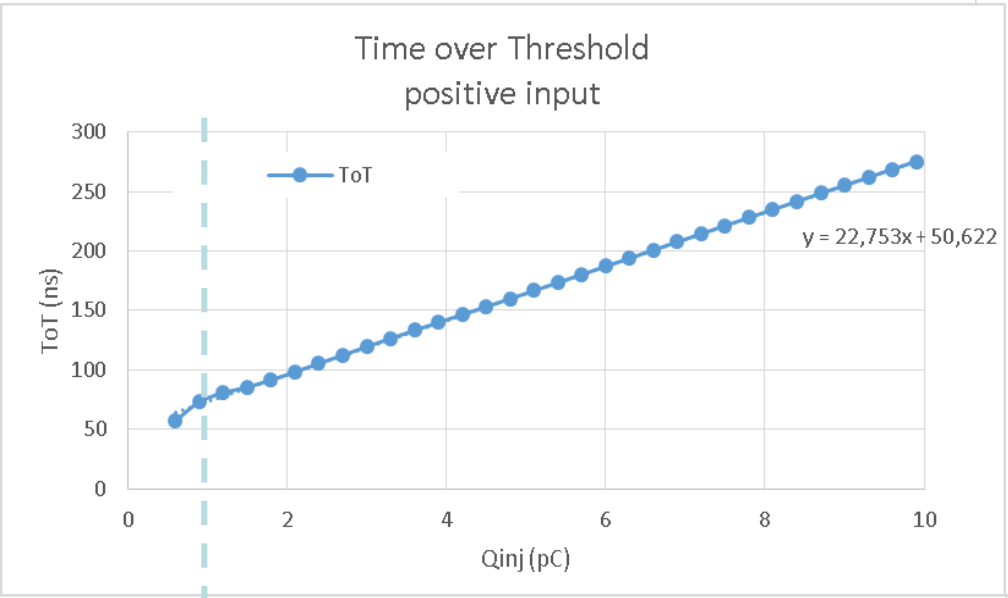
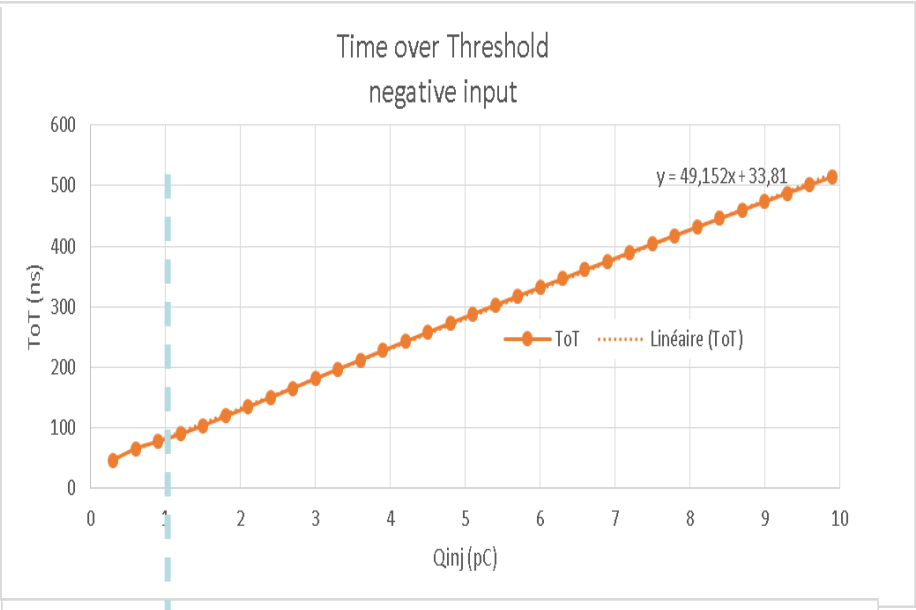
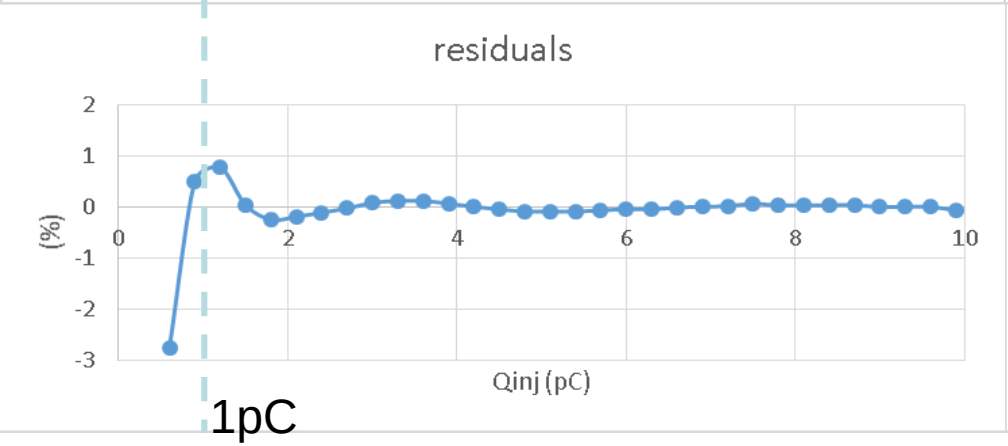
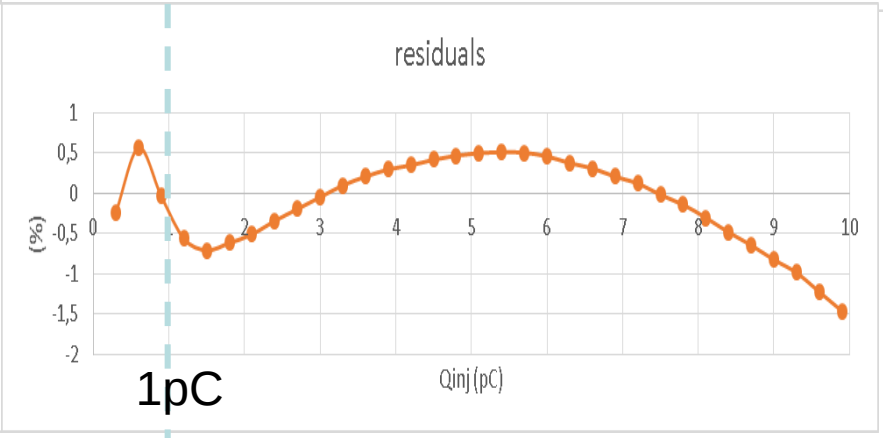
ToT Measurement







1pC



1pC

Low gain Saturation

Low gain Saturation

Trigger senstivity for ToA

- High speed discriminator after fast shaper (4 ns)
- Threshold at 10 fC and 30 fC
- Preliminary timing performance : 270 ps at 30 fC and 57 ps at 300 fC
- Will allow system level studies….

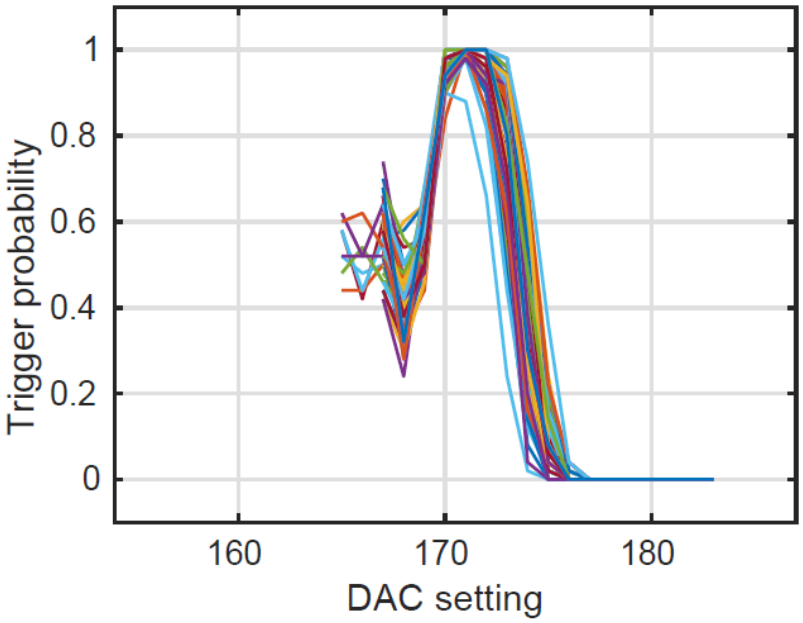


Figure 1: TOA S-curves at 10 fC

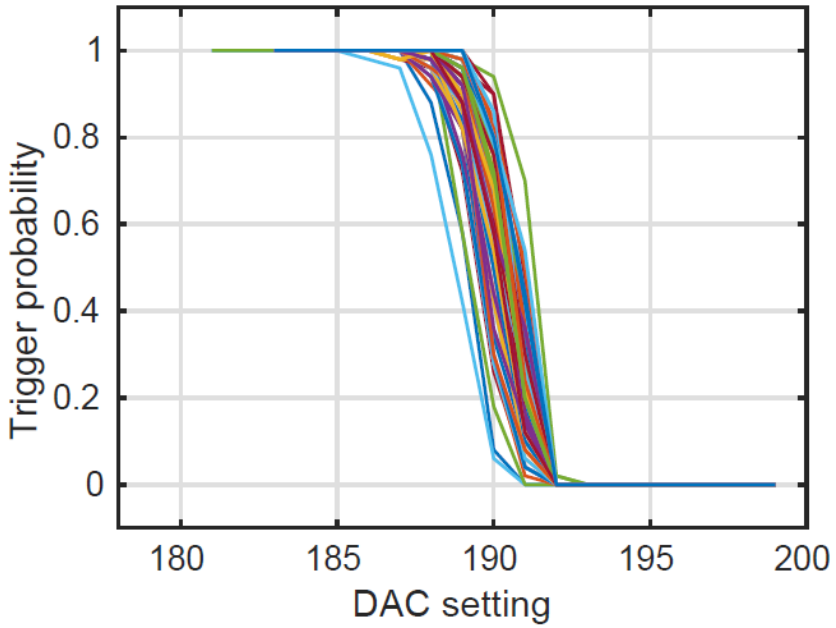


Figure 4: TOA S-curves at 32 fC

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Conclusion

- SKIROC2_CMS is a versatile chip for Si pads
  - 64 ch dual polarity charge/current preamplifier
  - HG/LG variable shaper 10-75 ns
  - 13 deep 40 MHz analog memory for event buffering
  - Fast branch (5 ns) for timing TOA and TOT
  - Internal 12 bit ADC/TDC

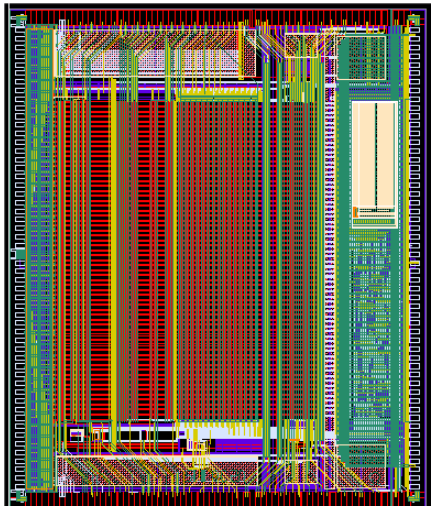
- SKIROC2_CMS for HGCAL testbeam operation
  - Will be used to validate HGCAL readout architecture
  - Front-end boards studies and system tests

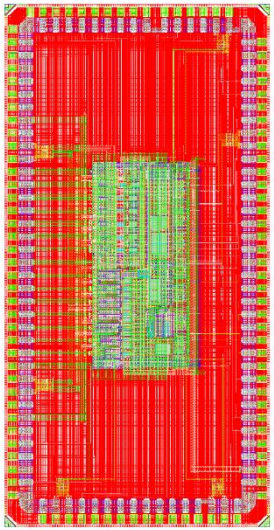
Conclusion

backup

Status of HGCAL electronics

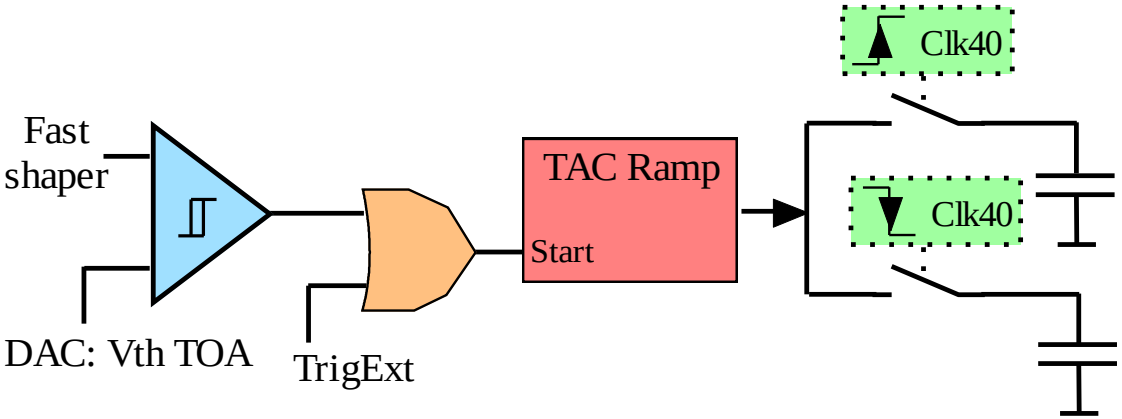
- SKIROC2_CMS received beg june
  - Preliminary tests shown here
- Test vehicle 1 submitted in may
  - Various preamp flavours, shapers, discriminators
  - TSMC130nm, received last week
- Test vehicle 2 foreseen in the fall
  - Different variants of a full one channel
- 64ch chip HGROC V1 foreseen june 2017
  - Collaboration AGH, CERN, Imperial, CEA/IRFU

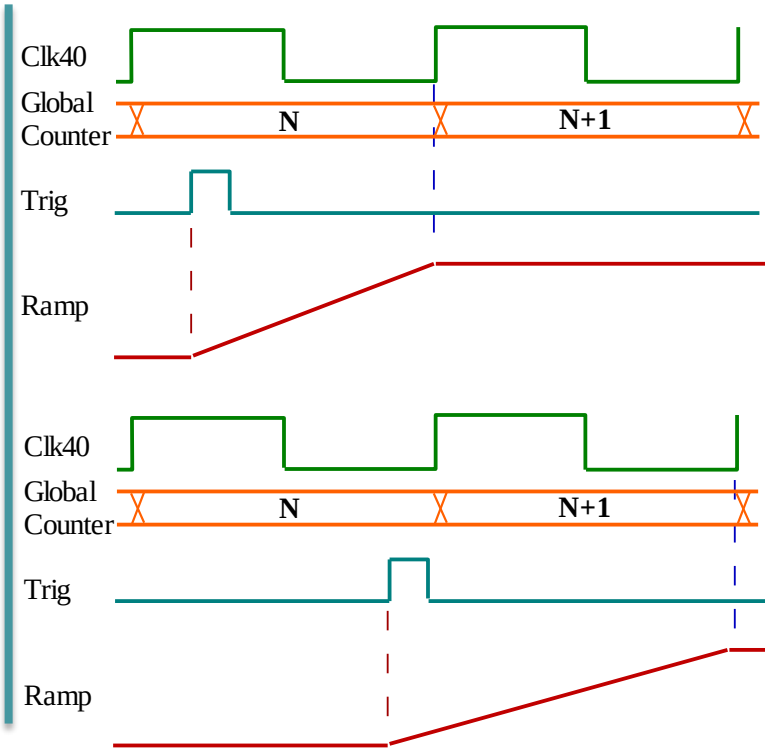




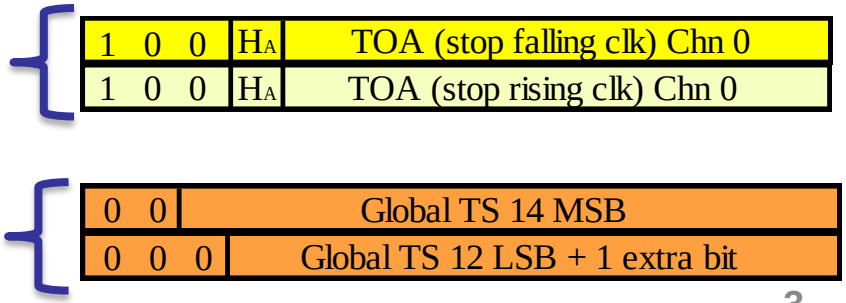
Time of Arrival principle (TOA)

- TOA based on a Time to Amplitude Converter (TAC):
  - 1 analog ramp / channel sampled on clock edges (both)
  - 1 global counter @ 40 MHz sampled with OR64_TOA
  - 1 global TrigExt available to calibrate ramps



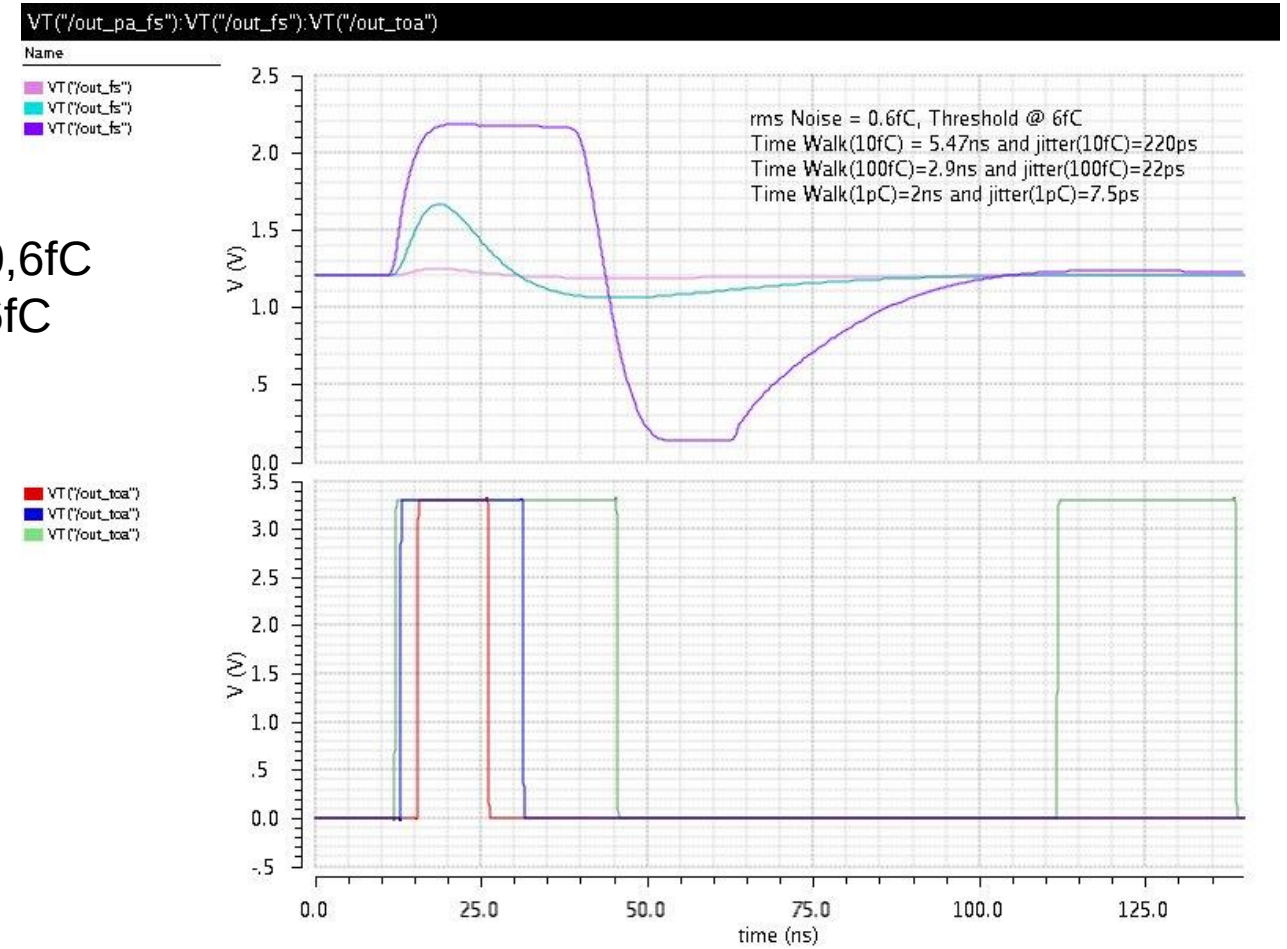


- If needed, pulse shape in “rolling” SCA used to mitigate counter value (multi-hits)
- Channel with TOA data are marked with Hit bit
- Relevant data in memory mapping:
  - Digitized TAC ramp (both edged)
  - Hit bit (H_A)
  - Global counter value @ 40 MHz



ToA: Time walk and jitter

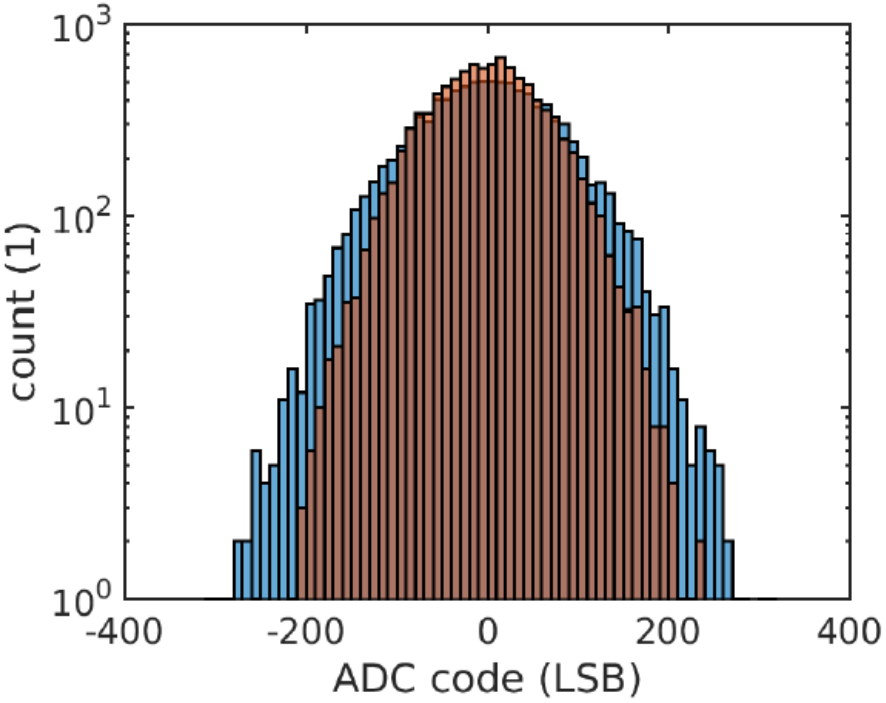
Rms Noise = 0,6fC
Threshold @ 6fC



Qinj(fC)	Time walk (ns)	Jitter (ps)
10	5,47	220
100	2,9	22
1000	2	7,5

Coherent and incoherent noise in ISA

- Using direct and alternate sums (DS and AS) on n channels (n=64)
- Incoherent noise IN=AS/√n
- Coherent noise : CN = $\sqrt{DS^2 - AS^2}$ /n
- Cohrent noise fraction : CF = CN/IN



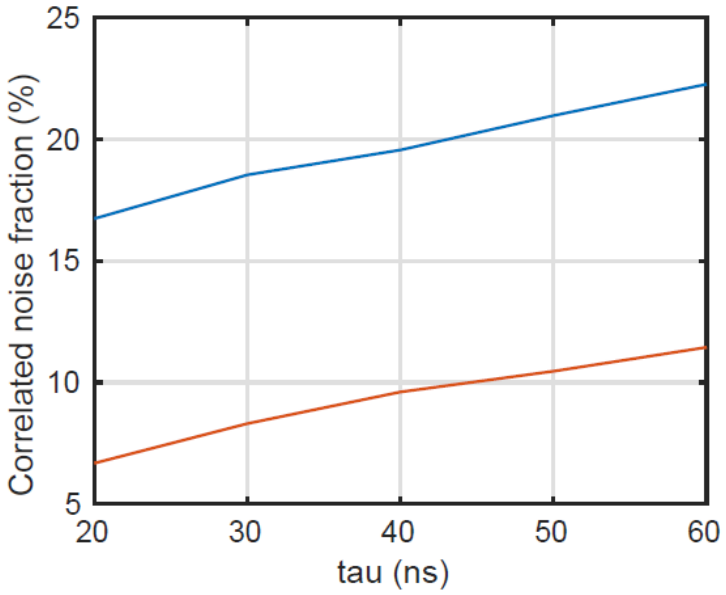


Figure 22: Correlated noise fraction (correlated/white)

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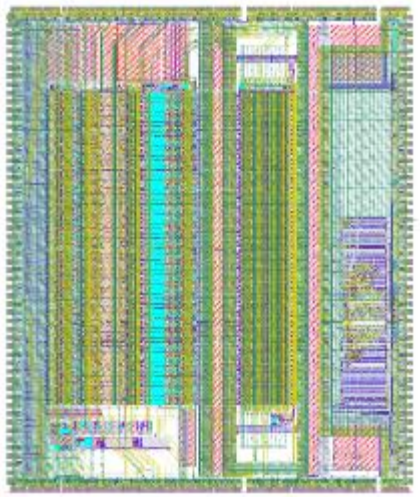
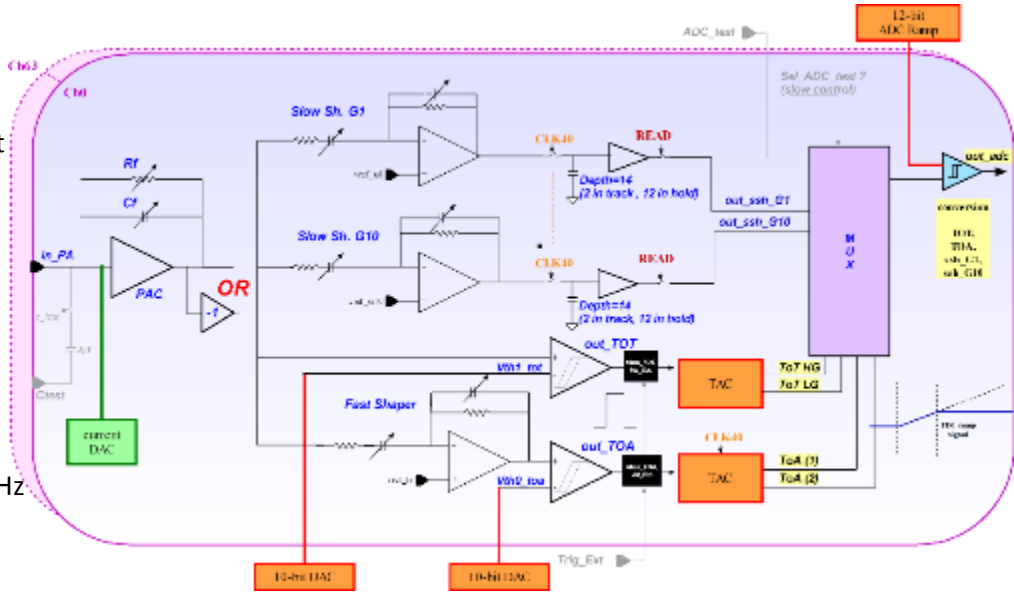
SKIROC2-CMS analogue architecture

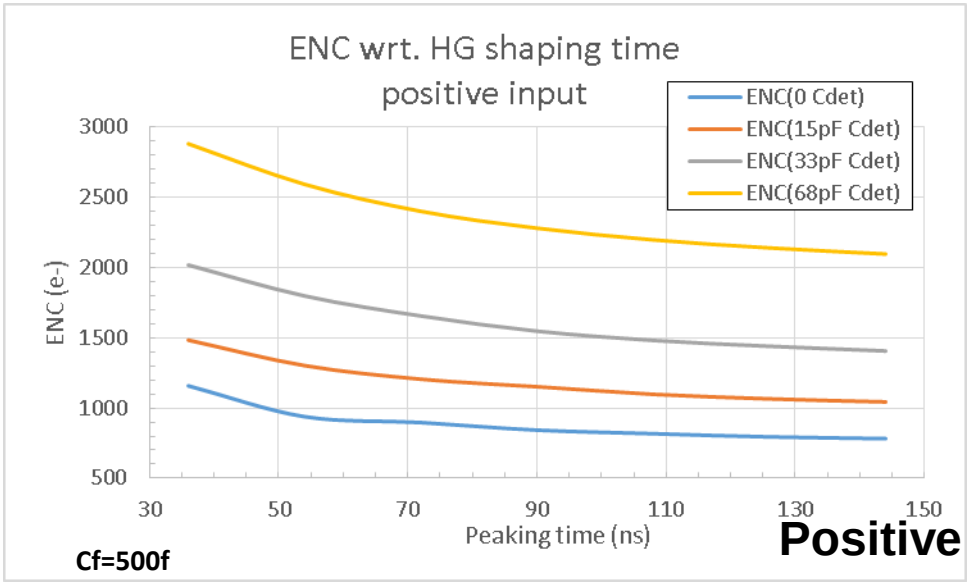
- Input DAC and 3pF calibration Cap.
- Versatile preamplifier
  - Dual polarity: single first stage with input PMOS transistor (available NMOS are directly on substrate), one feedback for each polarity (likely better for positive input charge), high dynamic range optimization
  - 60 dB Open loop gain, 4 GHz GBWP
  - Variable Rf: global 8 bits, from 10k to 2,55M
  - Variable Cf: global 6 bits, from 62fF to 4pF
- Charge measurement in 12 deep SCA
  - Slow shapers: gain 1 and 10, CRRC2; variable shaping time: global 4 bits, from 10ns to 150ns; output buffer
  - 2 measurements by BX, HG and LG
  - Nominal: roll mode @ 40MHz; custom mode: managed by external trigger
- Charge measurement with ToT for signal after peamp saturation
  - Discriminator connected to the preamp output
  - Fast ramp dedicated to the special study of the non-linear part
  - Slow ramp for the entire range (up to 10pC)
  - ToT data are memorized into the feedback capacitance of the integrator, rising edge starts the ramp and falling edge stop it
- Time measurement
  - Fast shaper: CRRC, gain 6, shaping time: 3bits, 1,25 to 9ns
  - Fast discri
  - Ramp: 35ns, rising edge starts the ramp
  - Time SCA: 2 holds done on rising and falling edges of the 40MHz
- Analogue to digital conversion
  - 12 bits Wilkinson ADC, common ramp

SKIROC2-CMS





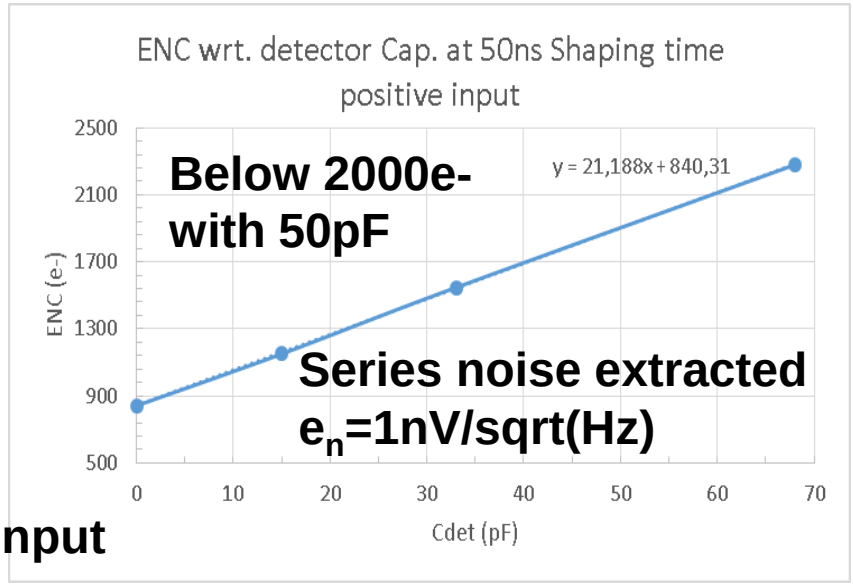
Noise measurements

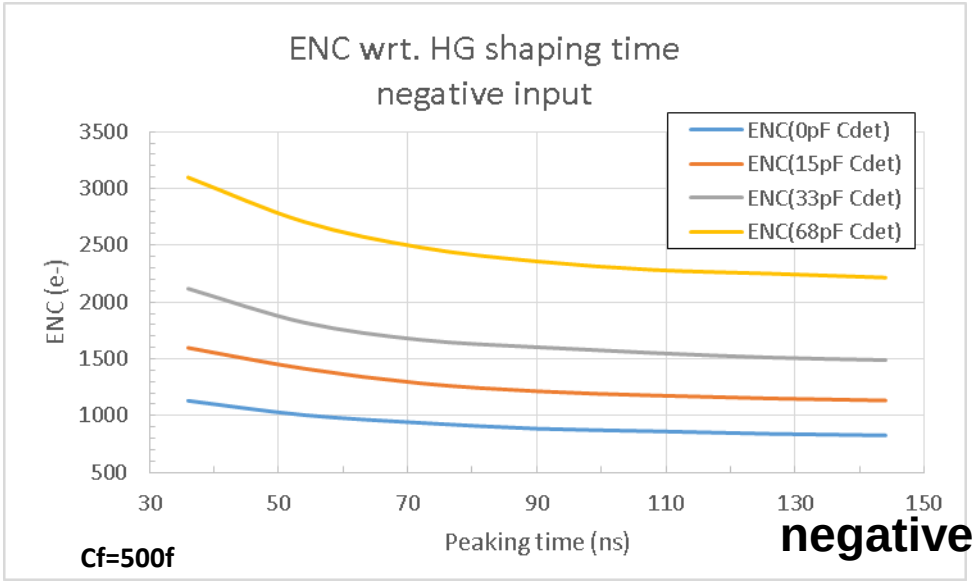


Cf=500f

Rf=2M

Positive input

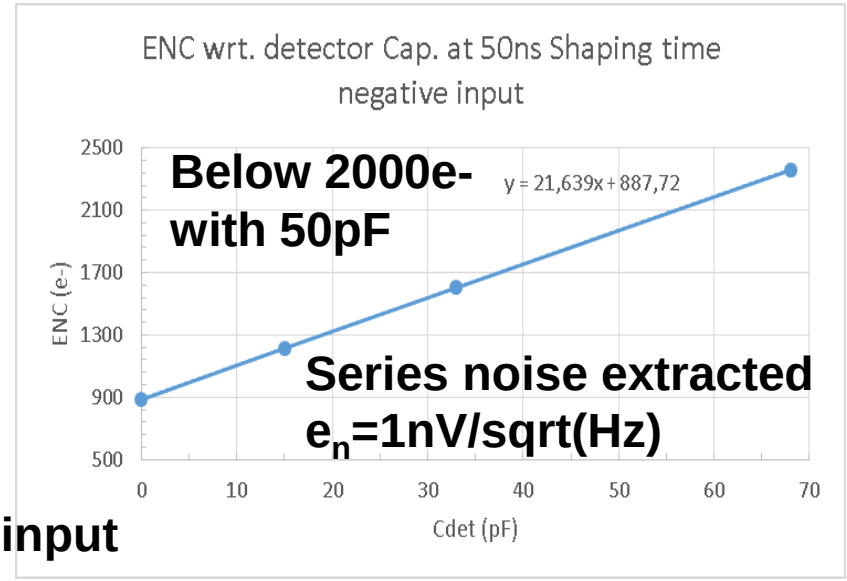




Cf=500f

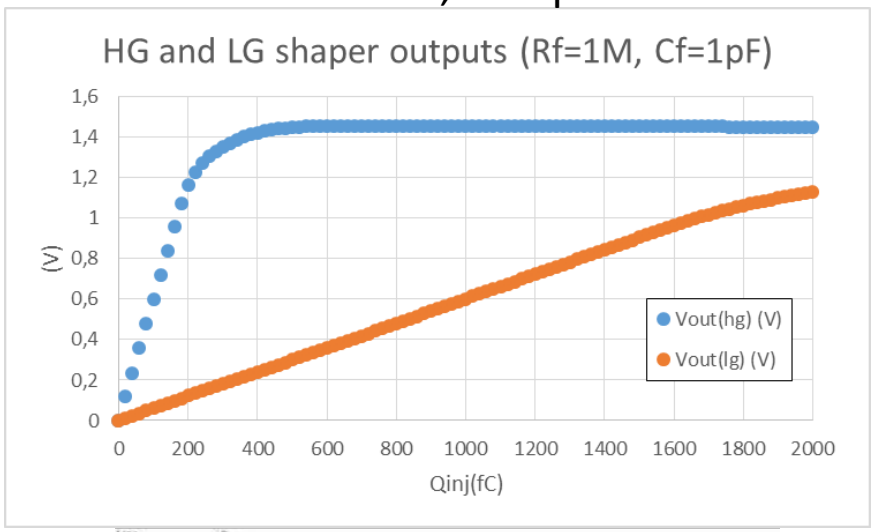
Rf=2M

negative input

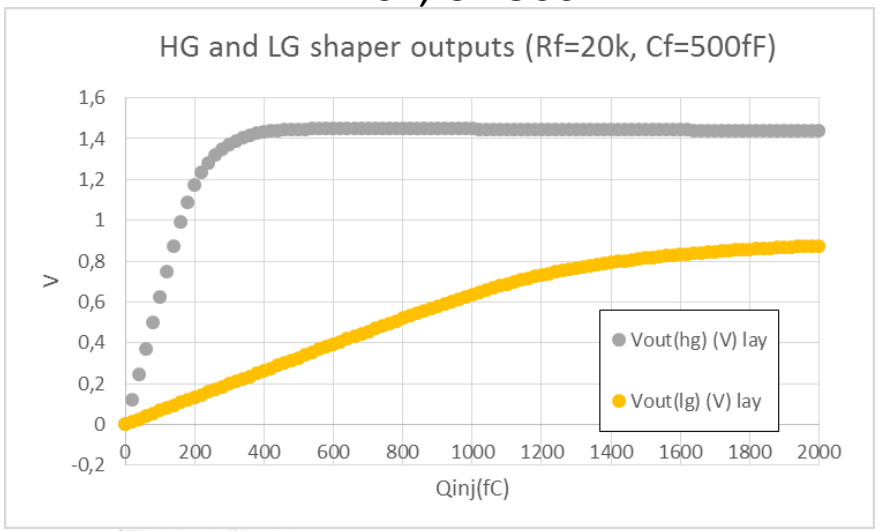


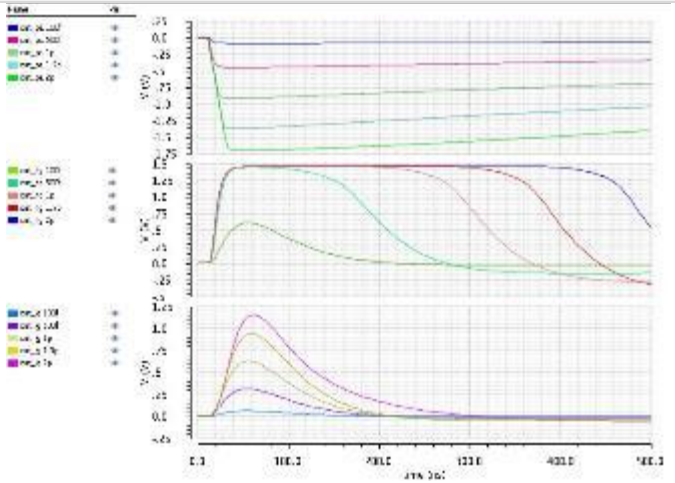
Positive input: HG and LG linearity post-layout simulations

Charge PA
Rf=1M, Cf=1pF



Current PA
Rf=20k, Cf=500fF

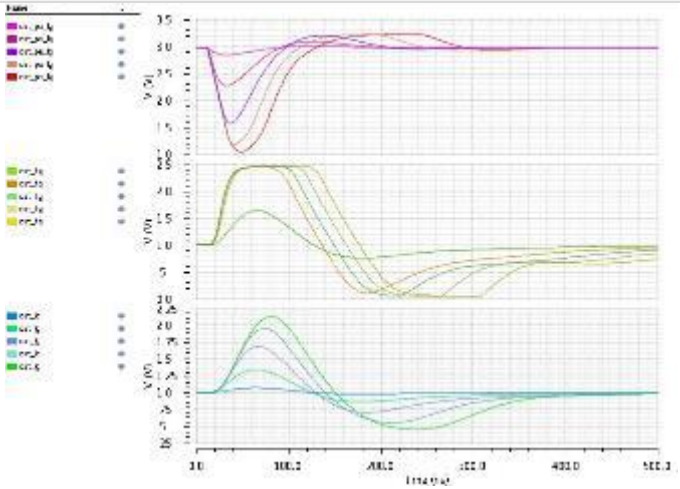




Preamp output

HG shaper output

LG shaper output

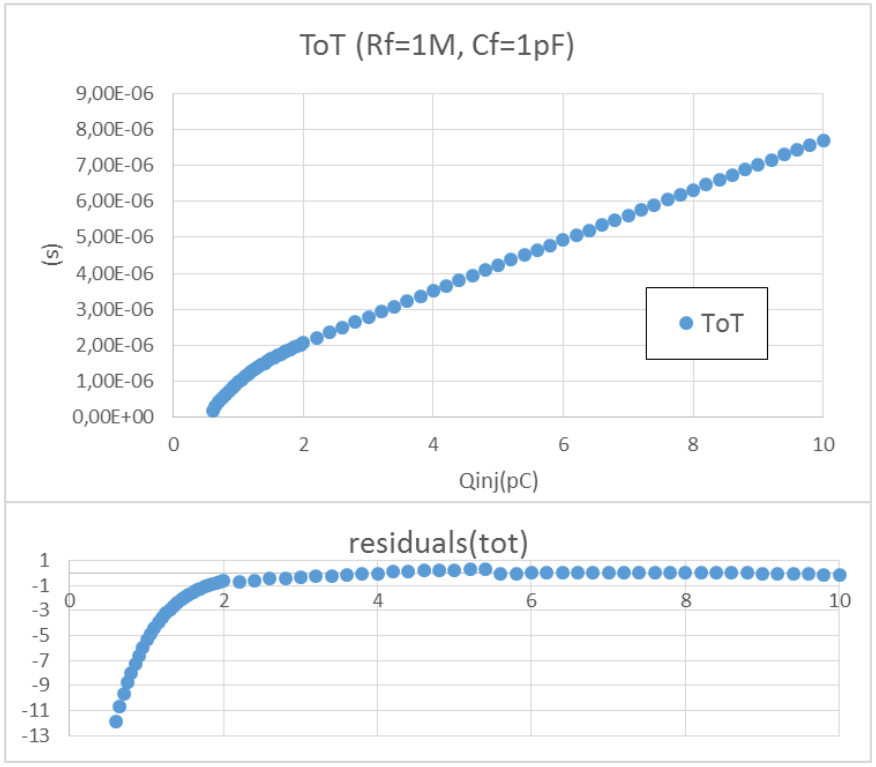


- HG linearity: from 0 to 180 fC
- LG linearity: from 0 to 1700 fC

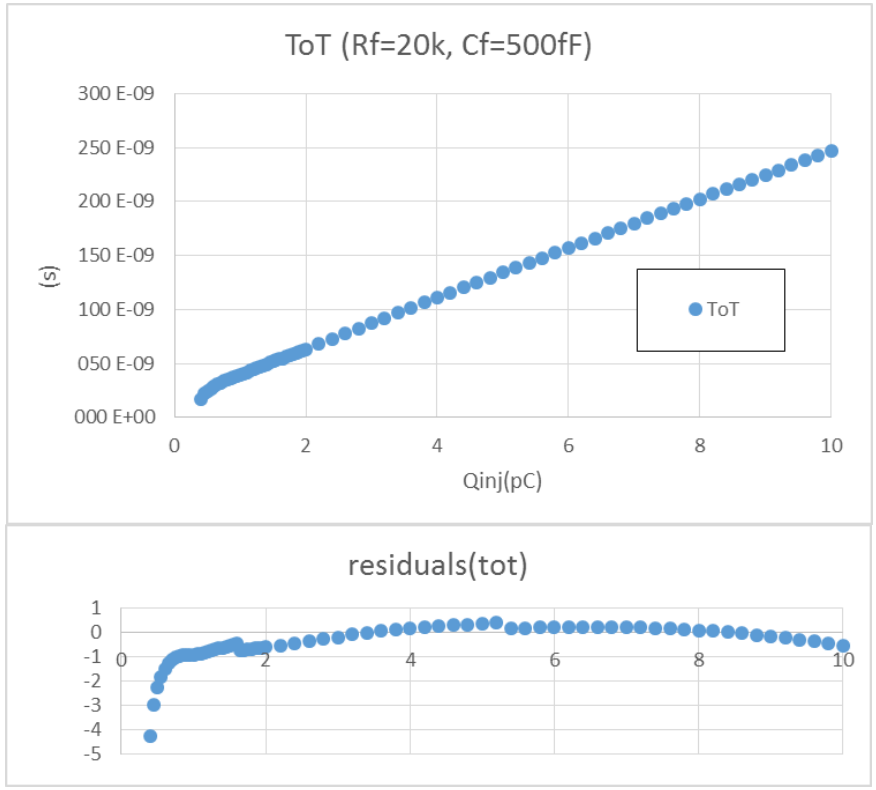
- HG linearity: from 0 to 160 fC
- LG linearity: from 0 to 950 fC

Positive input: ToT post-layout simulations

Charge PA
Rf=1M, Cf=1pF



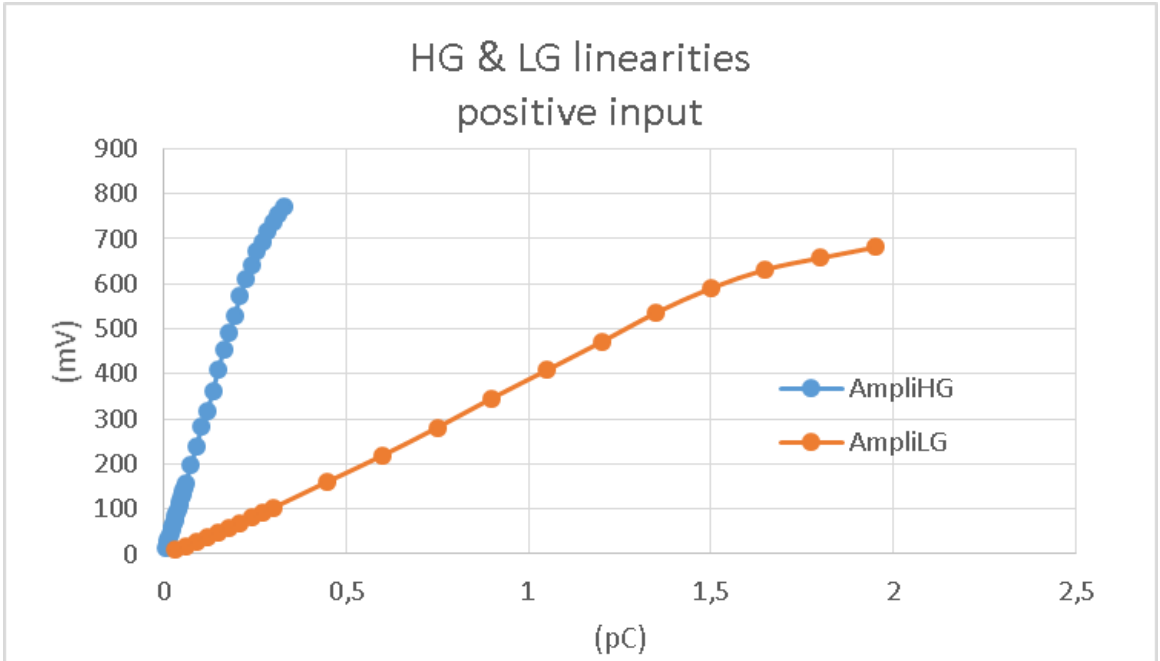
Current PA
Rf=20k, Cf=500fF

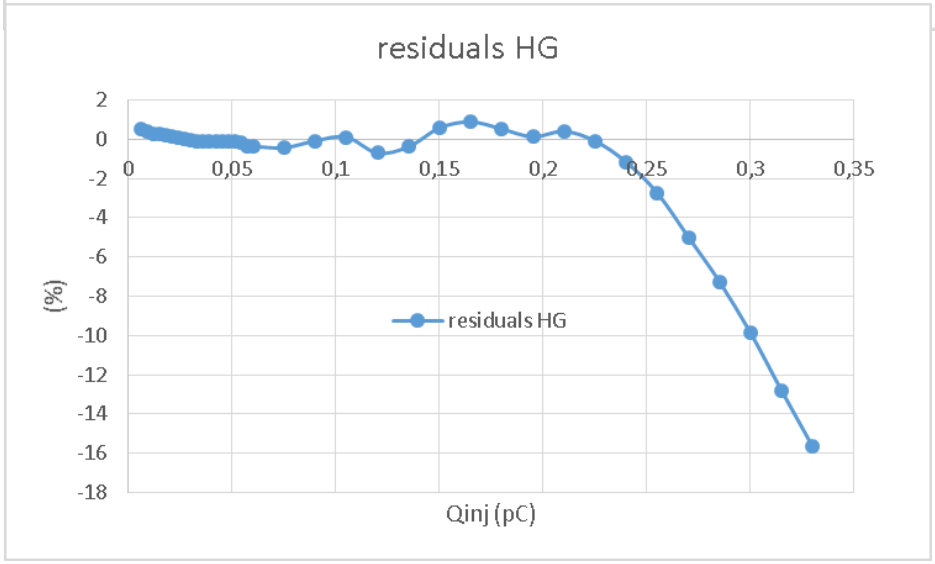
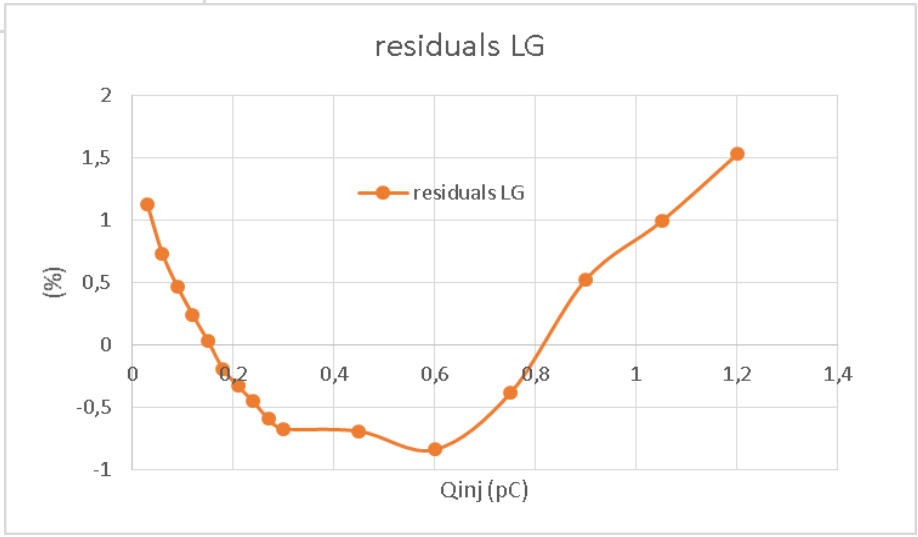


- Threshold @ 700 fC
- ToT linearity: from 800 fC to 10 pC

- Threshold @ 450 fC
- ToT linearity: from 1,7 pC to 10 pC

Linearity measurements (HG and LG)



Setup:
Cf=500fF,
Rf=30k,
Cd=68pF
Tau = 40ns

linearity better than 1% up to 250fC for HG and 1pC for LG