HGCAL calorimeter for phase 2 (technical proposal)

Modules
With 2x 6 - 8” Hexagonal Si sensors, PCB, FE chip, on W/Cu baseplate

Modules mounted on Cu Cooling plate with embedded pipe
=> Cassettes

Cassettes inserted in mechanical structure (containing absorber)

12 Cassettes mounted together to form the ECAL (EE) and Front HCal (FH)

3 sensor active thicknesses 100-200-300 µm
0.5-1 cm² pads for 100(-00/300) µm
Capacitance ~30-50 pF

Final design still under development

Replaced EndCap (maintained at -30°C)
HGCAL Front-End electronics

- Stringent requirements for Front-End Electronics
  - Low power (<10 mW), low noise (<2000 e-), high radiation (200 Mrad, $10^{16}$ N)
  - System on chip (digitization, processing…), high speed readout (5-10 Gb/s)
  - ~92,000 FE chips

- Baseline: charge + ToT [J. Kaplon CERN]
  - Charge readout 0-100 fC (0-50 MIP) 10 bits
  - Time over Threshold (0.1-10 pC) (40-2000 MIPs) : 12 bits
  - In addition: timing information to 50 ps accuracy
  - Variants: more classical readout (bi-gain) or switched feedback [Omega]
VFE architectural issues

- key issues to be studied:
  - Noise
  - Resolution
  - Stability
  - Linearity
  - Accuracy
  - Calibration
  - Crosstalk
  - Radiation
  - Timing
  - Systematic effects

- And also:
  - 65/130 nm
  - System issues
  - Trigger path

CdLT HGCAL electronics

0.2 pC ~100 MIPS
SKIROC2-CMS: Electronics for testbeam

- Testbeam electronics
  - Use SKIROC2 from CALICE to exercise system issues (low noise, large range)
  - Complex front-end boards designed at UCSB and FNAL and CERN
  - Evolutive readout designed at FNAL

- Development of SKIROC2-CMS
  - Optimized version for CMS test beams, pin to pin compatible
  - Dual polarity charge/current preamplifier
  - Faster slow shaper (25ns instead of 200ns)
  - SCA in roll mode (sampling of slow shapers @ 40MHz, depth = 300ns)
  - ToT for high input charge
  - TDC (TAC) for ToA (~20 ps binning, ~50ps jitter)
  - Will replace SKIROC2 on modules for timing and ToT studies
Overview of SK2_CMS

- 64 channels versatile Si calorimeter readout based on CALICE SKIROC2
Digital readout scheme

- Based on Calice chips readout scheme

- Roll mode @ 40MHz
- depth 12x25ns=300ns

- 12-bit Wilkinson ADC, starts on external Trigger
- 2 ToT (fast & slow); 2 ToA; 2x13 HG & LG Charge
- Duration (worst case) = $2^{12} \times 25\text{n} \times 30 = 3\text{ ms}$

- OC @ 5MHz (SK2) to LVDS @ 40MHz (SK2-CMS)
- Cst. $1924 \times 16 \times 25 = 770\mu\text{s}$
Preamp architecture

- PMOS input $I_d=1$ mA, direct cascode
- Variable $R_f$ 20k-2M, $C_f=0.06-4p$ (4 bits)
- Level shifter for negative polarity

<table>
<thead>
<tr>
<th>ENC</th>
<th>$R_f=1M$, $C_f=1pF$</th>
<th>$R_f=20k$, $C_f=500fF$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive input</td>
<td>0.2fC (1250 e-)</td>
<td>0.25fC (1560 e-)</td>
</tr>
<tr>
<td>Negative input</td>
<td>0.23fC (1440 e-)</td>
<td>0.3fC (1875 e-)</td>
</tr>
</tbody>
</table>
Positive input: HG and LG linearity post-layout simulations

**Preamp: R_f=1M, C_f=1pF**

- HG linearity: from 0 to 180 fC
- LG linearity: from 0 to 1700 fC

**Preamp: R_f=20k, C_f=500fF**

- HG linearity: from 0 to 160 fC
- LG linearity: from 0 to 950 fC
Time over Threshold principle (TOT)

- TOT based on a Time to Amplitude Converter (TAC):
  - 2 analog ramp / channel
  - Slow ramp to validate TOT mode (~0-500 ns)
  - Fast ramp to characterize non-linear region (~0-50 ns)
  - 1 global TrigExt available to calibrate TOT

Channel with TOT data are marked with Hit bit

Relevant data in memory mapping:
- Digitized TAC ramp (fast / slow)
- Hit bit (HT)

<table>
<thead>
<tr>
<th></th>
<th>Hit bit (HT)</th>
<th>TOT slow Chn 0</th>
<th>TOT fast Chn 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 0</td>
<td>HT</td>
<td>TOT slow Chn 0</td>
<td>TOT fast Chn 0</td>
</tr>
</tbody>
</table>
Positive input: ToT post-layout simulations

Preamp: R_f=20k, C_f=500fF

- Threshold @ 700 fC
- ToT linearity: from 800 fC to 10 pC

- Threshold @ 450 fC
- ToT linearity: from 1.7 pC to 10 pC
Timing studies

- Timing tests [M Mannelli et al. ACES2016]
  - 700ps/(S/N) (+) 20 ps
  - But 2 GHz BB amps
  - 5 Gs/s digitization
- Theory: \( \sigma_t^J \approx \alpha C_d \sqrt{\frac{t_d}{g_m}} \)
- But different readout electronics (CSA)
  - Different S/N, Reflections in PCB?
  - Time walk corrections
- Expect ~ 3-4 ns/fC (+) 50 ps (Cd=50pF)

Cd=50 pF th=100um td=1ns MIP=1.5 fC
50 ohm transmission line, length=500ps (4 cm)
Some time performance simulations

**Time Walk (ns)**
30pF Cdet; T=-30°C

- Blue line: Time Walk (ns) - preamp gain = 2mV/fC
- Orange line: Time Walk (ns) - preamp gain = 4mV/fC

**jitter (ps)**
30pF Cdet; T=-30°C; preamp gain = 2mV/fC

- Blue line: Jitter (ps)

**Time Walk**
10fC injected charge

- Blue line: Time Walk (ns) - preamp gain = 2mV/fC
- Orange line: Time Walk (ns) - preamp gain = 4mV/fC

**jitter @10fC injected wrt. Cdet**

- Blue line: Jitter (10fC Q inj; 500fF preamp Cf; 20ns fast pt)
- Orange line: Jitter (10fC Q inj; 500fF preamp Cf; 2.5ns fast pt)
Experimental measurements

- Chips packaged in BGA for testboards
- Tests carried out at Imperial College, Univ Split and OMEGA
SCA operation

- 40 MHz circular analog memory. 13 cells in store and 2 in track
- Allows ~300 ns trigger latency
Waveforms with 1 MIP injection

- 3 fC test pulse injection ~1 MIP
  - $V_{out} = 5 \text{ mV}$  $N = 0.4 \text{ mV}$

- HG shaper $\tau = 20 \text{ ns}$
  - $V_{out} = 15 \text{ mV}$  $N = 1.2 \text{ mV}$

- Fast shaper $\tau = 5 \text{ ns}$
  - $V_{out} = 12 \text{ mV}$  $N = 1.4 \text{ mV}$
Reconstructed waveforms CSA config

- Charge sensitive configuration: $R_f = 2.5 \text{ M}\Omega$  $C_f = 0.5\text{pF}$
- Hi Gain / Lo Gain positive/negative configurations

![Graphs showing ADC code over time for different tau values in Low-gain (LG) and High-gain (HG) configurations with positive and negative polarities.](image-url)
Linearity

- Linearity < 1%,
  temperature sensitivity ~0.1%/K

![Graphs showing linearity and temperature sensitivity](image-url)

**Figure 2:** High-gain transfer function for different T: positive polarity, $\tau = 40\,\text{ns}$.
Uniformity, temperature stability

- Dispersion ~0.5% rms stability : 0.1%/K

Figure 1: Low-gain gain of each channel, $\sigma_{25°C}$=0.014 (lsb/fC), $\sigma_{30°C}$=0.014 (lsb/fC)

Figure 2: Low-gain pedestal of each channel in ADC units, $\sigma_{25°C}$=6.3 (lsb), $\sigma_{30°C}$=6.0 (lsb)

Figure 4: High-gain gain of each channel, $\sigma_{25°C}$=0.120 (lsb/fC), $\sigma_{30°C}$=0.126 (lsb/fC)

Figure 16: High-gain gain of each channel, $\sigma_{25°C}$=0.116 (lsb/fC), $\sigma_{30°C}$=0.122 (lsb/fC)
- $Cd = 47 \text{ pF}$, positive and negative preamps
- Shaping time = 20-60 ns
- ENC = 0.3-0.4 fC = 2000-2500 e-
- Series-noise dominated, slightly worse for negative (as expected)

![Graphs showing Noise vs shaper setting scaled based on Fig. 5 and Fig. 11.](image)
• Linear fit of series noise gives $e_n = 1.0 \text{nV}/\sqrt{\text{Hz}}$
• Parasitic capacitance: $C_a = 34 \text{ pF}$ (10 pF chip 20 pF board)

![Graph](image)

Figure 8: High-gain noise vs $C_d$, positive polarity, $\tau = 40 \text{ ns}$. Least-squares linear fit: $y = 0.17367 + 50.718 \times 10^{-3}x$ (fC, pF), $y = 0$ yields $C = 34 \text{ pF}$. 
• Series noise dominated at fast shaping
• Significant supply noise at slow shaping
• Removed with additional $v_{DDA}$ filtering
Coherent and incoherent noise

- Using direct and alternate sums (DS and AS) on \( n \) channels (\( n=64 \))
- Incoherent noise \( \text{IN} = \text{AS} / \sqrt{n} \)
- Coherent noise : \( \text{CN} = \sqrt{\text{DS}^2 - \text{AS}^2} / n \)
- Coherent noise fraction : \( \text{CNF} = \text{CN} / \text{IN} \approx 10\% \) at fast shaping.
- Measurement after \( \nu_{\text{DDA}} \) decoupling

Figure 18: Histogram of direct and alternating sums, \( \tau=40 \) ns, High gain

Figure 22: Correlated noise fraction (correlated/white)
Waveforms: ISA configuration

- Current sensitive configuration: \( R_f = 20 \text{ k}\Omega \) \( C_f = 0.5\text{pF} \)
- Hi Gain / Lo Gain positive/negative

Figure 33: Shaper response for different \( \tau \), Low-gain, positive polarity

Figure 34: Shaper response for different \( \tau \), High-gain, positive polarity

Figure 35: Shaper response for different \( \tau \), Low-gain, negative polarity

Figure 36: Shaper response for different \( \tau \), High-gain, negative polarity
Trigger sensitivity for ToT

- discriminator at preamp output
- Low Threshold 30 fC high threshold 100 fC
- ~ 0.7 DACU / fC
- Dispersion ~5 fC

Figure 10: TOT S-curves at 10 fC

Figure 16: TOT S-curves at 100 fC
ToT measurements

- TOT measurements starting…

**TOT VS HG/LG, -30C**

![Graph showing TOT vs Charge for different DAC settings at -30C temperature.](image)
ToT Measurement

Time over Threshold positive input

\[ y = 22.753x + 50.622 \]

Time over Threshold negative input

\[ y = 49.152x + 33.81 \]

Low gain Saturation

1pC

residuals

1pC

residuals

CdLT SKIROC2_CMS TWEPP16
Trigger sensitivity for ToA

- High speed discriminator after fast shaper (4 ns)
- Threshold at 10 fC and 30 fC
- Preliminary timing performance: 270 ps at 30 fC and 57 ps at 300 fC
- Will allow system level studies….

Figure 1: TOA S-curves at 10 fC

Figure 4: TOA S-curves at 32 fC
SKIROC2_CMS is a versatile chip for Si pads
- 64 ch dual polarity charge/current preamplifier
- HG/LG variable shaper 10-75 ns
- 13 deep 40 MHz analog memory for event buffering
- Fast branch (5 ns) for timing TOA and TOT
- Internal 12 bit ADC/TDC

SKIROC2_CMS for HGCAL testbeam operation
- Will be used to validate HGCAL readout architecture
- Front-end boards studies and system tests
Status of HGCAL electronics

• SKIROC2_CMS received beg june
  – Preliminary tests shown here

• Test vehicle 1 submitted in may
  – Various preamp flavours, shapers, discriminators
  – TSMC130nm, received last week

• Test vehicle 2 foreseen in the fall
  – Different variants of a full one channel

• 64ch chip HGROC V1 foreseen june 2017
  – Collaboration AGH, CERN, Imperial, CEA/IRFU
**Time of Arrival principle (TOA)**

- TOA based on a Time to Amplitude Converter (TAC):
  - 1 analog ramp / channel sampled on clock edges (both)
  - 1 global counter @ 40 MHz sampled with OR64_TOA
  - 1 global TrigExt available to calibrate ramps

- If needed, pulse shape in “rolling” SCA used to mitigate counter value (multi-hits)
- Channel with TOA data are marked with Hit bit
- Relevant data in memory mapping:
  - Digitized TAC ramp (both edged)
  - Hit bit \( H_A \)
  - Global counter value @ 40 MHz

```
<table>
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<tr>
<th></th>
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<th>HA</th>
<th>TOA (stop falling clk) Chn 0</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
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<th>GlobaTS 14 MSB</th>
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<table>
<thead>
<tr>
<th></th>
<th></th>
<th>GlobaTS 12 LSB + 1 extra bit</th>
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Rms Noise = 0.6fC  
Threshold @ 6fC

<table>
<thead>
<tr>
<th>Qinj (fC)</th>
<th>Time walk (ns)</th>
<th>Jitter (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>5.47</td>
<td>220</td>
</tr>
<tr>
<td>100</td>
<td>2.9</td>
<td>22</td>
</tr>
<tr>
<td>1000</td>
<td>2</td>
<td>7.5</td>
</tr>
</tbody>
</table>

Time walk and Jitter

Qinj (fC) = 10

Time Walk = 5.47ns and Jitter = 220ps

Qinj (fC) = 100

Time Walk = 2.9ns and Jitter = 22ps

Qinj (fC) = 1000

Time Walk = 2ns and Jitter = 7.5ps
Coherent and incoherent noise in ISA

- Using direct and alternate sums (DS and AS) on n channels (n=64)
- Incoherent noise $\text{IN} = \text{AS}/\sqrt{n}$
- Coherent noise: $\text{CN} = \sqrt{\text{DS}^2 - \text{AS}^2} / n$
- Coherent noise fraction: $\text{CF} = \text{CN} / \text{IN}$

![Graph showing ADC code distribution and correlated noise fraction](image-url)
SKIROC2-CMS analogue architecture

- **Input DAC and 3pF calibration Cap.**
- **Versatile preamplifier**
  - Dual polarity: single first stage with input PMOS transistor (available NMOS are directly on substrate), one feedback for each polarity (likely better for positive input charge), high dynamic range optimization
  - 60 dB Open loop gain, 4 GHz GBWP
  - Variable Rf: global 8 bits, from 10k to 2.55M
  - Variable Cf: global 6 bits, from 62fF to 4pF
- **Charge measurement in 12 deep SCA**
  - Slow shapers: gain 1 and 10, CRRC2; variable shaping time: global 4 bits, from 10ns to 150ns; output buffer
  - 2 measurements by BX, HG and LG
  - Nominal: roll mode @ 40MHz; custom mode: managed by external trigger
- **Charge measurement with ToT for signal after peamp saturation**
  - Discriminator connected to the preamp output
  - Fast ramp dedicated to the special study of the non-linear part
  - Slow ramp for the entire range (up to 10pC)
  - ToT data are memorized into the feedback capacitance of the integrator, rising edge starts the ramp and falling edge stop it
- **Time measurement**
  - Fast shaper: CRRC, gain 6, shaping time: 3bits, 1.25 to 9ns
  - Fast discr
  - Ramp: 35ns, rising edge starts the ramp
  - Time SCA: 2 holds done on rising and falling edges of the 40MHz
- **Analogue to digital conversion**
  - 12 bits Wilkinson ADC, common ramp
Noise measurements

**ENC wrt. HG shaping time**

- **positive input**
  - \( e_n = 1 \text{nV/\sqrt{Hz}} \)

- **negative input**
  - \( e_n = 1 \text{nV/\sqrt{Hz}} \)

C\(_f\) = 500f

R\(_f\) = 2M

**ENC wrt. detector Cap. at 50ns Shaping time**

- **positive input**
  - Below 2000e-
  - with 50pF
  - \( y = 21,188x + 840,31 \)

- **negative input**
  - Below 2000e-
  - with 50pF
  - \( y = 21,639x + 887,72 \)
Positive input: HG and LG linearity post-layout simulations

**Charge PA**
Rf=1M, Cf=1pF

**Current PA**
Rf=20k, Cf=500fF

- HG linearity: from 0 to 180 fC
- LG linearity: from 0 to 1700 fC
- HG linearity: from 0 to 160 fC
- LG linearity: from 0 to 950 fC
Positive input: ToT post-layout simulations

**Charge PA**
Rf=1M, Cf=1pF

- Threshold @ 700 fC
- ToT linearity: from 800 fC to 10 pC

**Current PA**
Rf=20k, Cf=500fF

- Threshold @ 450 fC
- ToT linearity: from 1,7 pC to 10 pC
Linearity measurements (HG and LG)

Setup:
C_f = 500 fF,
R_f = 30 k,
C_d = 68 pF

Tau = 40 ns

Linearity better than 1% up to 250 fC for HG and 1 pC for LG