Contribution ID: **98** Type: **Oral**

SKIROC2_CMS : an ASIC for testing CMS HGCAL

Wednesday 28 September 2016 10:15 (25 minutes)

SKIROC2_CMS is a chip derived from CALICE SKIROC2, providing 64 channels of low noise readout for 50pF Si-sensors over 10pC dynamic range. The pre-amps are followed by high/low gain 25ns shapers, 16-deep 40 MHz analog memory "waveform sampler"and 12-bit ADCs. A fast shaper followed by discriminator and TDC provide timing information to an accuracy of 50 ps, in order to test TOT and TOA techniques at system level.The chip, in AMS SiGe 0.35um, is expected in May. It will be tested and used for beam tests in the autumn.

Summary

The high granularity silicon tungsten calorimeter (HGCAL) chosen by the CMS collaboration to replace its endcaps for the phase 2 upgrade will provide unprecedented 5D images of electromagnetic showers. The sensors are made of ˜1cm² PIN diodes of 100-300um thickness providing a MIP signal around 1-4 fC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. In particular, they will provide charge measurement for large signals by a time over Threshold technique (TOT) and will also measure the time of arrival (TOA) to 50 ps. System issues are very critical in such a design and an important testbeam campaign has been programmed by the collaboration to validate the design and performance.
For this reason, it has been decided by the collaboration to start the tests early enough with an existing chip. The first modules were tested in beam at FNAL in april and use SKIROC2, which has been used for more than 5 years by the CALICE collaboration to test a similar calorimeter, but at lower speed and occupancy. Moreover, the timing capability of the sensors, down to 20 ps, provide powerful information for physics analysis and background mitigation. Therefore a pin-pin compatible variation of the chip tailored to CMS needs was submitted in January in an engineering run. It keeps the same architecture with variable gain preamps and variable shaping time dual-gain shapers, which were accelerated to 25 ns. The analog memory was modified to run at 40MHz and provide waveform sampling, this can be used to study timing performance independently and study possible pulse shape variations.
The other modifications concern the timing branch, where the fast shaper was accelerated to 5 ns. Two discriminators provide ToA and ToT informations, thanks to a TDC based on a time-to-amplitude converter with a step of 25 ps. Charge and time are then encoded with the same 12 bits ADCs as in SKIROC2 and read out following the same protocol, so that the chip can replace directly SKIROC2 on the testbeam modules and interface to the DAQ.
Simulation results indicate a noise below 2000e- for 50 pF detector capacitance and timing accuracy below 50 ps above 10 MIPS. Power dissipation is below 15 mW/channel.
The chip was sent to fabrication in January in AMS SiGe 0,35um and is expected back in may. It will be tested in the lab and mounted on sensors during the summer for beamtests in the fall.
Electrical tests results will be available by the time of the conference as well as preliminary measurements with modules.

Author: DE LA TAILLE, Christophe (OMEGA (FR))

Co-authors: THIENPONT, Damien (IN2P3/OMEGA); Mr DULUCQ, Frederic (OMEGA - Ecole Polytechnique - CNRS/IN2P3); MARTIN CHASSARD, Gisele (OMEGA - Ecole Polytechnique - CNRS/IN2P3); RAUX, Ludovic (OMEGA Ecole Polytechnique -CNT); CALLIER, Stephane (OMEGA - Ecole Polytechnique - CNRS/IN2P3)

Presenter: DE LA TAILLE, Christophe (OMEGA (FR))

Session Classification: ASIC

Track Classification: ASIC