A synchronous analog very front-end in 65nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC

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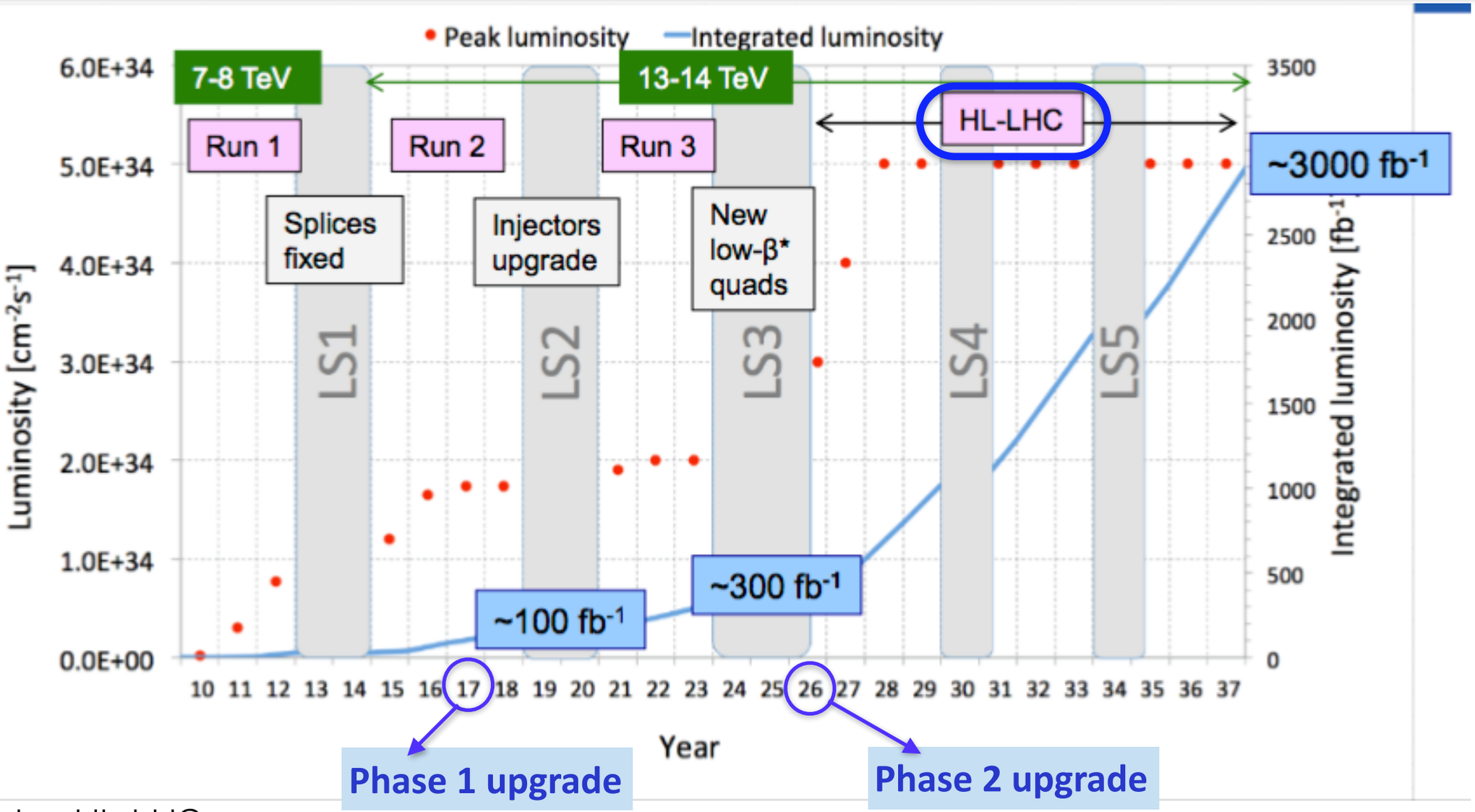
Outlook

- Introduction
- Synchronous architecture
  - Preamp
  - Comparator
- Measurements results
- Irradiation results
- Insertion in the CHIPIX65 demonstrator
- Conclusions

HL-LHC upgrade



- During HL-LHC:
  - The integrated luminosity of the machine will be increased by an order of magnitude between Phase 1 and 2 (**3000 fb^{-1} foreseen**)
  - Unprecedented Pile-Up conditions (**140-200 collisions per event**)
  - Very high particle flux **(3 GHz/cm^2)**
  - Unprecedented radiation levels (around **1 Grad in 10 years)**

Design communities on 65 nm phase 2 chip

- **RD53 collaboration** at CERN, a joint CMS-ATLAS effort approved in 2013 by LHCC
  - Common technology qualification
  - Around 20 institutes from different countries involved
  - Important INFN contribution
  - Submission of the final chip at beginning 2017

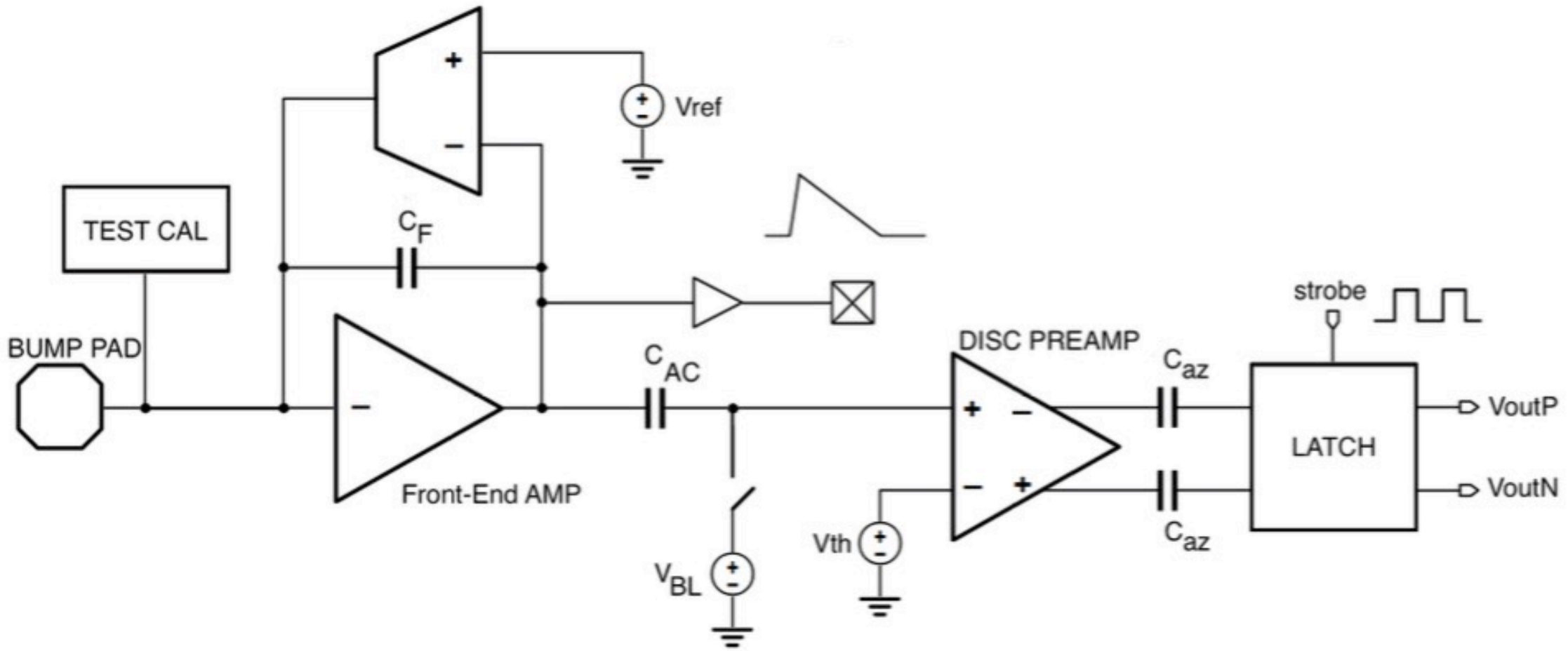
- **CHIPIX65**: approved by CSN5 in October 2013
  - Italian CMS/ATLAS groups involved
  - 8 INFN groups (Bari, Bergamo/Pavia, Lecce, Milano, Padova, Perugia, Pisa and Torino)
  - Small prototypes submissions during 2014 and 2015
  - Demonstrator chip submission in July 2016

Specs

- **Small pixel size** (in the chip → 50x50 um^2)
- **Low noise**
  - Goal of a low in time threshold (~ 1000 e^-)
- **Fast**
  - To keep dead time <1%
- **Compact analog design**
  - To leave at least half of the pixel area for the digital part (<35x35 μm^2)
- **Low power architecture**
  - Required in order to maintain the material budget as low as possible
  - Around 10 μW per pixel (analog + digital)

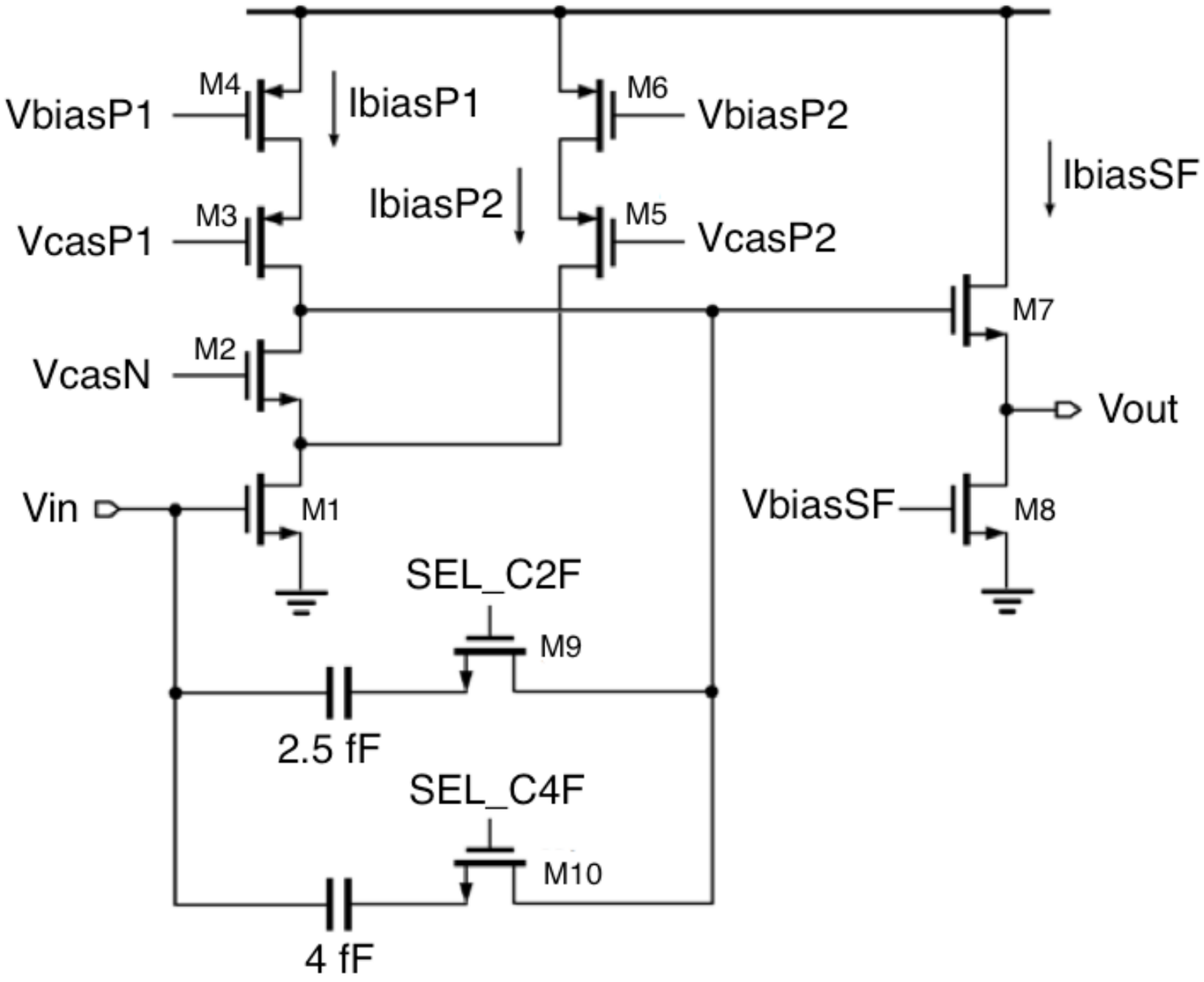
Synchronous analog very front-end architecture

Front-end scheme



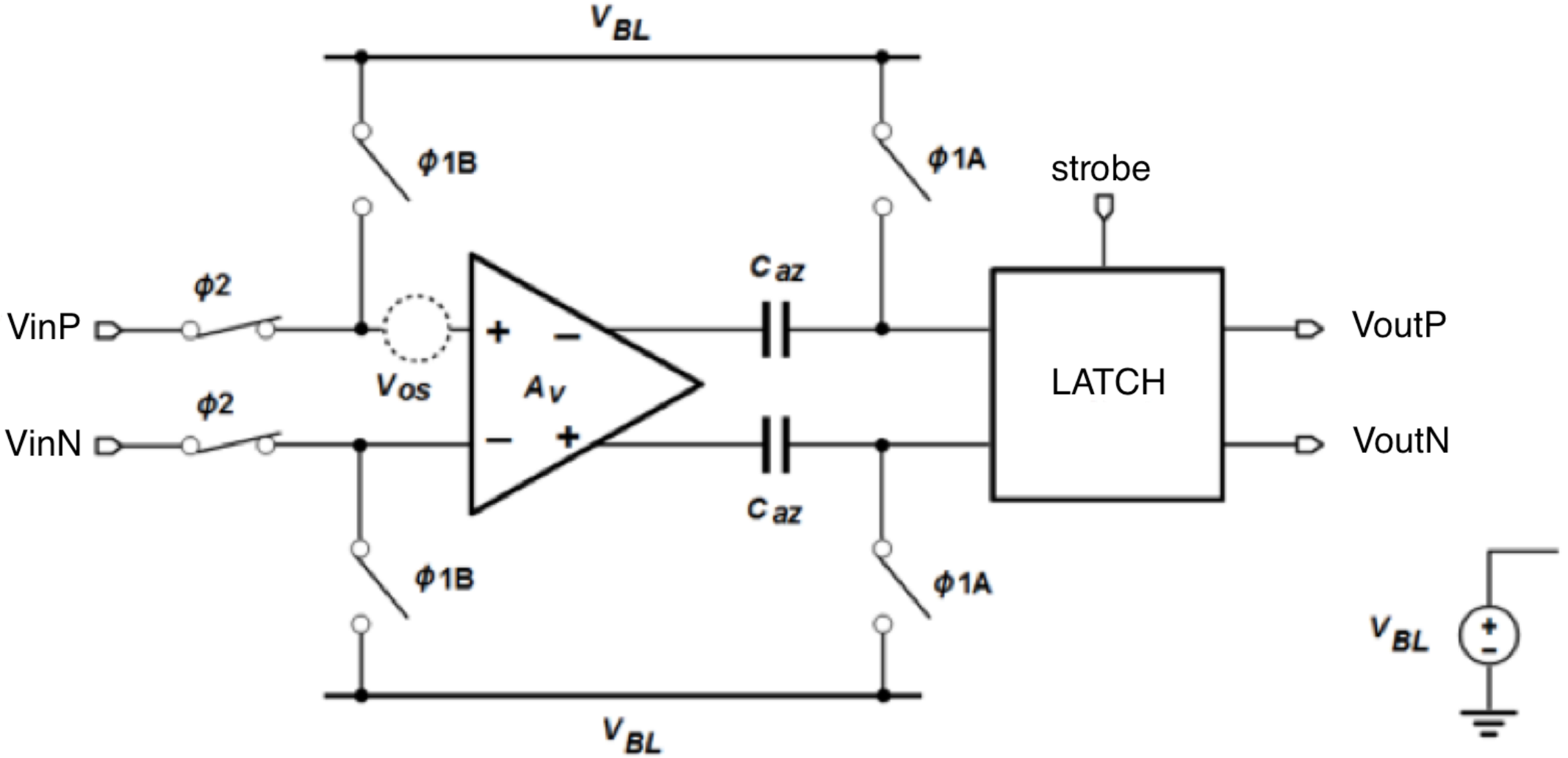
- Preamp: single stage Charge Sensitive Amplifier (CSA) with Krummenacher feedback
- Synchronous discriminator AC coupled to the first stage
- Offset compensation done with capacitors (no trimming needed)
- Fast Time-over-Threshold (ToT) using the latch as a local oscillator (up to 800 MHz)
- Total current consumption: ~ 5 μA

Charge Sensitive Amplifier



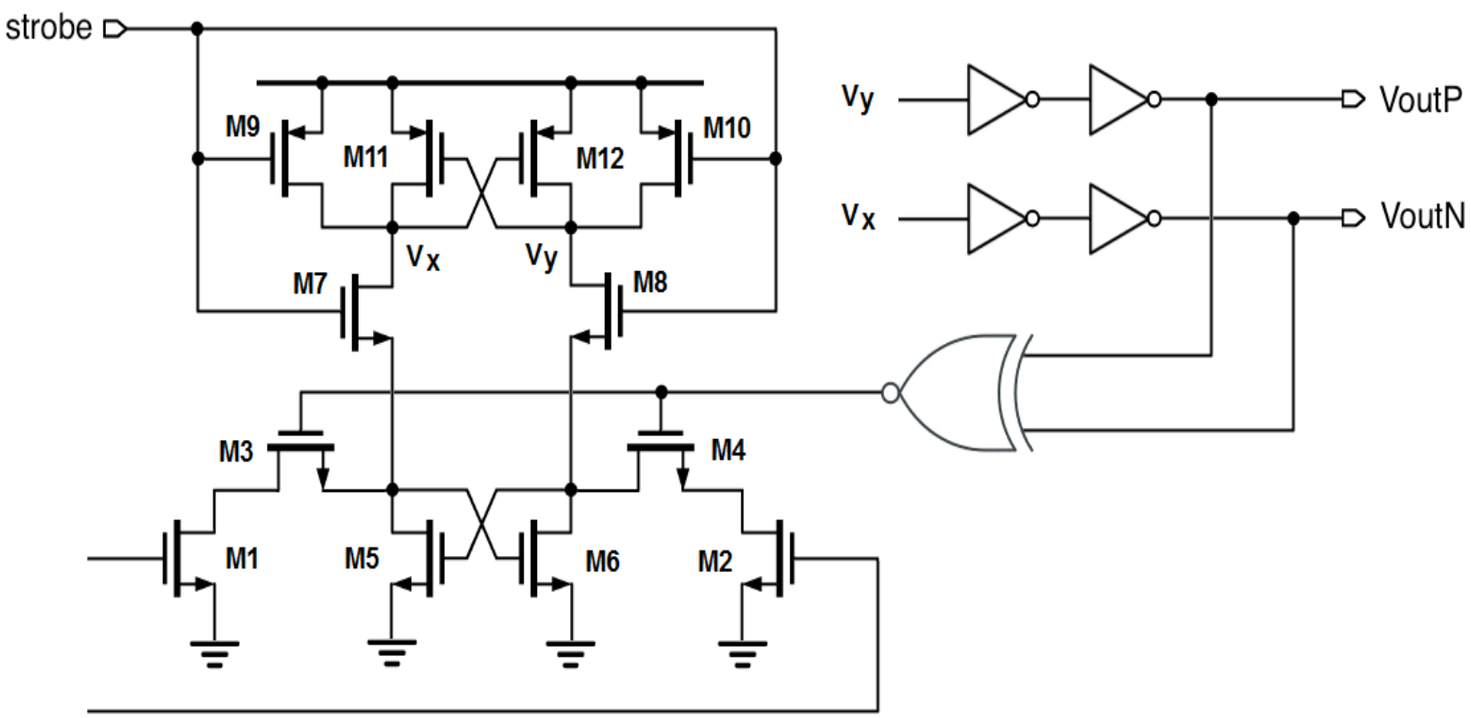
- Cascode with current splitting and source follower
- Two selectable values of feedback capacitance
- Open-loop gain = 1000 (60 dB)
- Current consumption ~ 2.5 µA
  - IbiasP1 = 0.5 µA
  - IbiasP2 = 1.5 µA
  - IbiasSF = 0.5 µA

Comparator



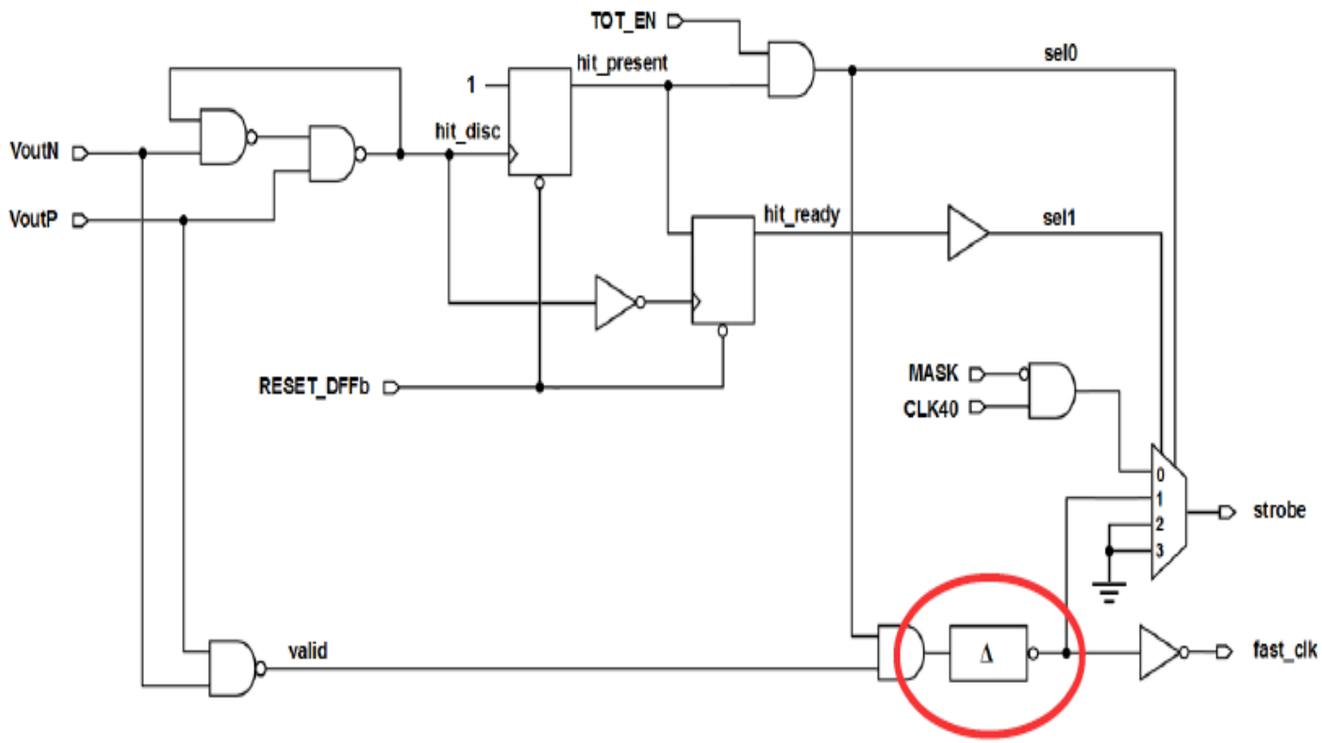
- Differential amplifier offset compensation done with capacitors (“auto-zeroing”)
  - 100 ns of compensation needed every 100 µs of operation (to cancel the effect of the slow capacitor discharge due to leakage currents)
- Latch designed with small mismatch: no threshold trimming via DAC needed
- Current consumption (static + dynamic) ~ 2 µA

Positive feedback latch

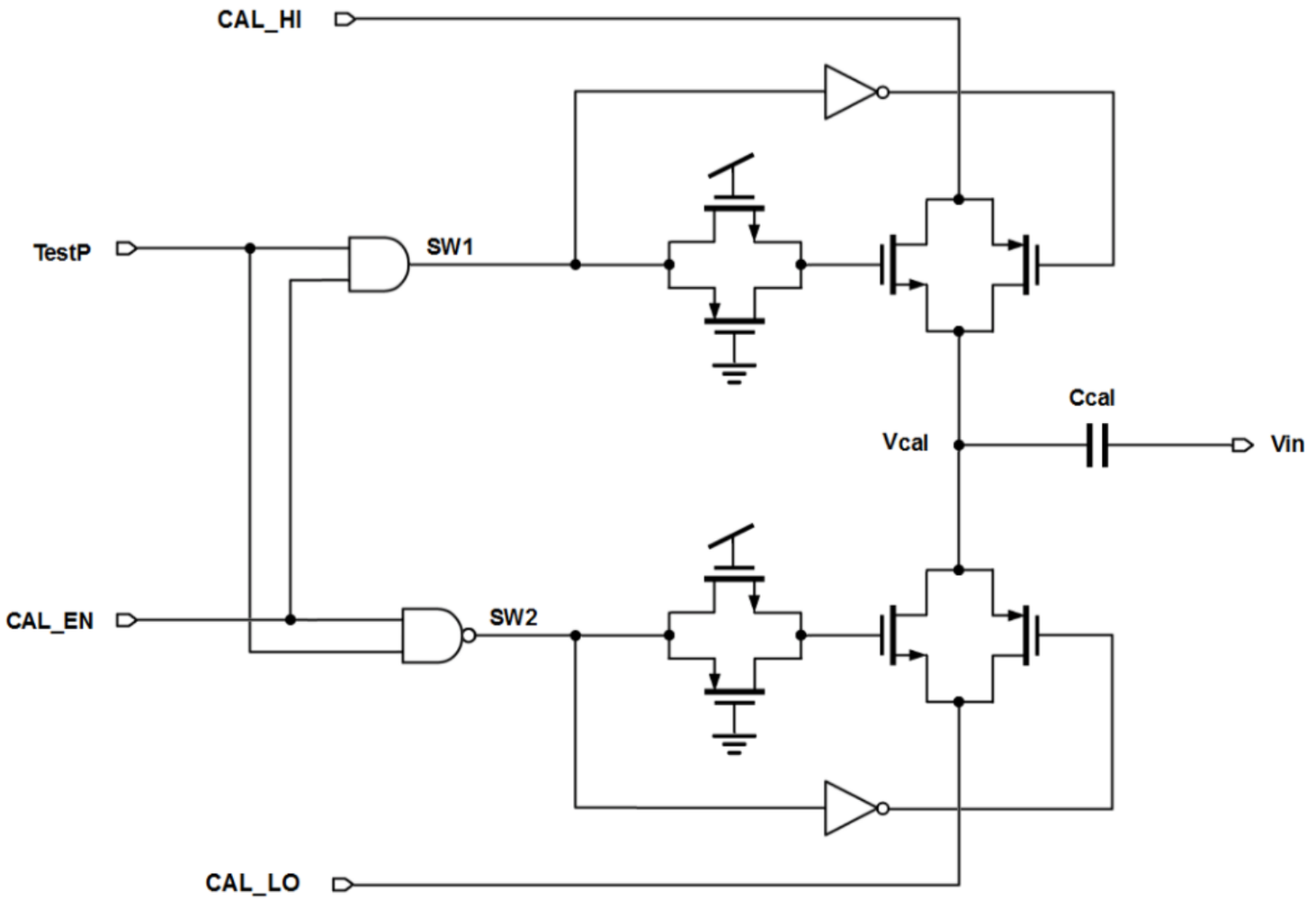


- Synchronous architecture motivations:
  - Particles arrival corresponds with the 40 MHz clock
  - No time-walk effect
  - Low power (dissipation only during transition)

- An asynchronous logic feedback loop can be used to make the latch work as a local oscillator (up to 800 MHz)
  - Allows fast ToT measurements (at least 4-5 bits)
  - Frequency can be tuned using a delay line



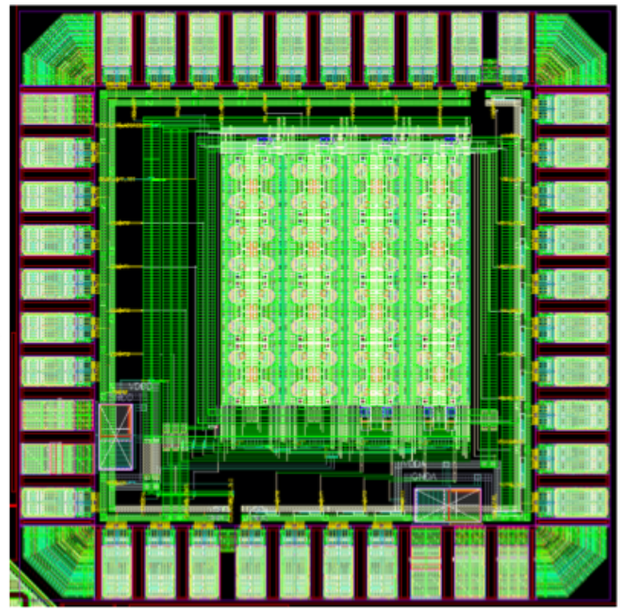
Charge injection strategy



- Local generation of the test pulse based on a DC level
- A switching digital pulse (TESTP) used to inject the signal

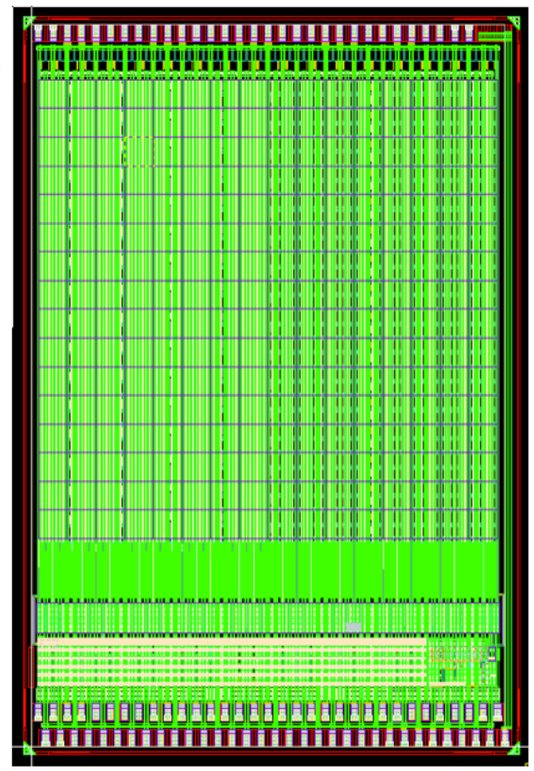
Timeline

- 2014: submission of a **first prototype** called CHIPIX_VFE_1 (8x8 pixel matrix with analog output of CSA and discriminator)



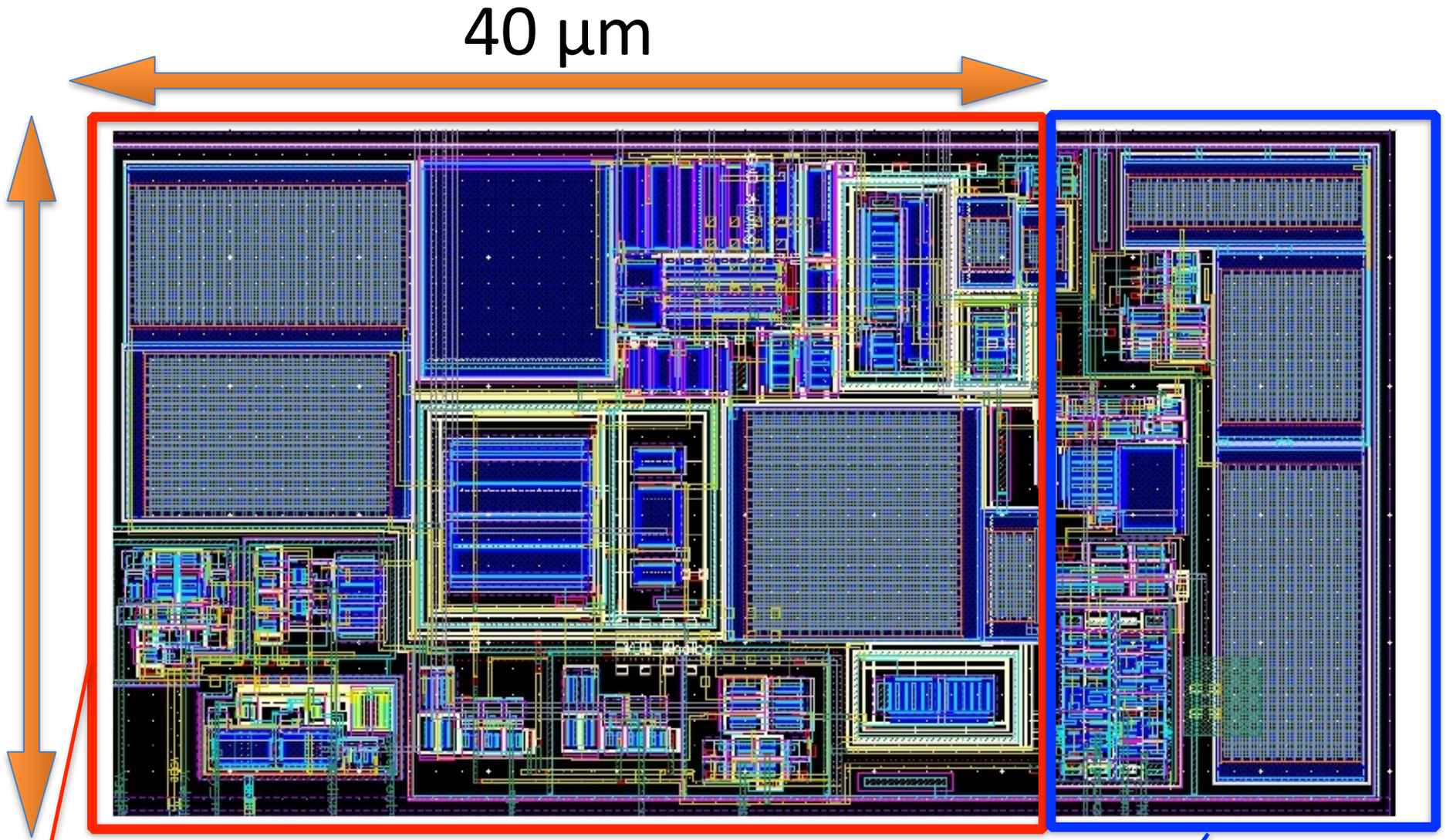
- 2015: submission of a **second prototype** (CHIPIX_VFE_2)
  - Improvements in key areas (gain, threshold dispersion)
  - Irradiated up to **600 Mrad**
  - Measurements presented in this talk

- 2016: CHIPIX65 demonstrator (small ROC with 64x64 pixel matrix and full digital architecture) submitted in July
  - **New version** of the front-end with further improvements included together with the previous one
  - Measurements to be started in October



Talk by Andrea Paternò

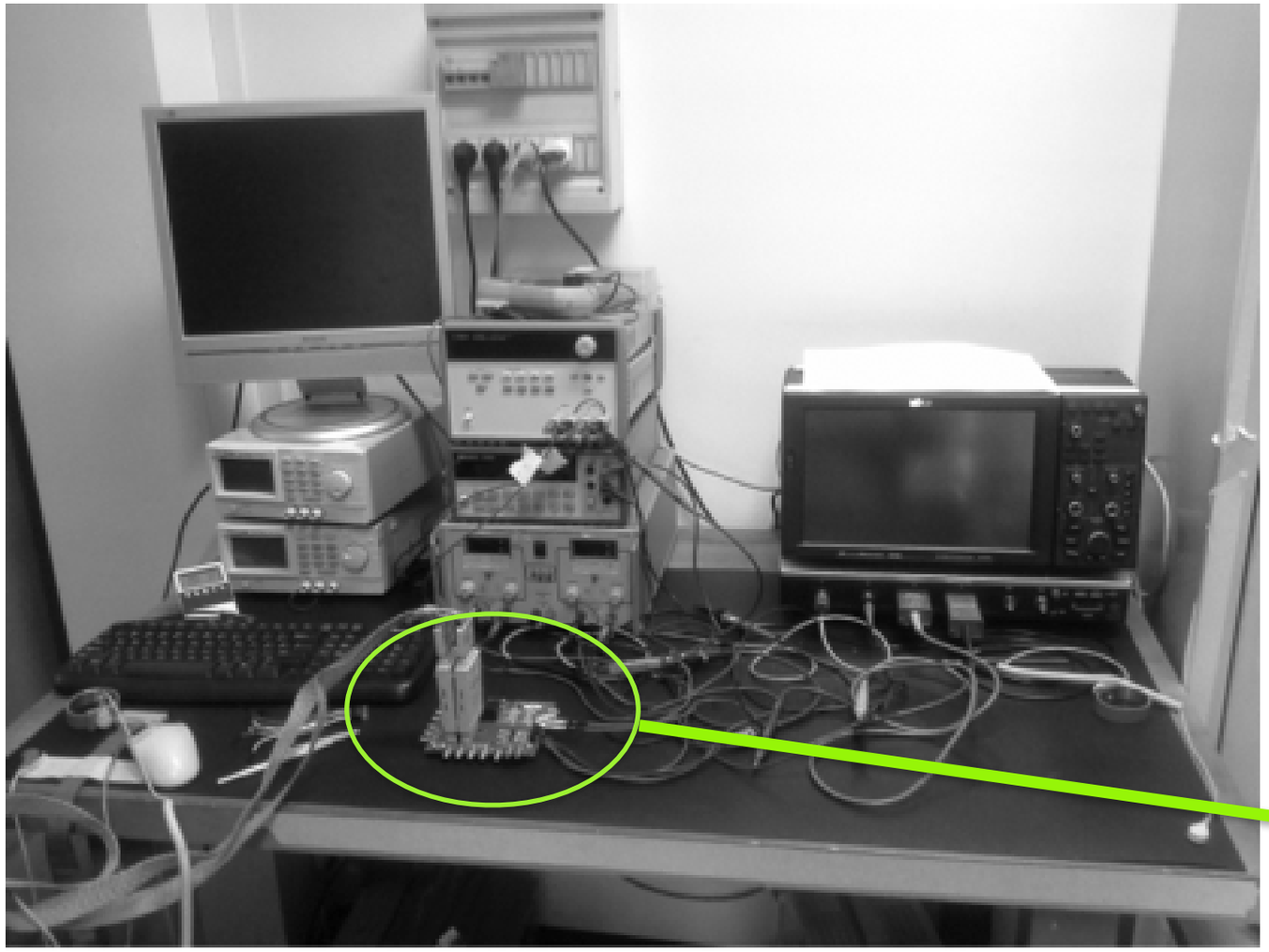
VFE_1 Layout



- CSA + Disc + Calibration circuit -> 26x40 µm^2
- In addition for tests:
  - Different capacitances to emulate the detector
  - Analog buffer in order to see the preamp and comparator output

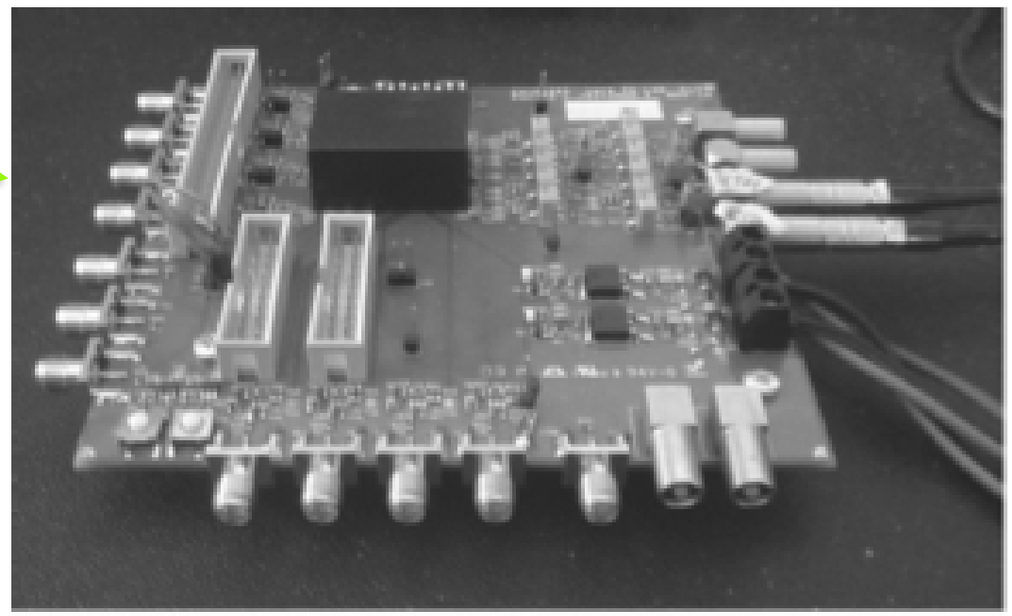
Measurement results

Experimental setup



TEST BOARD

(Designed by Luca Pacher and Francesco Rotondo)

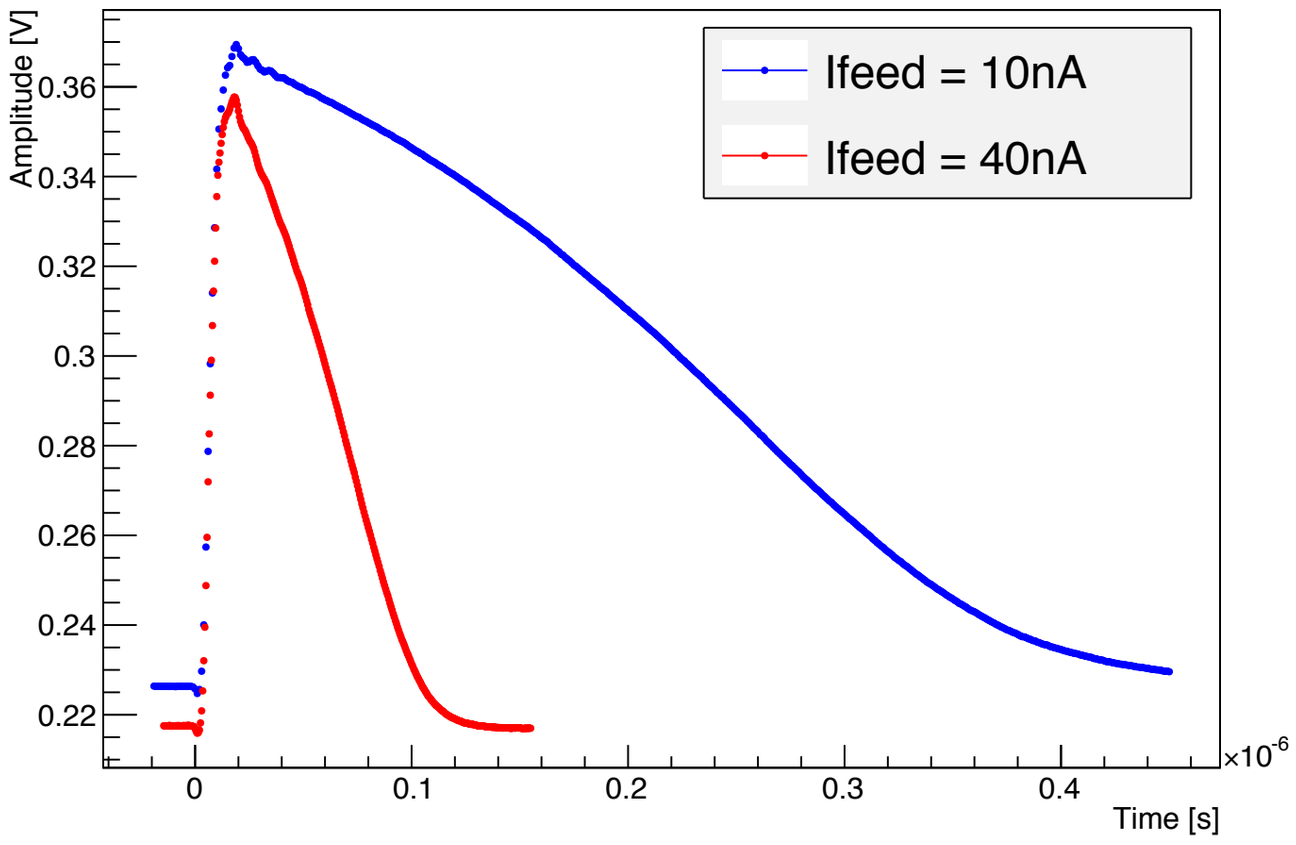


- Test board
- Power supplies
- Digital pattern generator
- Oscilloscope
- Analog signals measured with differential active probe

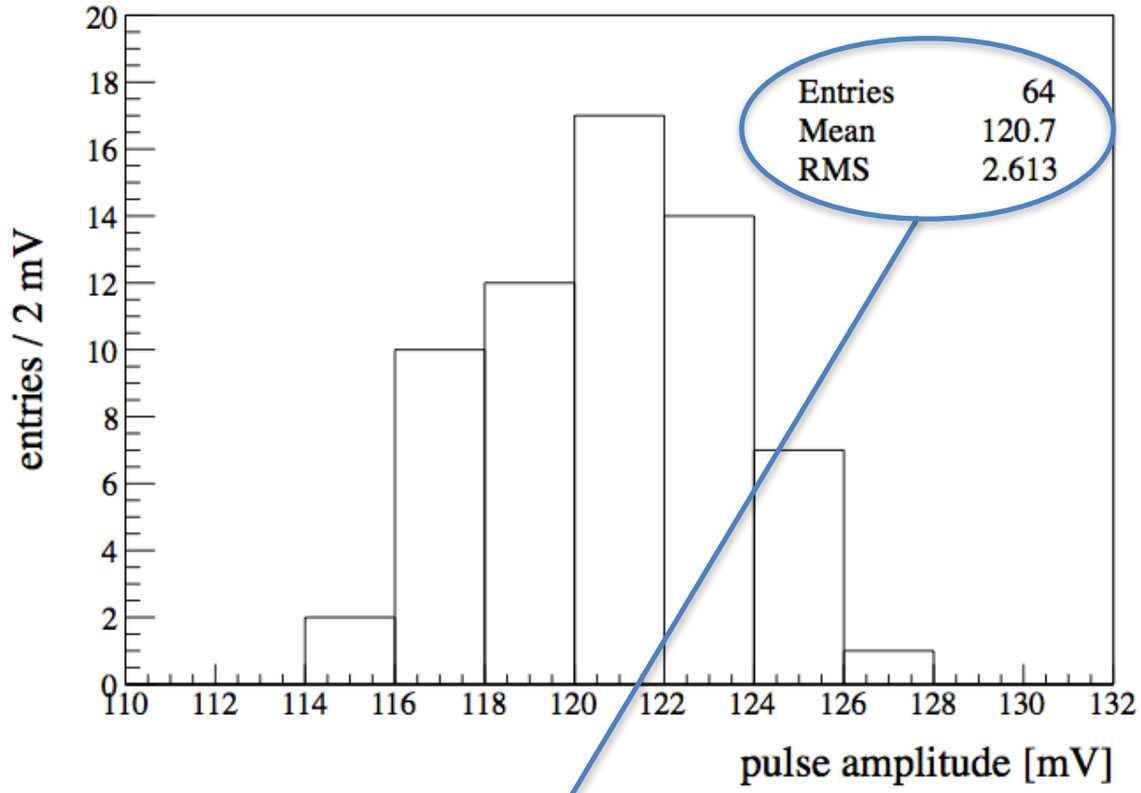
Gain

- ToT duration for a fixed signal can be regulated using the feedback current
- As a reference with Qin = 10 ke$^-$, C_{input} = 100 fF:
  - **10 nA** leads to a ToT = 400 ns → **SLOW** mode
  - **40 nA** leads to a ToT = 100 ns → **FAST** mode
- Peaking time ~ 24 ns

Analog signal (oscilloscope)



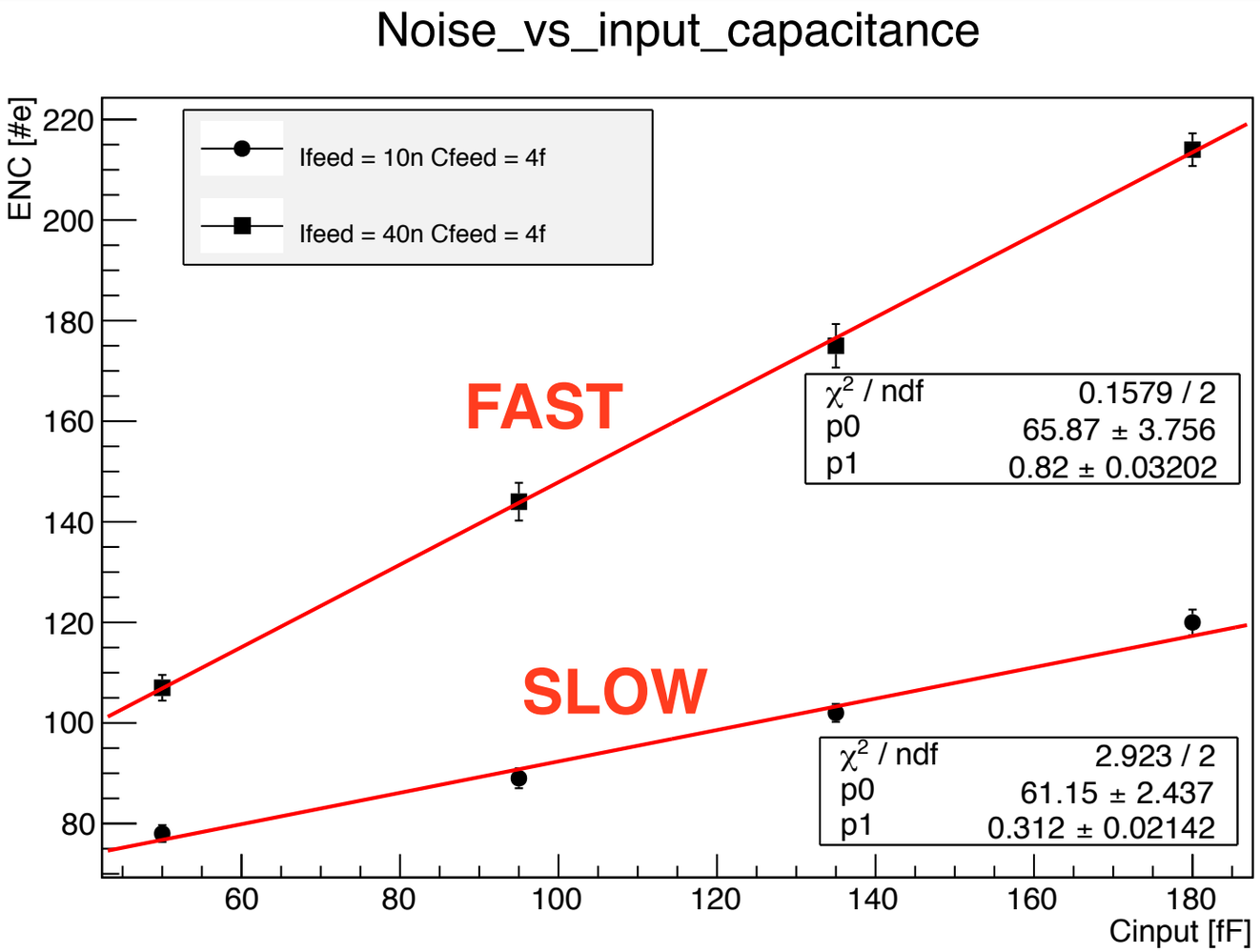
Gain distribution of the 64 pixels (Q_{in} = 6ke$^-$)



Amplitude dispersion below 2.2% RMS

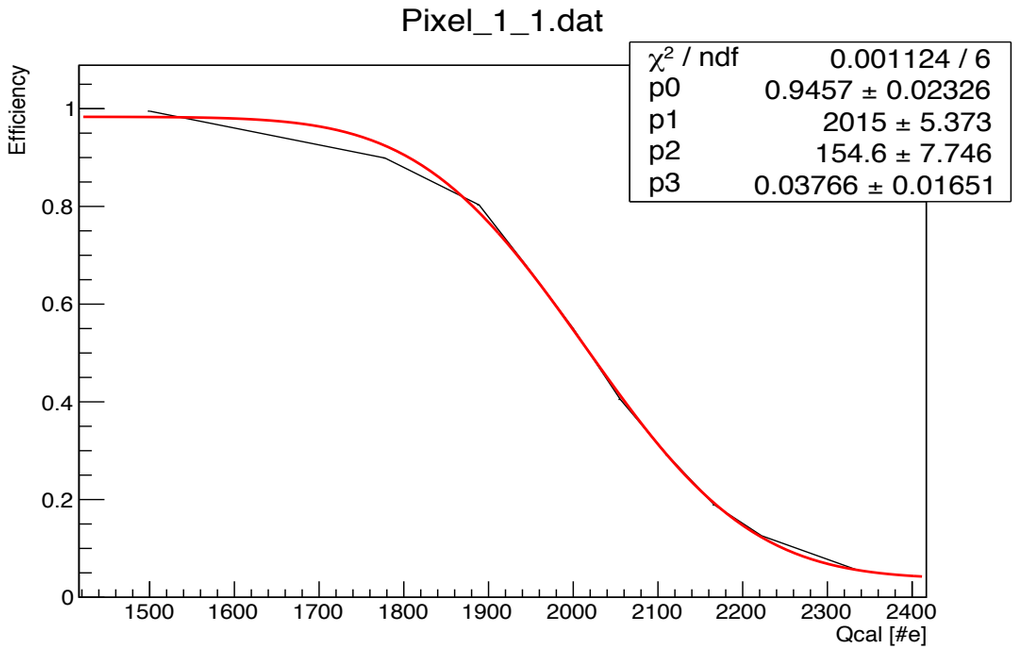
Excellent gain uniformity

Noise



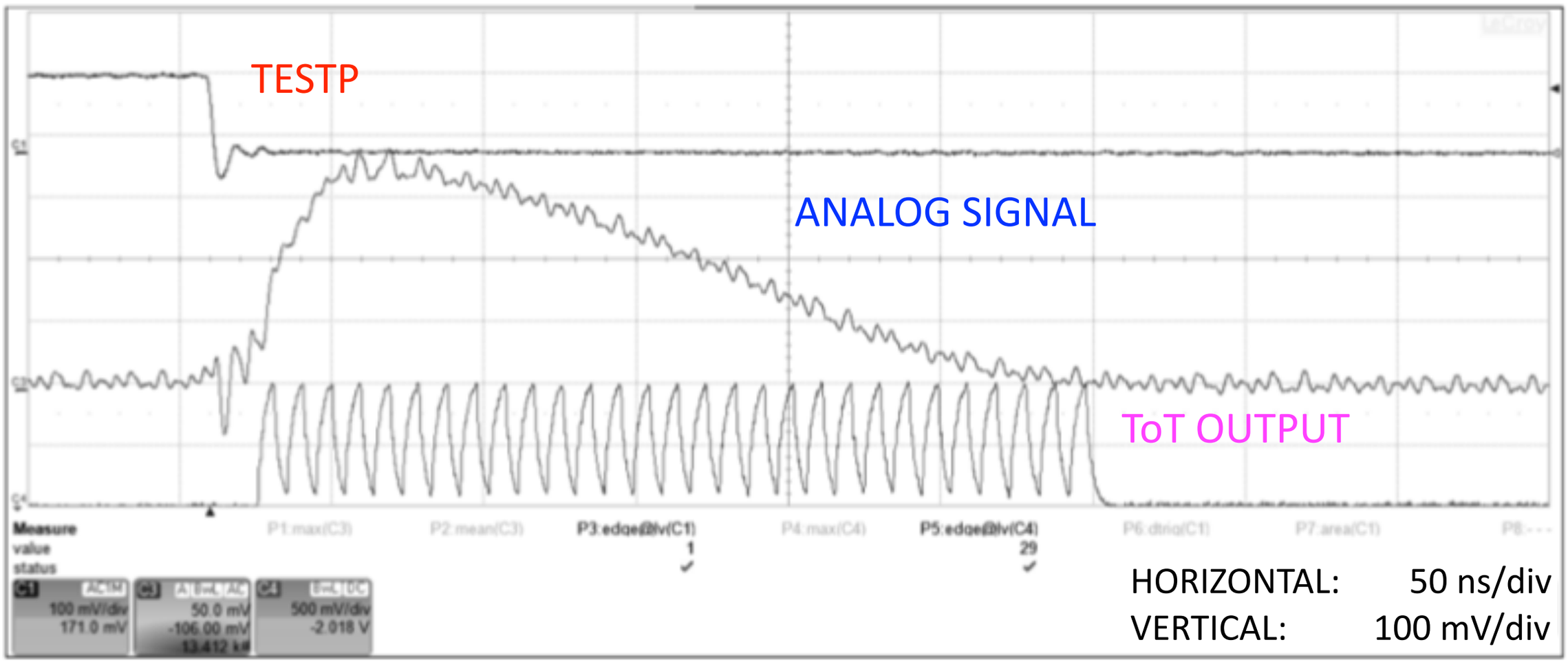
- Noise increases with the feedback current (ballistic deficit)
- Typical sensor capacitance at HL-LHC → 50 fF
- Threshold = 1000 e^- ⇒ Around 7σ of the noise

- Noise measured using the S-curve technique
- Taken at latch input (CSA + diff. amp. contributions considered)
- Linear trend of the Equivalent Noise Charge vs input capacitance as expected



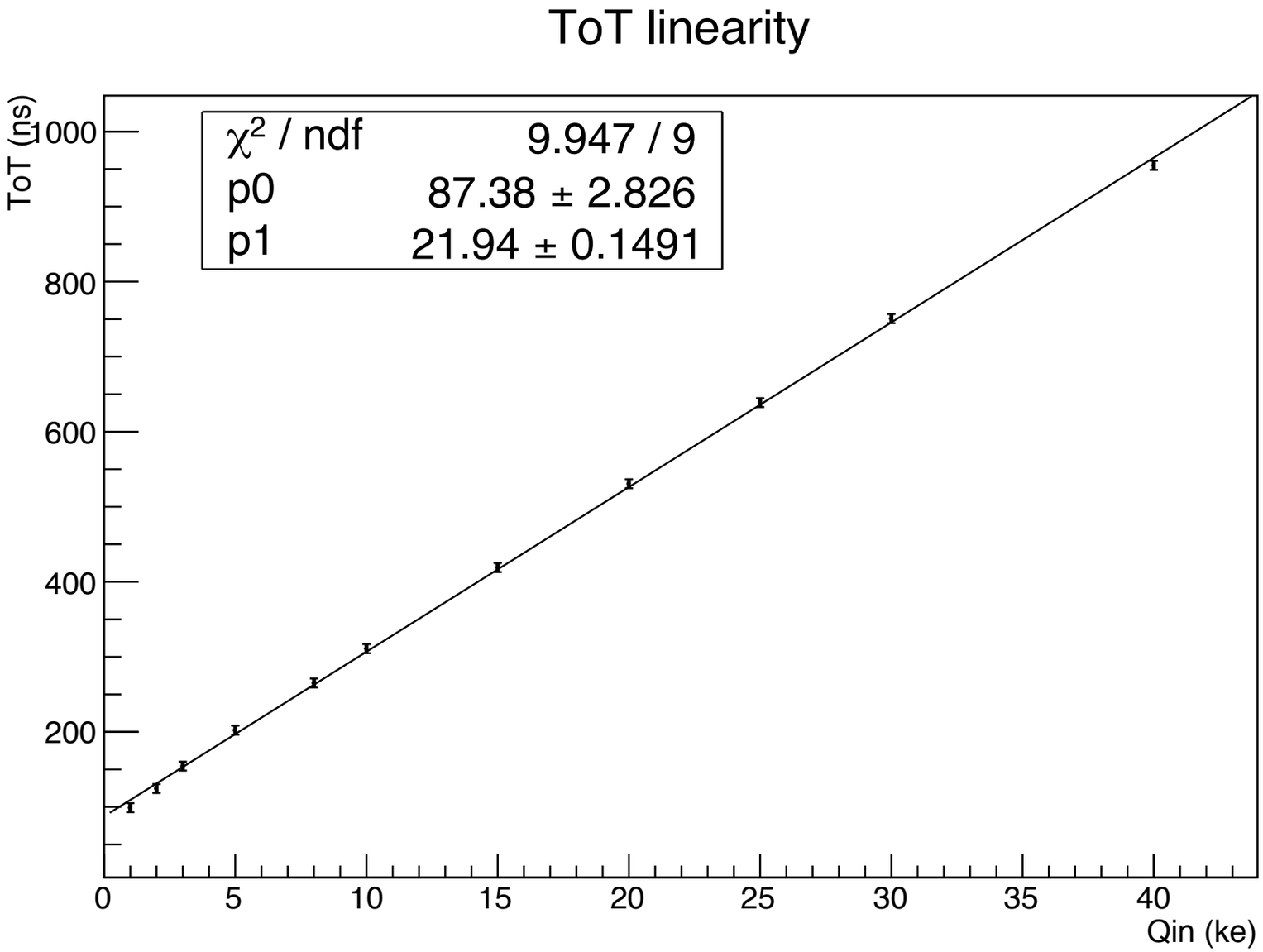
Comparator results

C_{input} = 100 fF Input signal 10 ke^- Threshold ≈ 1000 e^-



- Oscillator @ 100 MHz
- Time duration of the ToT output compatible with HIT in binary mode
- In the present version, oscillation speed can be tuned up to 500 MHz, but set-up bandwidth is limited to about 100 MHz

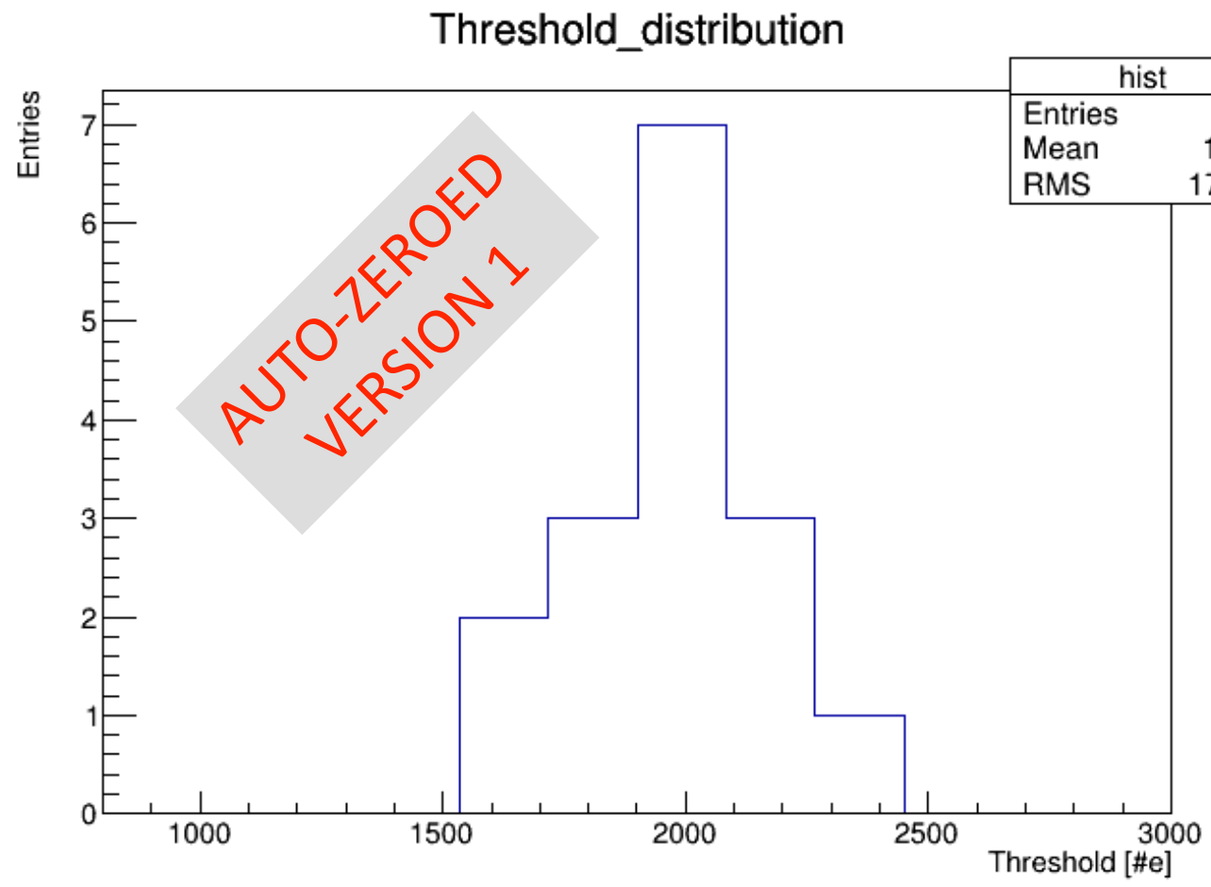
ToT linearity

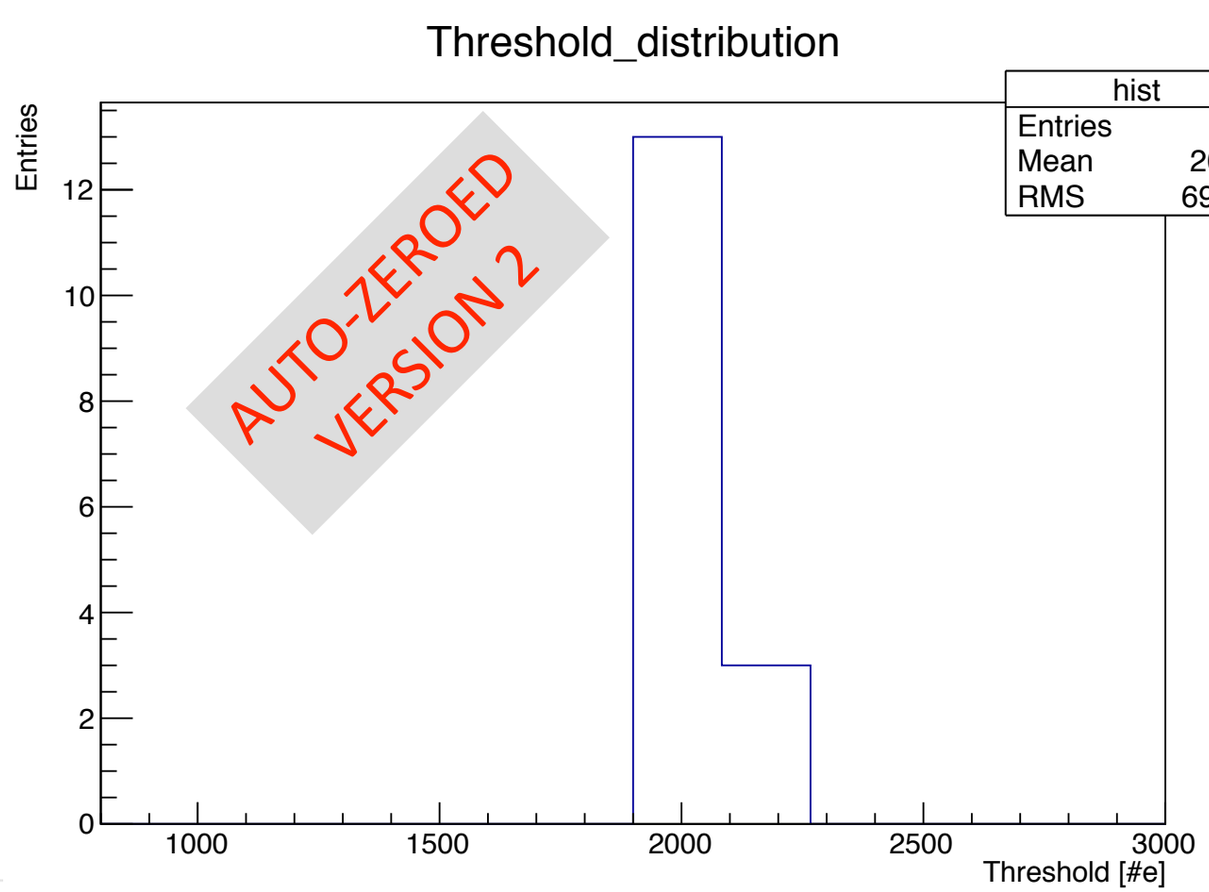


Ifeed = 15 nA in this measurement

- A MIP signal corresponds to around 10 ke$^-$
- The maximum signal of interest is 30 ke$^-$
- ToT is linear up to (at least) 40 ke$^-$
  - The whole input range covered

Residual threshold dispersion





Significant improvement wrt the first version

- In agreement with the reduction of the latch dynamic offset implemented in the second prototype
- The threshold RMS decreases from 174 e^- to 70 e^-
- RMS uncompensated = 273 e^-

Irradiation results

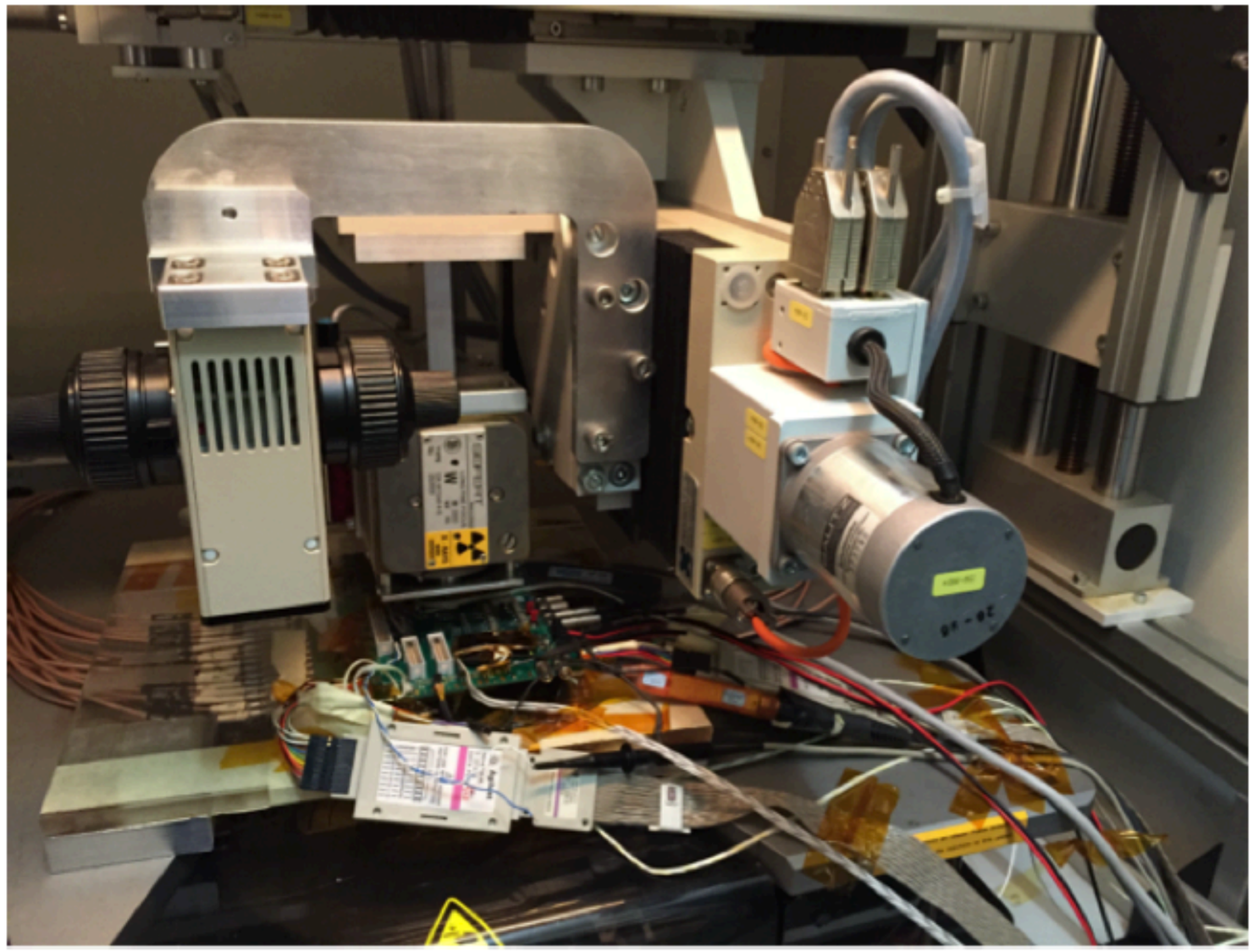
Irradiation procedure

- Made at CERN x-ray machine: thanks to F.Faccio, S.Michelis for availability

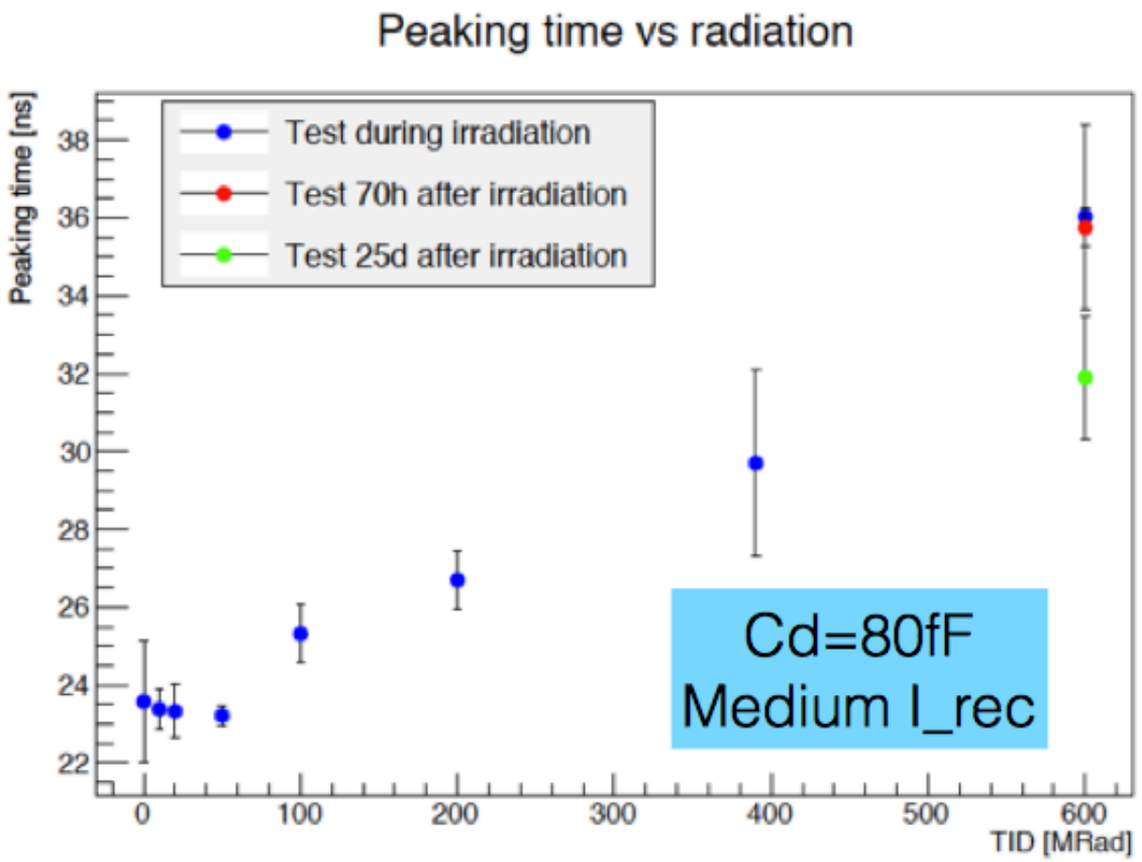
- **Chip powered, biased, clocked, readout active**: as during HL_LHC

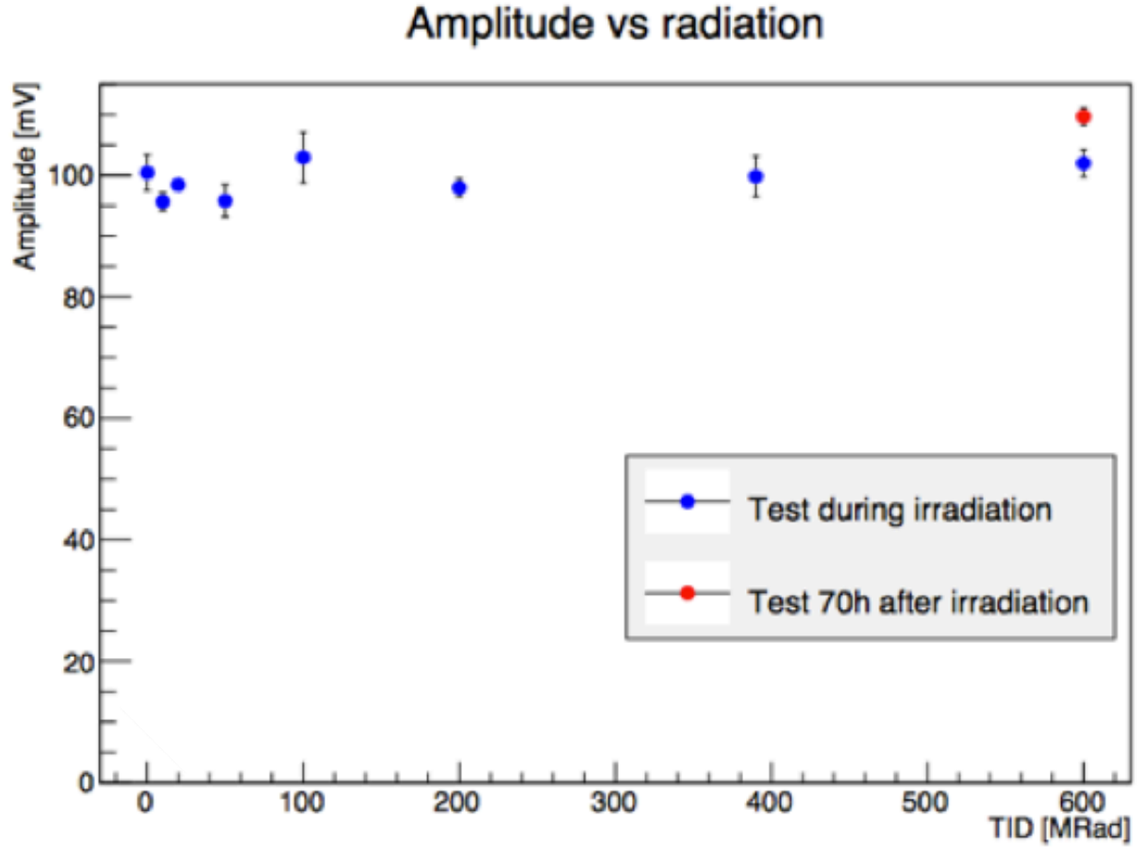
- Room temperature: worst case TID up to 600 Mrad

- In all these measurements
  - Cfeed = 4.2 fF
  - Ifeed = 20 nA



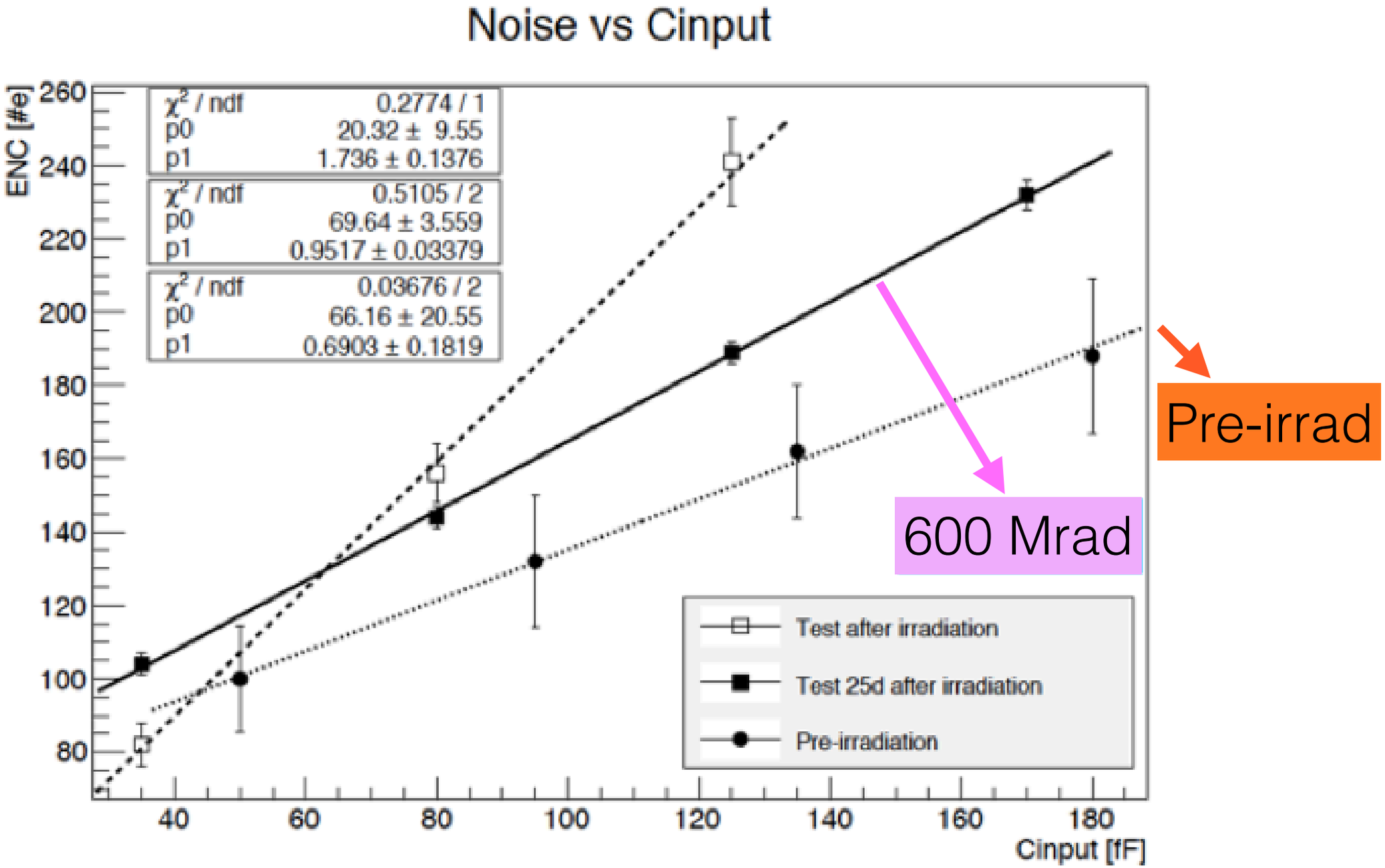
Analog parameters





- Peak time for Cd=80 fF: increase with TID then partial recovery
- Amplitude: no relevant variation seen

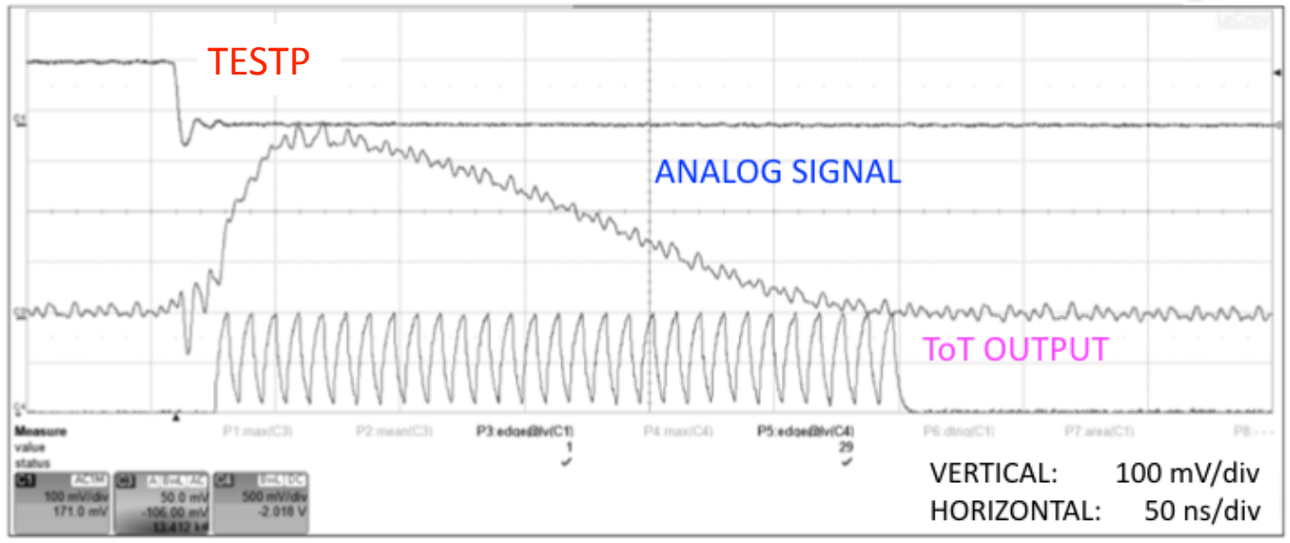
Noise



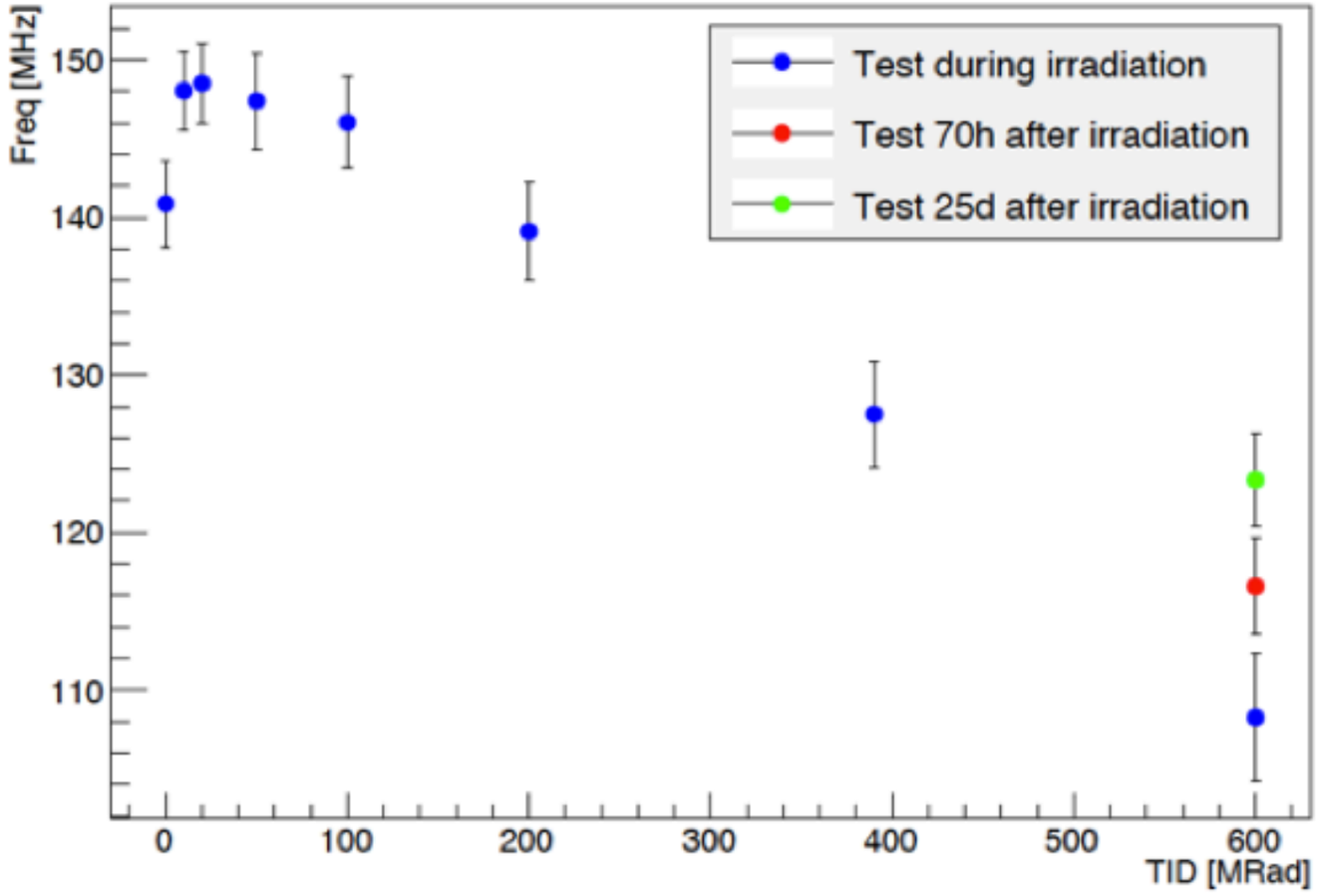
- For Cdet = 50 fF increase of 10% (measured in low-gain configuration)

ToT frequency

- Local oscillator set to 140 MHz
- Slow down with TID
- Partial recovery with time (annealing)
- Freq_rms ~ 1.8%
- Reminder: freq. can be set to higher values

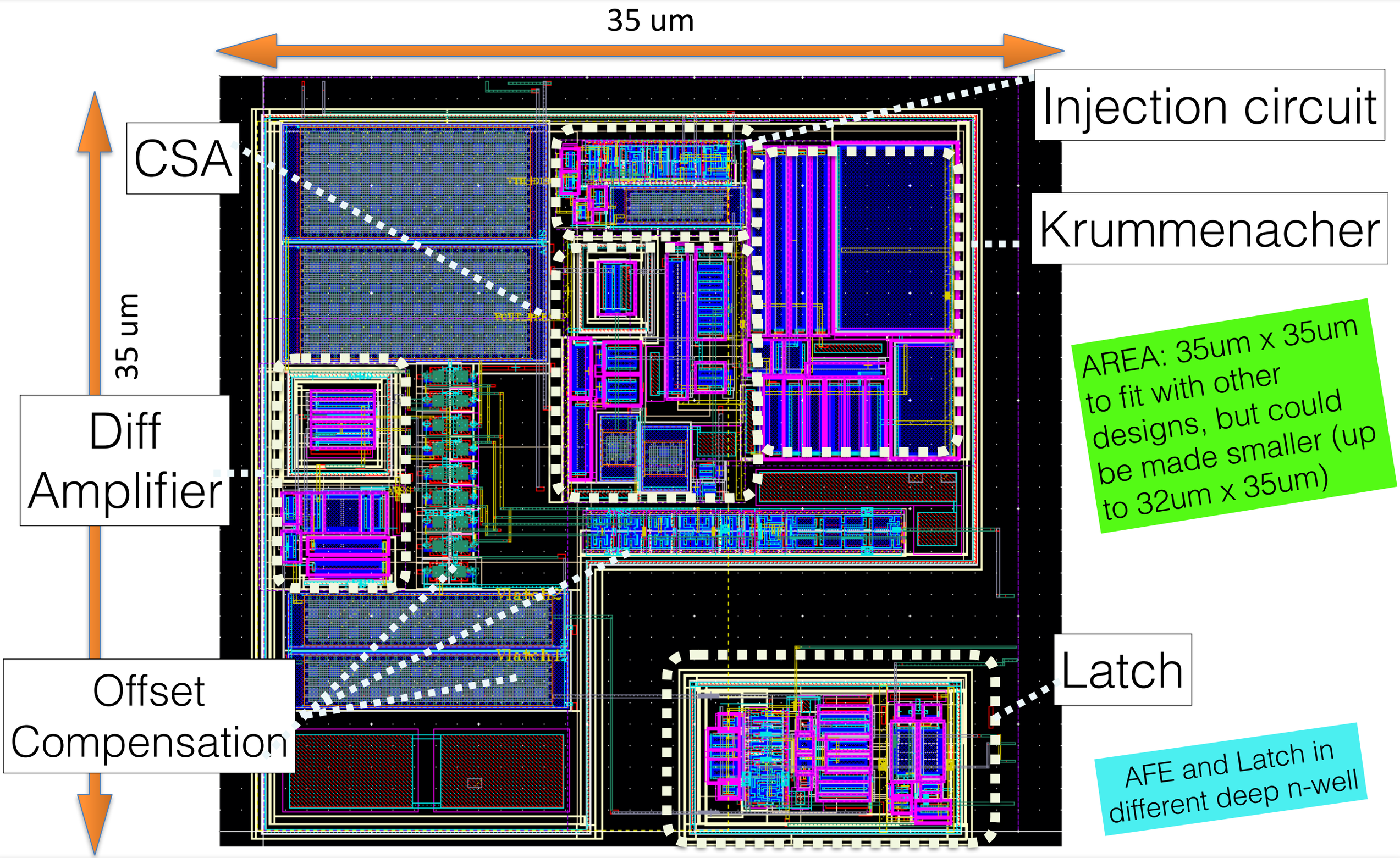


ToT frequency vs radiation

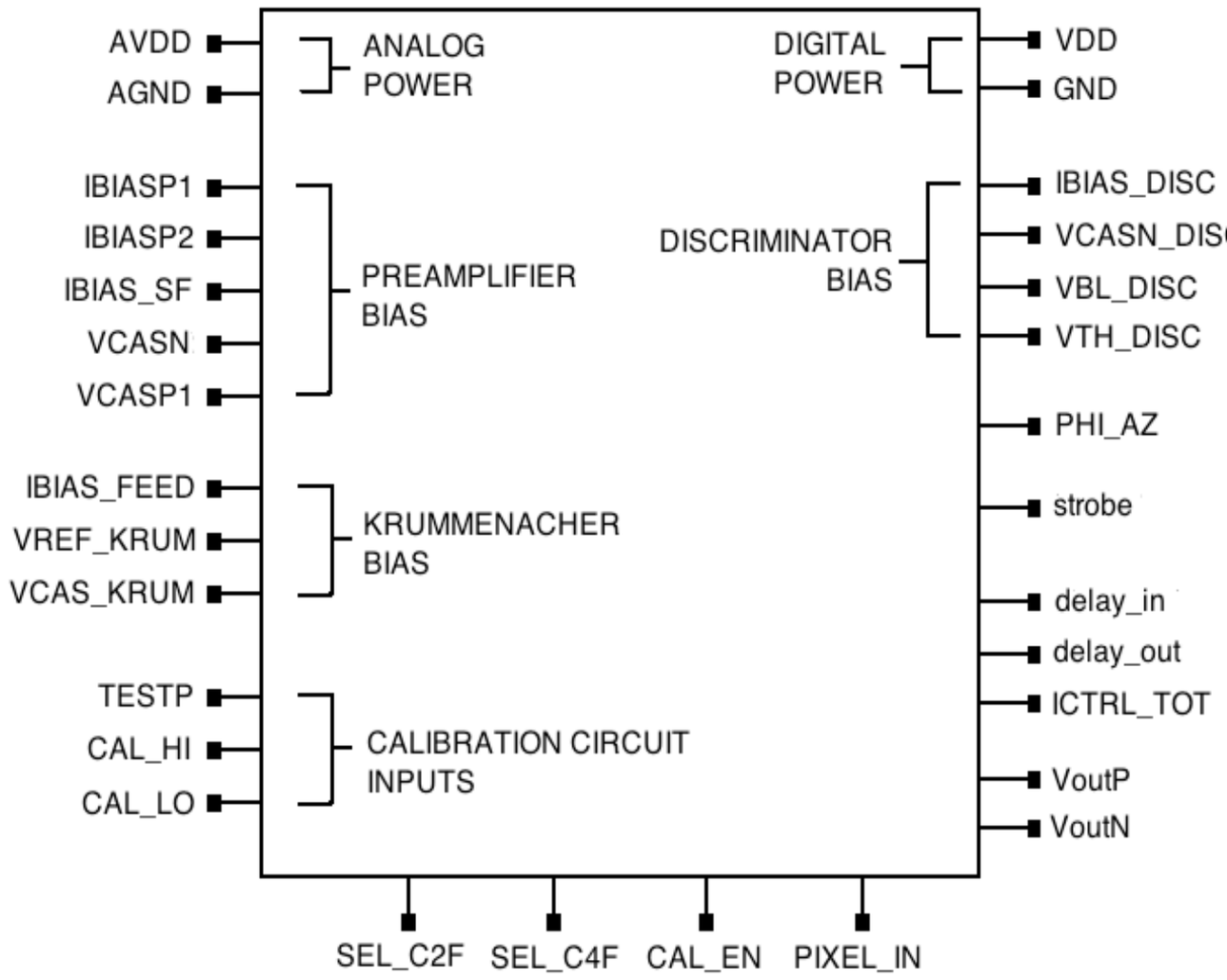


New version for the CHIPIX demonstrator

Layout


35 um
35 um
CSA
Diff Amplifier
Offset Compensation
Injection circuit
Krummenacher
Latch
AREA: 35um x 35um to fit with other designs, but could be made smaller (up to 32um x 35um)
AFE and Latch in different deep n-well

Analog FE interface



- The bias cells needed to provide the currents have been included in the prototypes

List of bias currents

PIN name	Description	Nom value
IBIASP1	Preamplifier main branch current	500 nA
IBIASP2	Preamplifier splitting branch current	1.5 µA
IBIAS_FEED	Krummenacher feedback current	10-35 nA
IBIAS_SF	Preamplifier Source Follower current	500 nA
IBIAS_DISC	Differential amplifier current	1 µA

Digital interface

PIN name	Polarity	Description	Default
SEL_C2F	Input	Preamplifier gain selection bit 0: disabled	0
SEL_C4F	Input	Preamplifier gain selection bit 0: disabled	1
CAL_EN	Input	Enables the injection pulse in the pixel	0
TESTP	Input	Charge injection pulse	-
VoutP/VoutN	Output	Latch outputs	-
delay_in/delay_out	Output	Delay line outputs	-

Simulation results

	TT	TT 500 Mrad	SS	FF	SF	FS
Charge Sensitivity (mV/fC)	39.1	40.2	36.3	40.7	37.3	39
ENC rms (e)	83	84	81	86	82	84
Threshold dispersion Qth rms (e)	80					
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ (e)	115					
In-time overdrive (e)	100	100	100	50	100	100
Current consumption (μA/pixel)	3.5 (no latch) 5.3 (total)	3.4 (no latch) 5.2 (total)	3.3 (no latch) 5.2 (total)	4.9 (no latch) 7.5 (total)	3.4 (no latch) 5.4 (total)	3.6 (no latch) 5.8 (total)
Time walk (ns)	9.2	9.0	10.1	8.6	9.4	9.4
Time-over-Threshold	285	290	287	277	281	286

Default values: C_{det} = 50 fF, Threshold = 600 e^-, T = 27°C, C_{feed} = 2.5 fF, I_{feed} = 35 nA

Conclusions

- First version of the synchronous front-end designed and submitted in October 2014 and an improved prototype has been realized in May 2015 (the results shown are based on this one)

- Both chips have been successfully tested during 2015 with very promising results
  - Compliant with the specs
  - Idea of “self-oscillating” comparator for fast ToT measurement works
  - Design proved that there is no need of threshold trimming via DACs
  - Good agreement between simulations and measurements

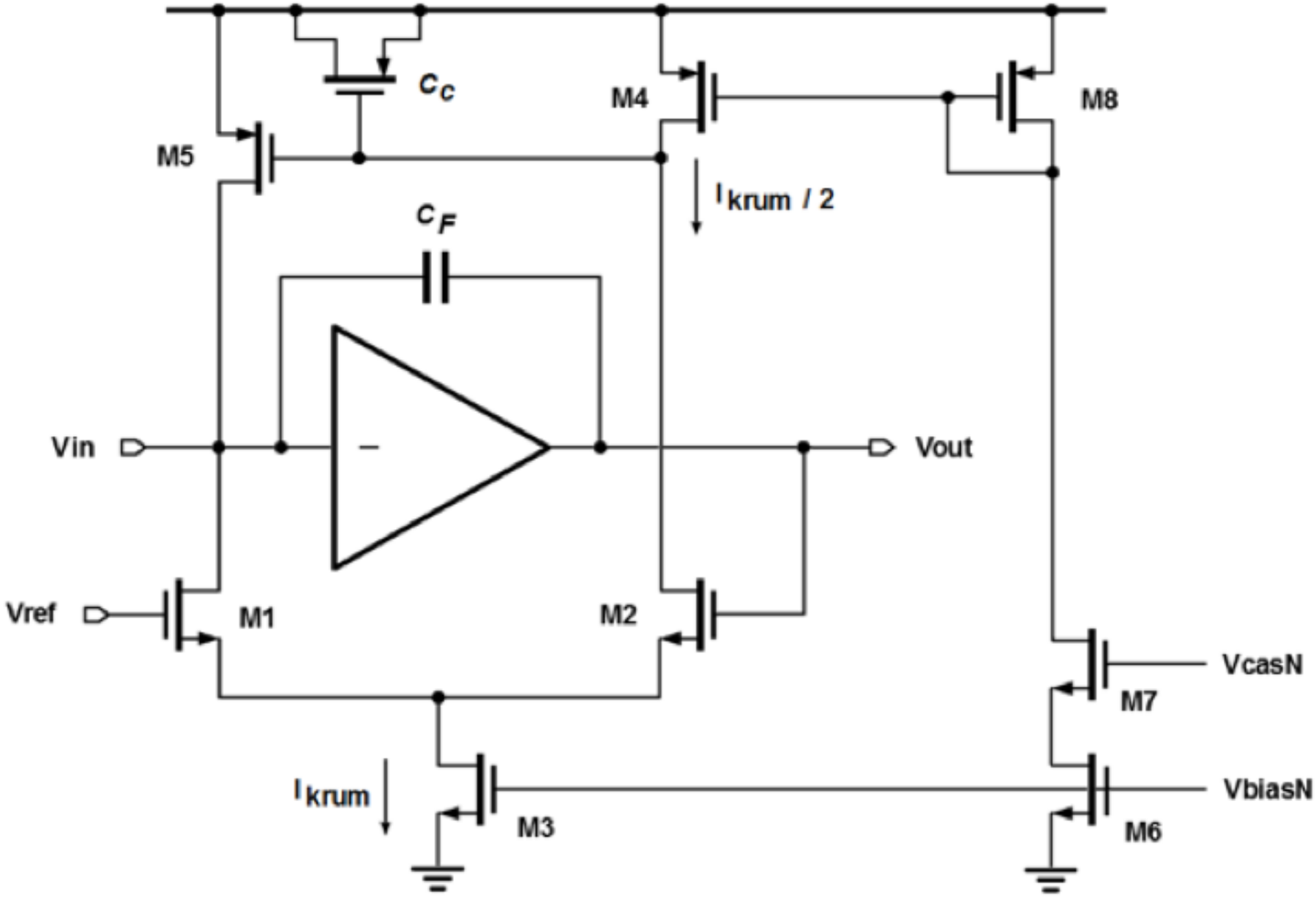
- Radiation tests show that the prototype works still properly with some affordable performance degradations after a TID = 600 Mrad

- A third improved version has been included in the CHIPIX65 demonstrator
  - Submitted on 5th July 2016

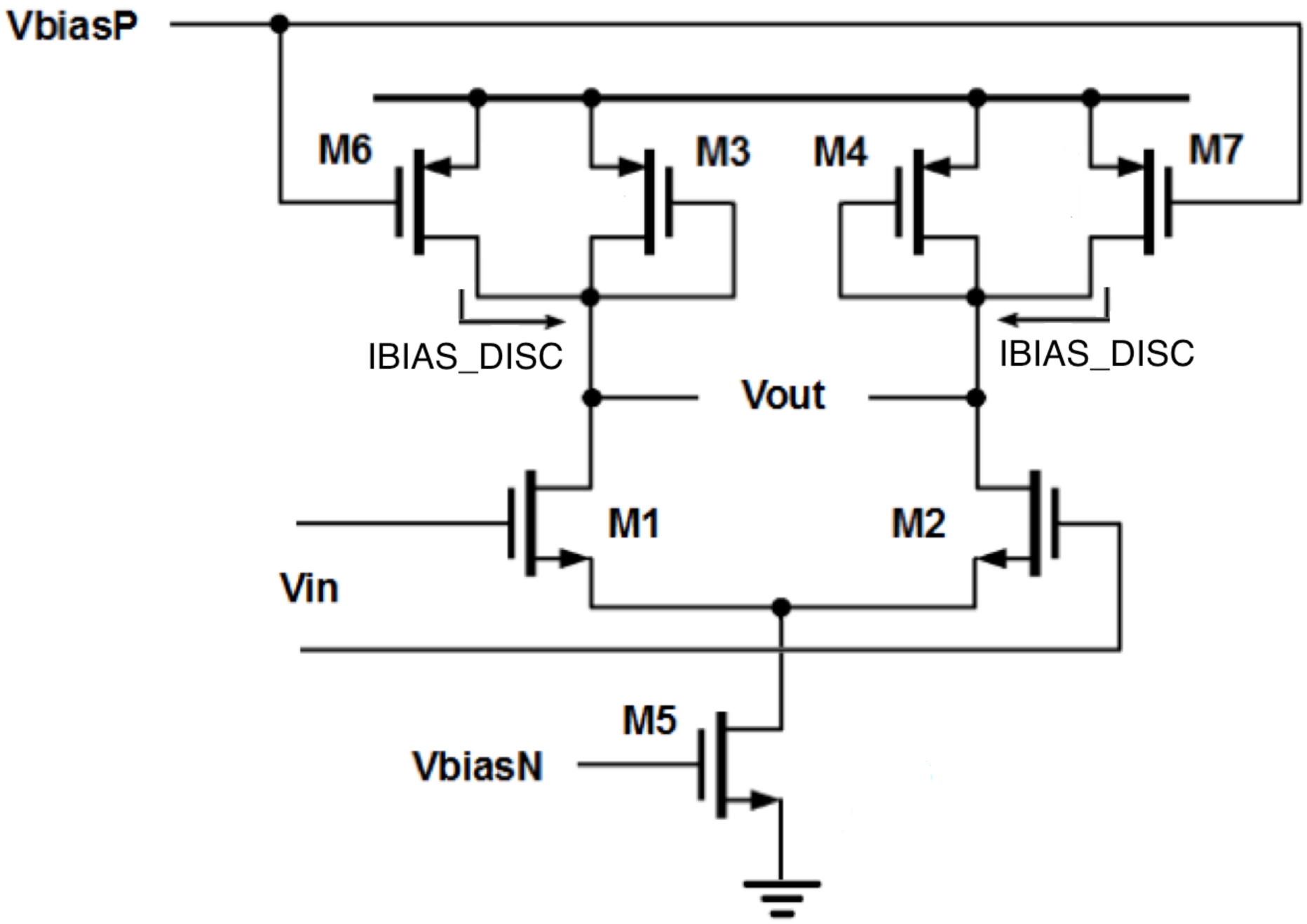
- This design will be one of the very front-end inserted in the RD53A full size prototype

Backup

Krummenacher feedback

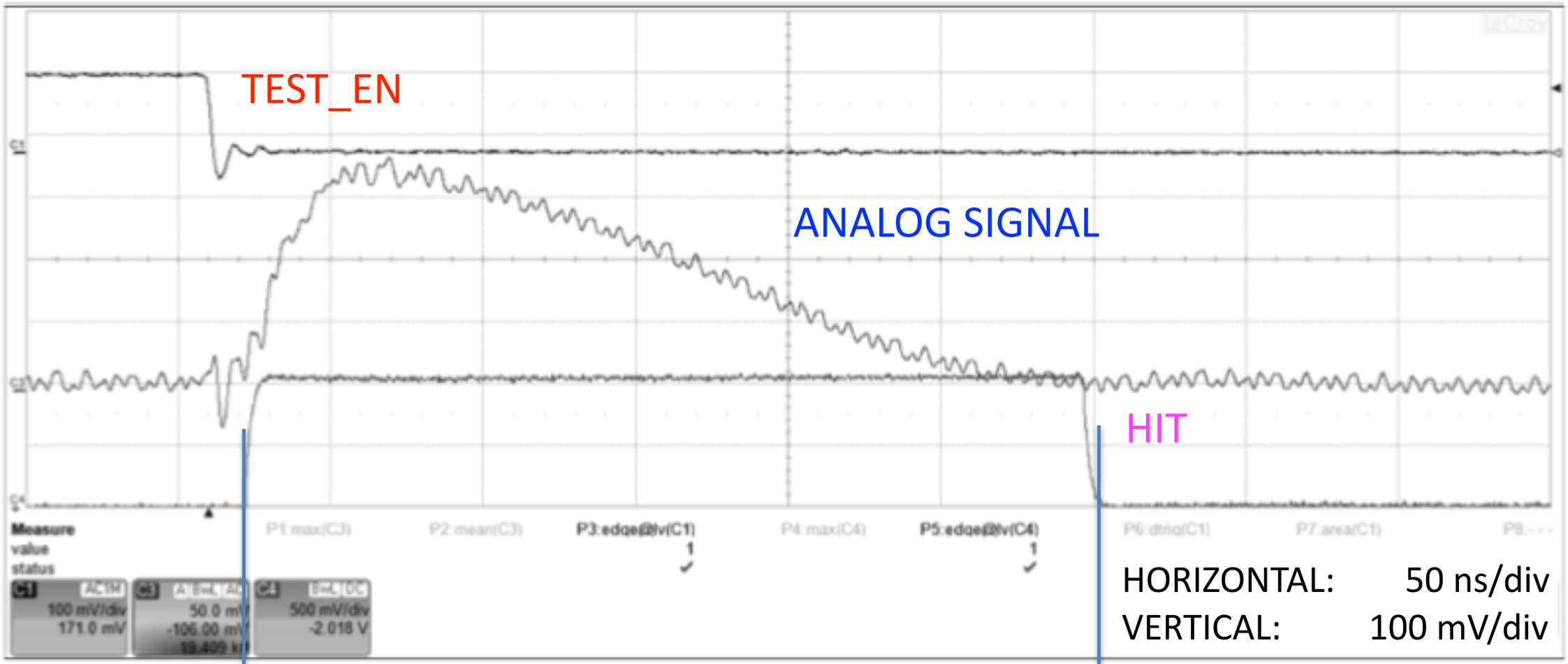


Differential amplifier



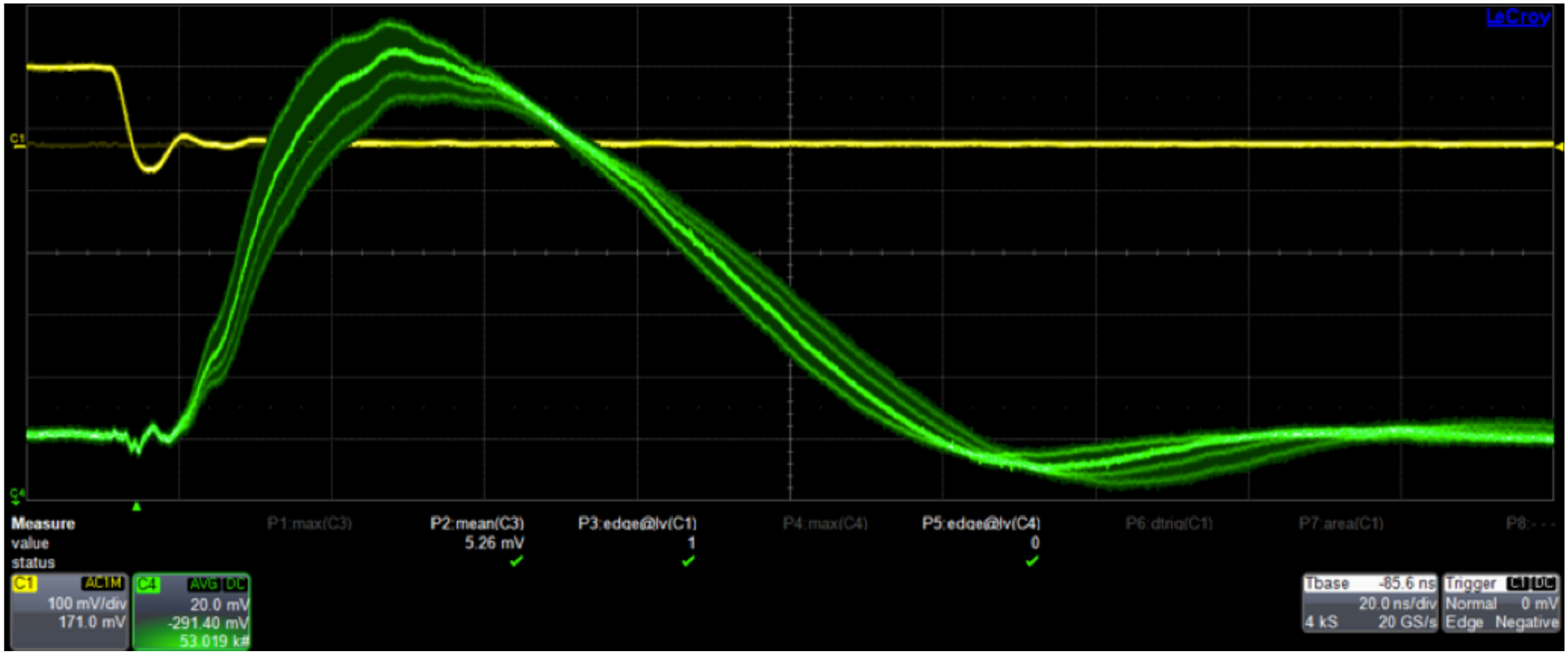
Comparator results

Input signal 10 ke$^-$ Threshold ≈ 1000 e$^-$



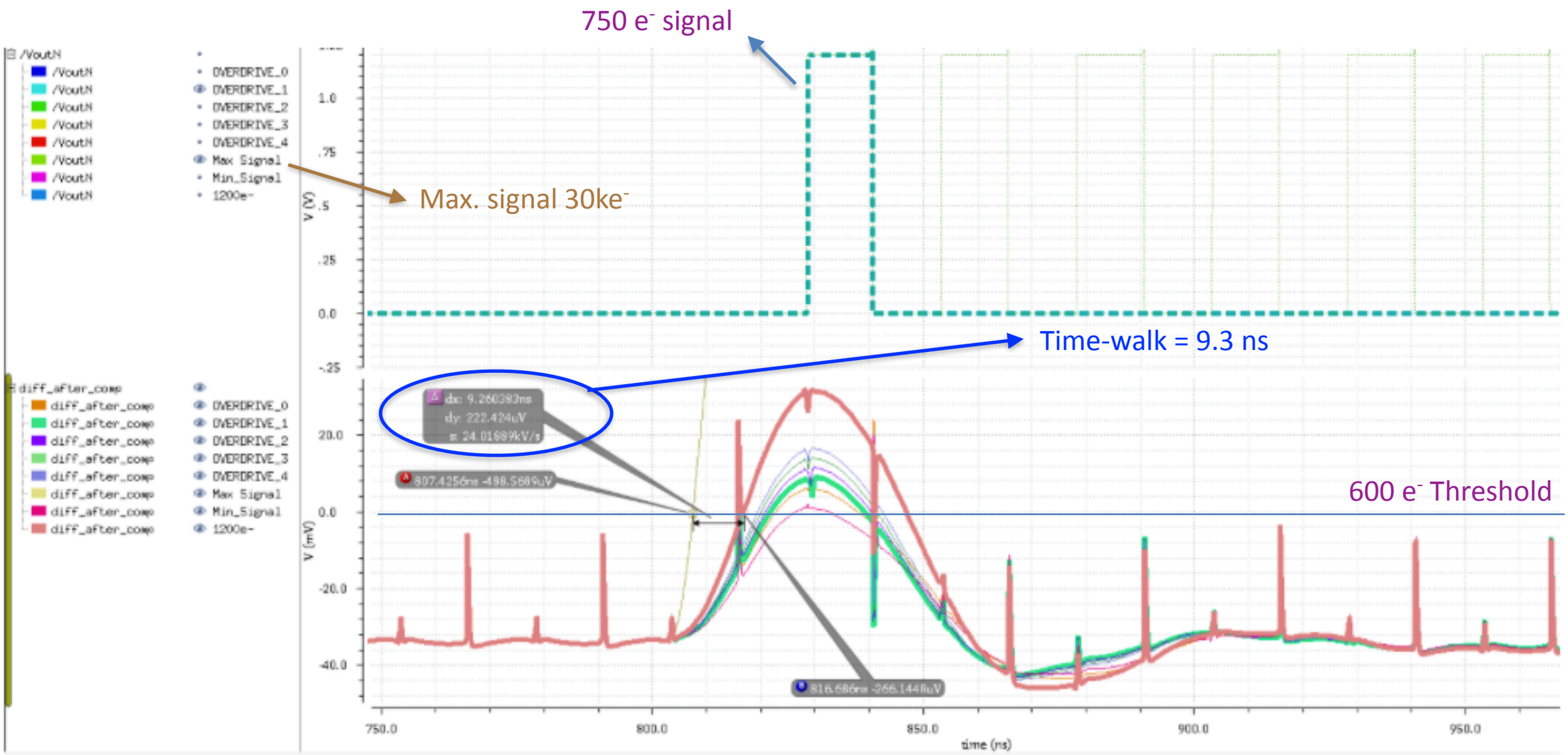
Time duration of HIT multiple of 25 ns (clock period)

Analog signal at the oscilloscope



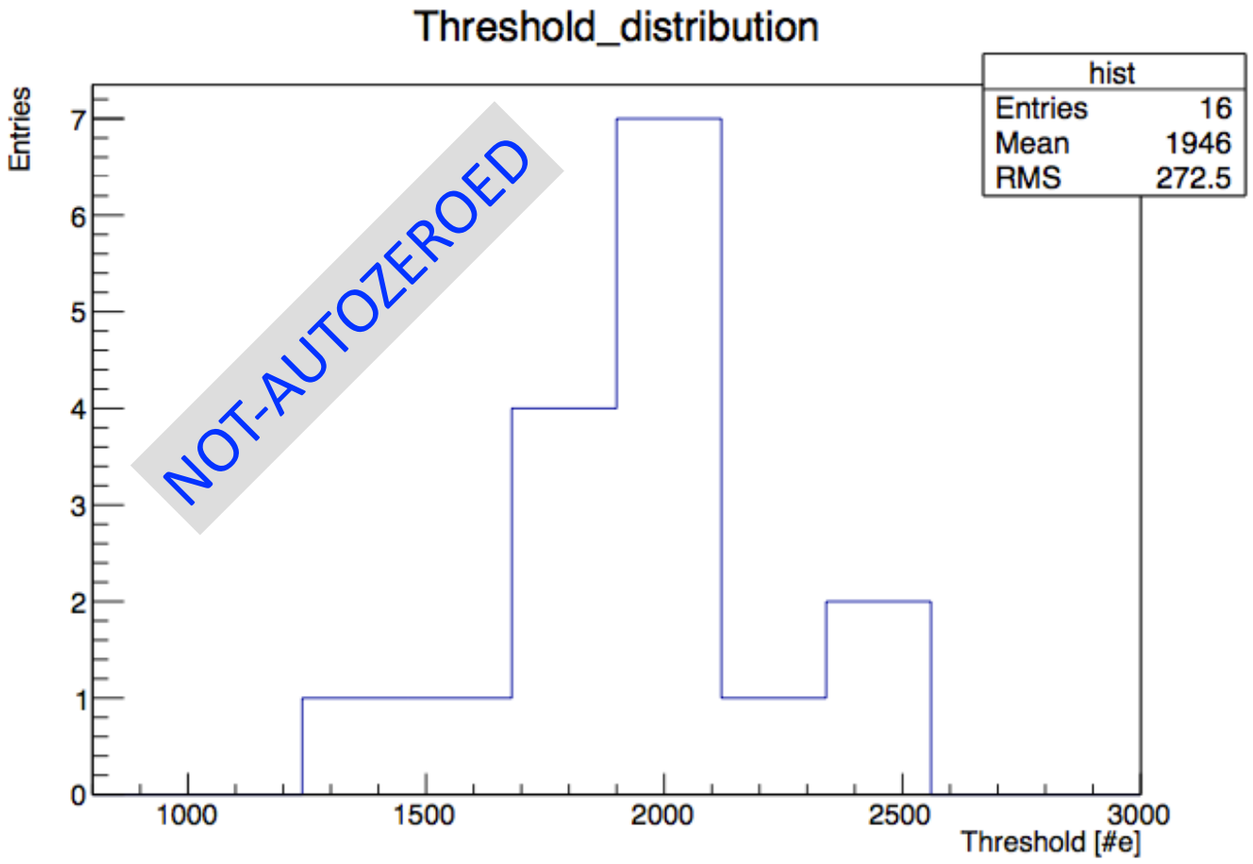
- Measured analog buffer output (averaged shapes):
  - Qin = 10 ke$^-$
  - Cdet = 20/65/105/150 fF
  - ToT ~ 90 ns

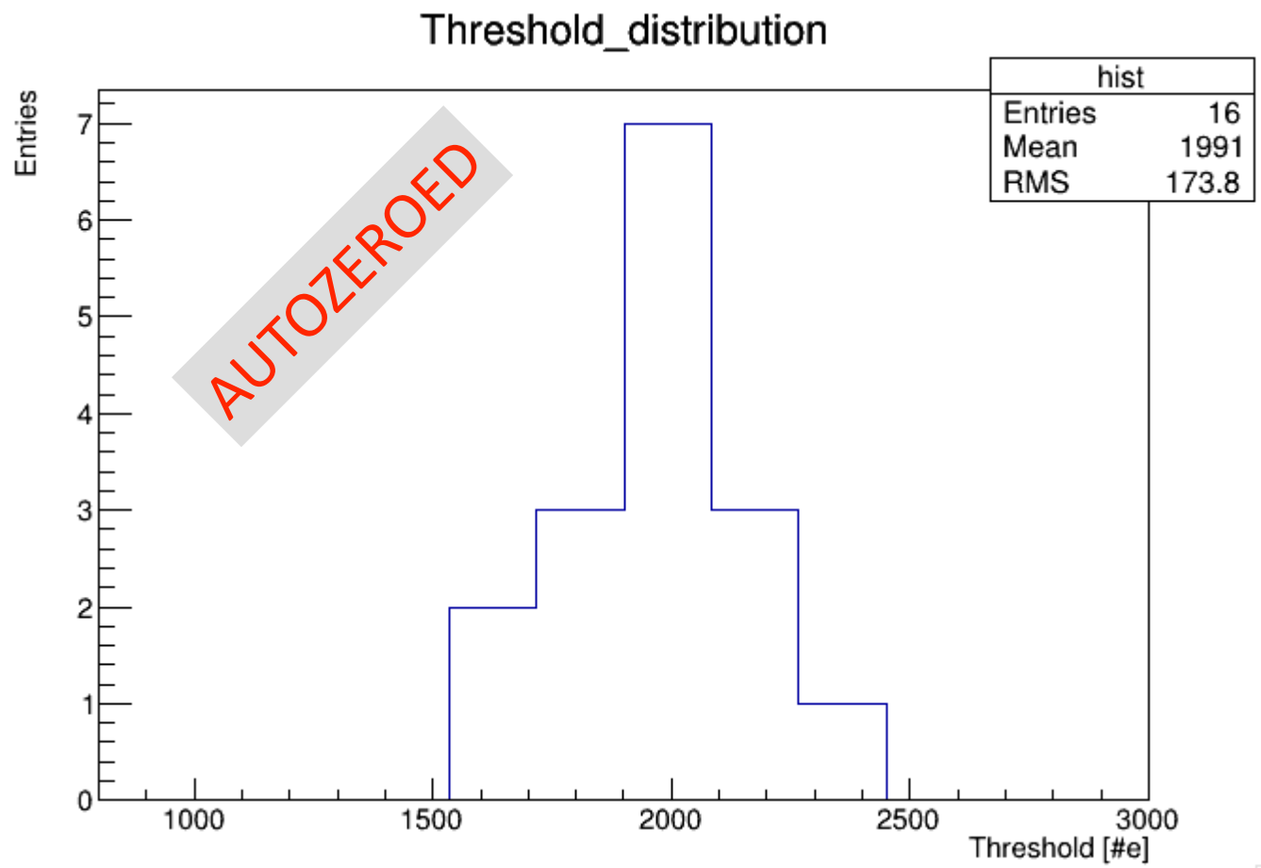
In-time overdrive and time-walk



- Threshold = 600 e-
- In-time overdrive (at the latch output) = 150 e-
- Analog time-walk at latch input = 9.3 ns

Offset compensation

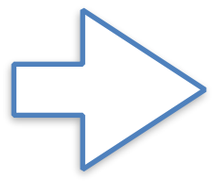




It could be better

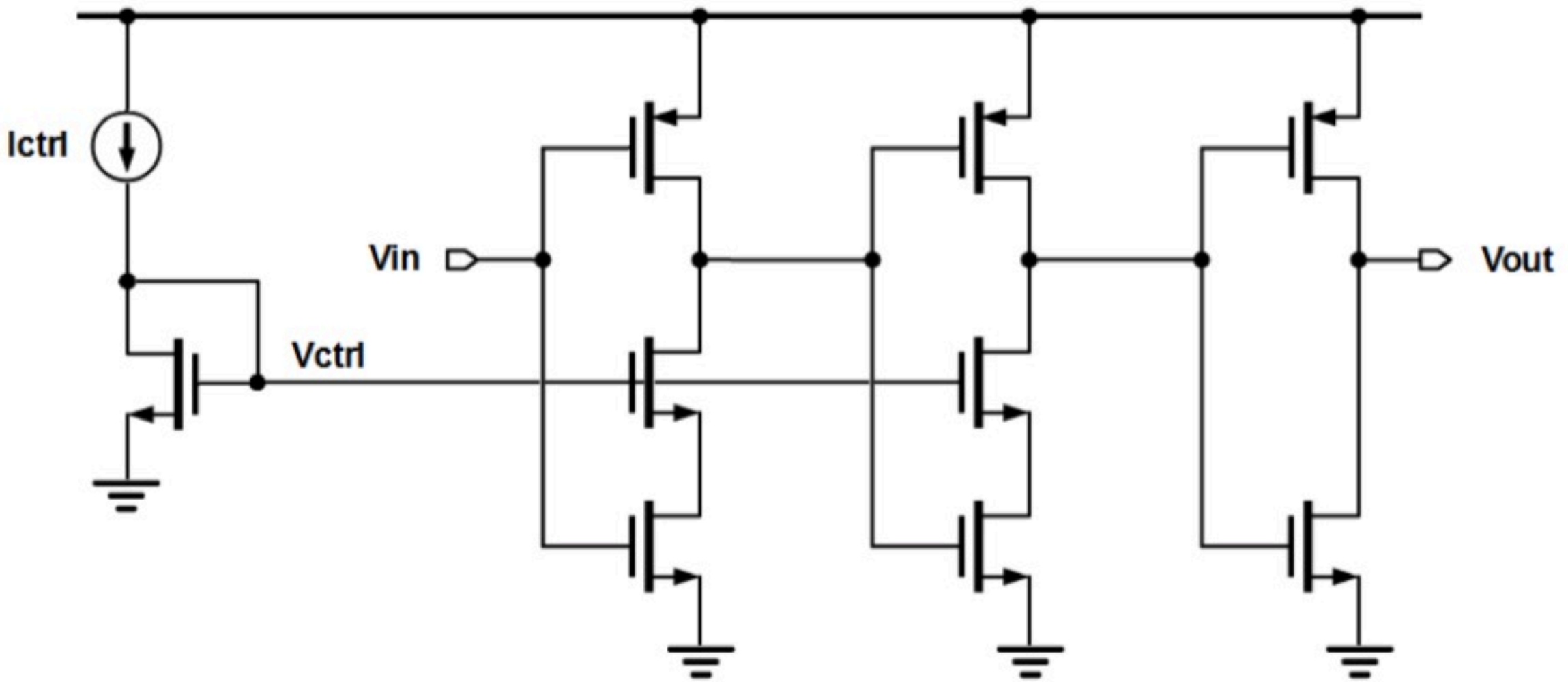
We have understood the problems

- Too high gain fluctuations due to mismatch
- Underestimation of the latch dynamic offset



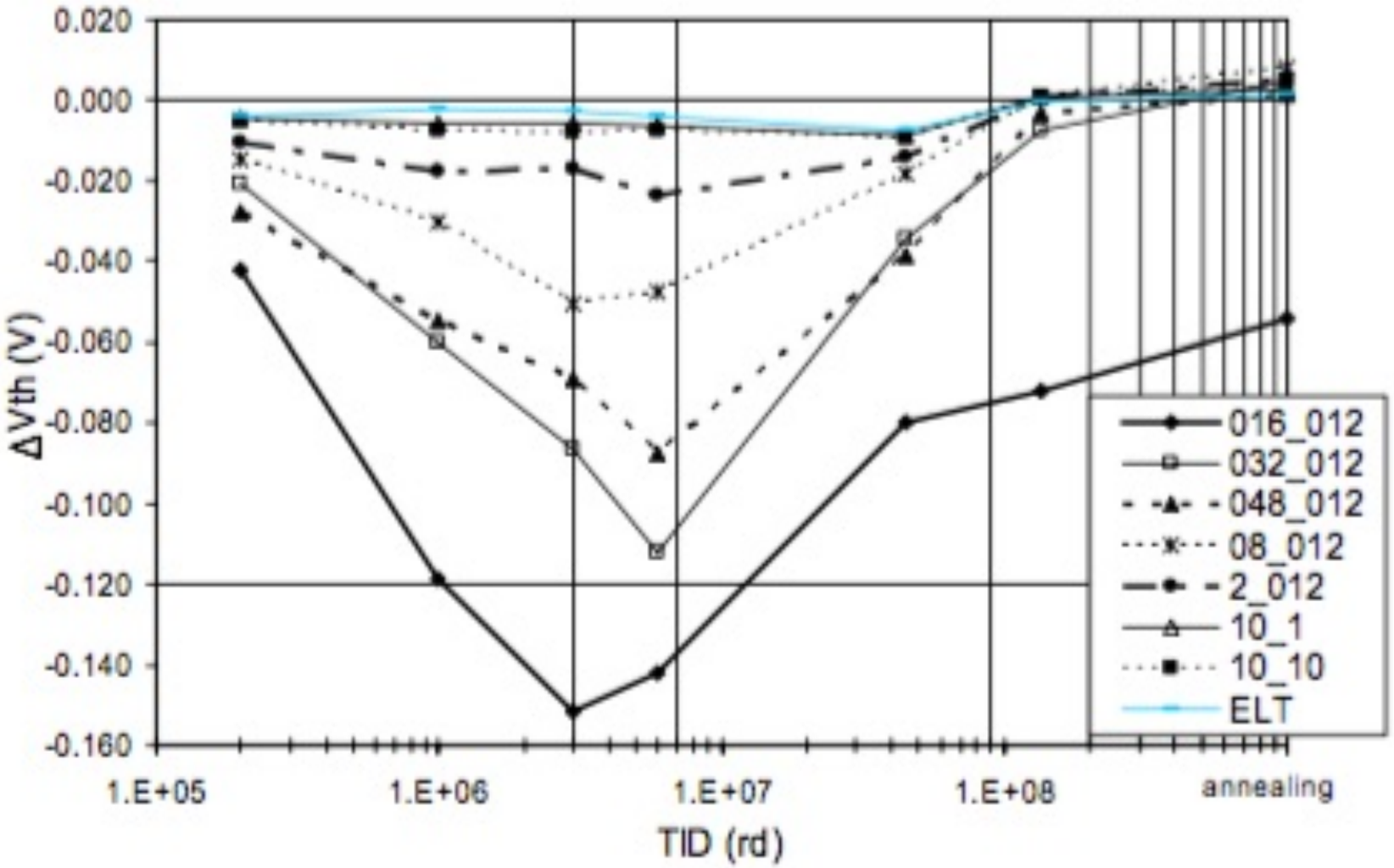
Solved in version 2

Delay line



- Current starving performed with NMOS-only transistors controlled by a current mirror

Irradiation effects at few Mrad



- In previous technologies like the 130nm there was a peak in threshold shift at a small irradiation values
- Compatible with what seen at few Mrad in the ToT frequency variation