Contribution ID: **101** Type: **Oral**

A synchronous analog very front-end in 65nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC

Tuesday 27 September 2016 12:00 (25 minutes)

This work describes the design, in 65nm CMOS, of a very compact, low power, low threshold synchronous analog front-end for pixel detectors at HL-LHC. Threshold trimming is avoided using offset compensation techniques. Fast ToT encoding is possible, as the comparator can be turned into a Local Oscillator up to few hundreds MHz. Two small prototypes have been submitted and tested; a X-ray irradiation up to 600 Mrad has been performed. Detailed results in terms of gain, noise, ToT and threshold dispersion are presented. This design will be part of the CHIPIX65 demonstrator and of the RD53A chip.

Summary

The HL-LHC accelerator will start its operation in 2025. It will establish unprecedented benchmarks in particle detection, in particular for the inner tracking systems of the experiments. Silicon pixel detectors and front-end electronics will face new challenges in terms of particle flux (up to 2 GHz/cm^2), radiation hardness (1 Grad in 10 years) and increased granularity (pixel size of 25x100 μm^2 or 50x50 μm^2).

In this paper the design of a new front-end for HL-LHC pixel sensors in 65 nm CMOS technology is presented. It consists of a one stage Charge Sensitive Amplifier with Krummenacher feedback AC coupled to a synchronous discriminator. The latter stage features a low gain differential amplifier and a track-and-latch comparator. The design has an area of 1225 μm^2 and a power consumption of 4.4 μA.
The offset compensation is performed via internal capacitors using the output offset storage technique, so that no threshold trimming via DACs is required. The latch can be also turned into a local oscillator by means of an asynchronous logic feedback loop in order to implement a fast time-over-threshold counting. This work has been performed and funded by the CHIPIX65/INFN project in the framework of CERN RD53 Collaboration.
Two testing prototypes containing a 8x8 pixel matrix have been submitted in October 2014 and in May 2015. Results in terms on gain, noise, ToT and offset compensation are presented. The voltage gain measured in all 64 pixels shows a very good linearity and uniformity with an RMS of 2.2%. The ToT linearity has been verified on a large interval of input charges (1-40 ke).
Noise shows a linear increase with the input capacitance: a ENC of 80 e- for an input capacitance of 50 fF is measured for a fast ToT of 90ns for 10ke- signal, important to keep analog dead-time below 1%.
The first prototype showed a threshold dispersion after the offset compensation phase equal to 174 e- RMS due to the mismatch of the latch stage; also an undesired baseline time-dependency was found. In order to fix this, the comparator was revised in the second prototype, leading to a reduction of the threshold dispersion to 70 e- RMS and eliminating any time-dependency.
The second chip was irradiated with X-ray up to 600 Mrad: analog signal amplitude, peaking time, noise and fast ToT frequency have been monitored during irradiation. The gain remains almost unaffected, while the peaking time increases from 24 ns to 31 ns. Offset compensation still works properly.
A 10% increase in noise for 50fF capacitance has been measured. The ToT frequency decreases linearly with radiation. These results have been compared with simulations using radiation models provided by the RD53 collaboration.

This front-end has been included in the CHIPIX65 demonstrator, a 64x64 pixel matrix designed by the CHIPIX65 collaboration and will be part of the RD53A final chip.

Authors: PATERNO, Andrea (Universita e INFN Torino (IT)); RIVETTI, Angelo (Universita e INFN Torino (IT)); LENG, Chongyang (INFN Torino); MONTEIL, Ennio (Universita e INFN Torino (IT)); ROTONDO, Francesco (Universita e INFN (IT)); CHAI, Junying (INFN, Politecnico di Torino); DEMARIA, Lino (Universita e INFN Torino (IT)); PACHER, Luca (Universita e INFN Torino (IT)); DA ROCHA ROLO, Manuel Dionisio (Universita e INFN Torino (IT))

Presenter: MONTEIL, Ennio (Universita e INFN Torino (IT))

Session Classification: ASIC

Track Classification: ASIC