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SALT Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment

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SALT is a new 128-channel readout ASIC for silicon strip detectors in the upgraded Tracker of LHCb experiment. It will extract and digitise analogue signals from the sensor, perform digital processing and transmit serial output data. SALT is designed in CMOS 130 nm process and uses a novel architecture comprising of analog front-end and ultra-low power (<0.5 mW) fast (40 MSps) sampling 6-bit ADC in each channel. An 8-channel prototype were already tested and the full 128-channel version was submitted. The design and first tests of 128-channel version will be presented.

Summary

The present Large Hadron Collider beauty (LHCb) detector performance is limited by readout electronics and data acquisition architecture. After the upgrade of LHC machine it will be capable to deliver more than one order of magnitude higher luminosity than presently used by the LHCb detector. To achieve this goal various detectors will need a new faster front-end electronics with the read-out running at the bunch-crossing rate of 40MHz.

Silicon strip detectors in the upgraded Upstream Tracker (UT) of LHCb experiment will require a new readout ASIC called SALT (Silicon ASIC for LHCb Tracking). A project of a 128-channel SALT ASIC is ongoing. It extracts and digitises analogue signals from the sensor, performs Digital Signal Processing (DSP) and transmits a serial output data. The ASIC is designed in CMOS 130nm technology, and uses a novel architecture comprising an analogue front-end and an ultra-low power (<0.5mW) fast (40MSps) sampling 6-bit ADC in each channel. The front-end comprises a charge preamplifier and a fast (T_{peak}=25ns) non-standard (fast recovery) shaper required to distinguish between the LHC bunch crossings at 40MHz. The front-end should work with sensor capacitances between 5-20pF. An ultra-low power (<1mW) DLL is used to control precisely the ADC sampling phase.

Digitised data from each ADC channel are processed in a DSP block which first subtracts pedestals and calculates mean common mode, which is then subtracted in each channel. The last DSP step is zero suppression (ZS). After ZS the data are buffered in SRAM, then a packet is formed and sent to DAQ via a number of serial DDR e-links.
An ultra-low power (<1mW) PLL is used in data serialization and fast data transmission circuitry.

Prototypes of all important SALT blocks, i.e. 8-channel analogue front-end, 8-channel 6-bit ADC, PLL, DLL and, SLVS I/O were designed in CMOS 130nm, fabricated and tested, showing very good performance.

An 8-channel SALT prototype comprising all important functionalities was produced and found, in tests, to be fully functional. In the first step, the serializers (DDR e-links) and deserializer were checked. Next, the DSP operation was tested extensively and all its functionalities were correct. After verification of digital processing and data transmission analogue pulses were observed, using DLL to shift the ADC sampling phase. Such measurements showd that pulse shape from front-end is correct, gain is about 0.45 ADC LSB/ke and the noise is below one LSB for input capacitance 10pF. The channel-to-channel baseline offset spread can be easily corrected by trimming DACs located in each channel, what was verified for all channels.

The full 128-channel prototype was just submitted. It includes also all blocks which were omitted in previous prototype: internal generation of common mode voltage, monitoring ADCs, band-gap reference source,

variable number of active e-links, etc.. The first test results of this prototype will be presented.

Primary author: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Presenter: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

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