Contribution ID: **113** Type: **Oral**

A fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm technology

Wednesday 28 September 2016 14:50 (25 minutes)

The design and measurement results of four ultra-low power 10-bit SAR ADCs, fabricated in CMOS 130˜nm technology, are presented. All prototypes use very similar architecture with main difference in split in the capacitive DAC network. The prototypes are fully functional, achieve excellent linearity (DNL < 0.3 LSB and INL ˜0.5 LSB), and show very good ENOB above 9.5 for 0.2 Nyquist input frequency, up to maximum sampling rate 40-50 MSps, depending on prototype. All prototypes consume less than 900 uW at 40 MSps achieving an excellent FOM 20-30 fJ/conversion-step.

Summary

In modern and future detectors of particle physics experiments an ultra-low power, area-efficient Analog-to-Digital Converter (ADC) is highly demanded. This work discusses the development of 10-bit Successive Approximation Register (SAR) ADC for readout system of luminosity detector at the future linear collider (ILC/CLIC). The presented design meets the most important requirements like ultra-low power consumption, excellent linearity and possibility of multichannel integration. The maximum sampling rate above 40MSps makes it also suitable for readouts of LHC experiments.

A fully differential architecture was chosen for ADC design. The ADC contains a pair of bootstrapped switches, differential Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture allows to eliminate static power consumption and to obtain power pulsing without additional effort. The Merge Capacitor Switching (MCS) scheme results in 93% switching energy reduction in comparison to conventional scheme. The minimum allowable capacitor was used as the DAC unit capacitance, moreover a split DAC architecture was applied to reduce total capacitance. Three different split architectures were designed in order to investigate the technology limits, namely the matching and parasitics. The asynchronous control logic was used to avoid a fast bit-cycling clock distribution. The ADC layout occupies 100 um x 800 um.

All prototypes were fabricated in CMOS 130 nm technology. Two prototypes use a default DAC split architecture 6-1-3 (6 MSB bits in first sub-DAC, split capacitance equal to LSB capacitance, 3 LSB bits in second sub-DAC) and differ slightly in control logic implementation, where various improvements increasing the meta-stability hardness and extending the maximum sampling rate above 50 MSps, were introduced. Two other prototypes, apart from using improved control logic, have different split in the capacitive DAC. They use 6-2-3 and 5-1-4 DAC networks and their input capacitance was reduced two times.

The 6-1-3 prototypes achieve an excellent linearity, with DNL below 0.3 LSB and INL ˜0.5 LSB, and excellent effective resolution. For 0.2 Nyquist input frequency the ENOB of 6-1-3 prototypes remains between 9.7 - 9.5 bits up to 40 MSps sampling rate, and above 9.3 bits up to 50 MSps for the improved prototypes. For Nyquist input the ENOB starts to decrease from 9.5 to 9.1 bits for sampling rates 30-40 MSps. The 5-1-4 and 6-2-3 show worse linearity (DNL ˜1 LSB, INL ˜0.9 LSB) and their ENOB is in range 9.3-9.0 over the range of sampling rates and input frequencies.

Power consumption of the default 6-1-3 configuration is below 700˜uW at 40 MSps. It gives excellent FOM below 28 fJ/conversion-step, the lowest, to the authors knowledge, FOM obtained in 130 nm CMOS for similar ADC specifications. Also other configurations show excellent, although slightly higher, FOMs. The measurement results and comparison of different prototypes will be given in this talk.

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Session Classification: ASIC

Track Classification: ASIC