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Developments of two 4 × 10-Gbps radiation-tolerant VCSEL array drivers in 65 nm CMOS

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We present designs and test results of two ASICs, VLAD and lpVLAD. Each is a 4-channel, 10-Gbps-per-channel VCSEL array driver fabricated in a 65 nm CMOS technology. lpVLAD deploys a novel high-efficient output structure to achieve a record low power consumption of 25 mW/ch when delivering 2 mA bias and 6 mA modulation currents at 10-Gbps. Eye diagrams of both two designs under post-layout simulations easily pass 10-Gbps requirement. The full-channel optical link test will be carried out in June and the results will be reported in the conference.

Summary

VCSEL-based high-speed, low-power, radiation-tolerant short-range optical data links are in high demand for detector data transmission in the LHC upgrades as well as in other physics detector developments. Benefited from the commercial array optical transceivers advancement, we have developed an array optical transmitter module (ATx) with radiation-tolerant optical components. Besides, another critical component and key challenge is a high-speed radiation-tolerant VCSEL array driver ASIC. In this paper, we present designs and test results of two 4-channle, 10-Gbps-per-channel, radiation-tolerant VCSEL driver ASICs, VLAD and lpVLAD, which are both fabricated in a commercial 65 nm CMOS technology.

Each channel in VLAD consists of an input matching impedance, a two-stage pre-driver (1.2 V), an output driver (1.2 V and 2.5 V) and their biasing circuits. The ASIC receives differential CML signals of 400 mVp-p, complying with the lpGBT output. The two output pads of each channel are directly wire-bonded to the anode and the cathode (GND) pads of the VCSEL, providing a bias current from 1 to 10 mA, and a modulation current from 3 to 9 mA. The total power consumption is 35 mW/channel at the default output of 1.5 mA bias and 7 mA modulation currents at 10 Gbps.

lpVLAD, the low-power version of VLAD, differs from VLAD in the output driver. This novel output structure uses a pair of PMOS and NMOS switches to modulate the VCSEL. The push-pull complementary switches fully utilize both differential outputs of the pre-driver and increase the VCSEL modulation efficiency to 100% theoretically. A single stage current generator is used to provide the VCSEL bias current, and a feed-forward signal from the pre-driver is used to stabilize the off-current to the VCSEL. This new driving method results in an ultra-low power consumption of 25 mW/ch when delivering 2 mA bias and 6 mA modulation currents at 10-Gbps. The lpVLAD is able to provide a bias current from 1 to 6 mA, and a modulation-current from 5 to 8 mA.

An I2C digital control module with triple-modular-redundancy structure adapted from CERN is used in both VLAD and lpVLAD. The 1.2 V and 2.5 V power bus topology is carefully designed. Current return paths and the grounds of the on-chip capacitors for the 1.2V and 2.5 V powers are separated with single-point connection to minimize possible multi-channel crosstalk.

Eye diagrams at the VCSEL under post-layout simulations for both VLAD and lpVLAD easily pass 10-Gbps data rate requirement in each channel when all four channels work simultaneously. We tapeout the designs in February 2016 and expect to test the ASICs in June and July 2016. The radiation-tolerant performance and full-channel optical link test including BER-OMA and crosstalk will be fully evaluated, and the results will be reported.

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