First results of the front-end ASIC for the strip detector of the PANDA MVD

T. Quagli¹, K.-T. Brinkmann¹, V. Di Pietro¹, A. Lai², A. Riccardi¹, J. Ritman², A. Rivetti³, M. D. Rolo³, T. Stockmanns², A. Zambanini²

¹ II. Physikalisches Institut, JLU Gießen
² Forschungszentrum Jülich GmbH
³ INFN, Sezione di Torino

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Outline

• The PANDA MVD

• The PANDA Experiment: Physics Motivation and Experimental Setup

• The Micro Vertex Detector

• The PASTA chip

• First results from the PASTA tests
The PANDA MVD
The PANDA Experiment

- **QCD in non-perturbative regime**
  - Charmonium spectroscopy
  - Search for hybrids and glueballs
  - Study of exotic states (X, Y, Z)
- **In-medium effects**
- **Nucleon form factor**
- **Hypernuclear physics**

- Fixed target experiment at FAIR, Darmstadt
- Antiproton beam with $p = 1.5 – 15$ GeV/c and hydrogen or nuclear target
- Located at the High Energy Storage Ring (HESR)
The PANDA Detector

- $4\pi$ acceptance
- Electromagnetic Calorimetry
- Tracking for Charged Particles (MVD, STT, GEM, FTS)
- Particle Identification (DIRC, SciTil, RICH)
- Continuous, triggerless readout

Target Spectrometer:
- solenoid superconducting magnet (2T field)

Forward Spectrometer:
- dipole magnet (2Tm field)
The Micro Vertex Detector (MVD)

- High resolution (<100 μm) vertex reconstruction; good time resolution (<6 ns)
- Radiation tolerance up to $\sim 10^{14} \text{n}_{1\text{MeV}_{\text{eq}}} / \text{cm}^2$
- High nominal rate capability ($2 \cdot 10^7 \text{ pbar-p annihilations/s}$) and triggerless readout
- Low material budget (<10% radiation length overall)

4 barrels surrounding the interaction point and 6 disks in the forward direction

Two technologies:

- Hybrid Pixel Detectors
- Double-sided Silicon Strip Detectors
The Micro Vertex Detector

beam
Strip disks

30 cm

Pixel disks

Pixel barrels

Strip barrels

53 cm
PASTA – PAnda STrip ASIC
PASTA

- **PANDA Strip ASIC**
- Free-running readout chip
- ToT-based readout with precise timestamp

**Key design features**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>64</td>
</tr>
<tr>
<td>Input pitch</td>
<td>63 μm</td>
</tr>
<tr>
<td>Rate capability</td>
<td>100 kHz/channel</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 4 mW/channel</td>
</tr>
<tr>
<td>Front-end noise</td>
<td>&lt; 600 e−*</td>
</tr>
<tr>
<td>Time bin width</td>
<td>50 - 400 ps</td>
</tr>
<tr>
<td>Charge resolution</td>
<td>8 bit (dyn. range) *</td>
</tr>
<tr>
<td>Radiation tolerance</td>
<td>100 kGy *</td>
</tr>
</tbody>
</table>

* Design goal

- Joint project Uni Gießen – INFN Torino – FZ Jülich
- Derived from TOFPET (M. Rolo et al, 2013 JINST 8 C02050)
Measurement Concept

• Low threshold: better time stamp resolution

• High threshold: better jitter performance
Timing

Diagram showing the timing of ToT (Time of Flight) and Clock signals.
Timing
PASTA Architecture

1. Front-end
   - PreAmp
   - \( \text{thr}_T \rightarrow 4 \times \text{TAC}_T \rightarrow \text{ADC}_T \)
   - \( \text{thr}_E \rightarrow 4 \times \text{TAC}_E \rightarrow \text{ADC}_E \)

2. Analog TDC
   - \( \text{TDC}_{\text{CTRL}T} \)
   - \( \text{TDC}_{\text{CTRL}E} \)
   - hit-valid.

3. TDC Control
   - \( \text{TDC}_{\text{CTRL}E} \)
   - hit-valid.

4. Global Control
   - data register
   - CLK
   - config.
   - output buffer
   - LVDS clock
   - LVDS config
   - LVDS data

"analog", "digital"
Front-End Implementation

- Preamplifier
- Current Buffer
- ToT Amplifier
- Hysteresis Comparator
Front-End Implementation

- First preamplification
- Two input polarities, same output polarity
Front-End Implementation

• Current amplification
• Impedance adaptation
Front-End Implementation

- Last amplification
- Constant current discharge of feedback capacitance
Front-End Implementation

- Low noise sensitivity
- Two for each channel: energy and time branches
Front-end Simulations

TOT linearity in the input charge range of 1fC to 40 fC with a capacitance of 25 pF

Electronic noise considering an input capacitance in the range 1pF to 30 pF with an input charge of 4fC
Analog TDC

Clock frequency 160 MHz
Amplification 128
Time bin width 50ps

\[ C_{TDC} = 4 \cdot C_{TAC} \]
\[ I_{TDC} = \frac{1}{32} \cdot I_{TAC} \]
Optimization of the TDC Control

• Size reduced by ~80%
• Overall power consumption halved
• Radiation-hard logic implemented

Single Event Upset (SEU) Protection

• 1 bit: Triple Modular Redundancy
• N bits: Hamming encoding
PASTA Tests
PASTA Test Board

- Prototypes fabricated on a Multi Project Wafer
- 110 nm commercial CMOS technology
- Test board designed, fabricated and assembled
JDRS – Jülich Digital Readout System

Modular, flexible system, used for PASTA as well as for the ToPix chip.

Data conversion and communication with the PC:

- **DUT**: ToPix, PASTA
- **Evaluation board**: Xilinx ML605 (Virtex 6 FPGA)
- **Firmware**: VHDL

Configuration and data handling:

- **PC**
- **Software (C++)**
- **MVD readout framework (MRF)**
- **Qt-based GUI**
SDI:
Global Configuration sent to the chip

SDO:
Chip acknowledges the reception of the Global Configuration
SDI:
Global Configuration read command

SDO:
Chip sends back the stored Global Configuration.

Values match correctly.
Analog Front-End Amplifier

Comparator output, Energy and Time branches

ToT amplifier output
Linearity of the ToT amplifier output vs. pulse amplitude of the calibration circuit

Analog Front-End Amplifier
Linearity of the comparator output vs. pulse amplitude of the calibration circuit

ToT [ns]

Pulse amplitude
Tests with the PASTA DAQ

Digital output readout:
• possible in compact mode (one word for event) with a clock of 80 MHz;
• data decoding ok (e.g. one can identify the firing channels, the active TAC and the continuity of the frame IDs to check for data loss);
• possibility of enabling/disabling channels;
• operation of the local configuration unclear; work in progress.
Conclusions

- PASTA chip designed and fabricated.

- Hardware and software test system now available and in use.

- Encouraging results from the first tests, but lot of work still to be done!
Thank you for your attention!
Preamplifier

n-type Strips

Current Buffer
Current Buffer
ToT Amplifier
MVD – Strip Part

- Rectangular, square and trapezoidal sensors
- Two barrels and two rings around the last disks
- 200k channels on 296 sensors

Barrel sensors
- Readout chip: 64 strips
- 512 x 512 strips
- 896 x 512 strips
- Stereo angle: 90°
- Strip pitch: 65 µm

Disk sensors
- 768 x 768 strips
- Stereo angle: 15°
- Strip pitch: 45 µm
Strip Modules – Barrels

- Front-end electronics
- Flexible Printed Circuit
- Cooling pipe
- Sensors
- Composite stave