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First results of the front-end ASIC for the strip detector of the PANDA MVD

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PANDA is a key experiment of the future FAIR facility and the Micro Vertex Detector (MVD) is the innermost part of its tracking system. It will be composed of four barrels and six disks, instrumented with silicon hybrid pixel detectors and double-sided microstrip detectors.
PASTA (PAnda STrip ASIC) is the readout chip for strip sensors.
An overview of the chip, of its readout system and of the first results of its characterization will be presented.
Supported by BMBF, HIC4FAIR and JCHP.

Summary

PANDA is a key experiment of the future FAIR facility, under construction in Darmstadt. It will study the collisions between an antiproton beam with momenta between 1.5 GeV/c and 15 GeV/c and a fixed proton or nuclear target, allowing to study QCD at intermediate energies.
The Micro Vertex Detector (MVD) is the innermost part of the tracking system of the experiment; it will be composed of four concentric barrels and six forward disks, instrumented with silicon hybrid pixel and double-sided silicon microstrip detectors.

The triggerless operation of PANDA, in addition to the high expected collision rate, poses significant challenges on the detector readout electronics.
The PASTA (PAnda STrip ASIC) chip has been developed to read out the strip sensors of the MVD and its architecture is based on the Time-over-Threshold technique.
The first stage of the analog frontend chain consists of a preamplifier which can be connected to both n-type and p-type strips, and a second stage where a constant current discharges a feedback capacitance to extract a linear ToT information.
The leading and trailing edges of the ToT signal are measured with time-to-digital converters with linear analog interpolators, with an architecture inherited from TOFPET [1], thus providing a time resolution adjustable between 50 and 500 ps.
A 64 channel chip prototype has been submitted in a commercial 110 nm CMOS technology; the final prototype size is 3.4 x 4.5 mm^2.

The chip is hosted and wire bonded on a test board which allows to connect the LVDS input/output lines to the acquisition system, as well as to probe the analog and digital test pads.
Additionally, a strip sensor can be placed on the board and connected to the chip channel inputs.
In order to completely characterize the chip, the Jülich Digital Readout System (JDRS) is used.
The system, originally developed to read out the pixel electronics of the MVD, is based on a Virtex 6 FPGA on a Xilinx development board. Its structure consists of four layers which handle the ethernet connection between the FPGA board and the PC, the data transfer and formatting and the board-specific and chip-specific functions. Thanks to this modularity, the system can be adapted with relative ease to test different chips in high-rate environments.
The first test of the PASTA chip concerns the functionality of the global controller and of its capability of reading and storing the chip configuration.
The analog frontend chain can be tested by means of injecting a pulse on a test pad and probing the output of the ToT amplifier through dedicated pads.
Finally, it is possible to simulate the comparator output by injecting a pulse in the digital local controller, thus

allowing to test the TDC block, consisting of the analog TDC and of the local controller.
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[1] M.D. Rolo et al.
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