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SAMPA Chip: the New ASIC for the ALICE TPC and MCH Upgrades

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This paper presents the SAMPA, a new ASIC for the ALICE upgrade for Time Projection chamber (TPC) and Muon chamber (MCH) read-out frontend electronics.

The SAMPA ASIC is designed in 130nm CMOS technology with 1.2V nominal power supply. SAMPA includes 32 channels, with selectable input polarity, and three possible combinations of shaping time and sensitivity. Each channel comprises a Charge Sensitive Amplifier, a shaping stage, and a 10-bit ADC. A DSP block and 11 SLVS output links (throughput up to 3.2 Gbps) complete the chip.

Experimental results of the first complete ASIC prototype will be presented.

Summary

Operating the ALICE TPC (Time Projection Chamber) at a Pb-Pb collision rate of 50 kHz requires to replace the present MWPC based read-out by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time is higher than the average time between interactions, a trigger-less continuous read-out is required, which is not supported by the present front-end electronics. Also in the case of the Alice Muon Chambers (MCH) detector, the present front-end electronics installation does not cope with the future (higher interaction rate) running conditions and needs to be replaced. Thus, the new read-out ASIC, named SAMPA, is developed to serve both the TPC and Muon Chamber read out.

The SAMPA ASIC integrates 32 channels of the full data processing chain, it is designed in TSMC 130 nm CMOS technology with nominal voltage supply of 1.2 V and it supports continuous and triggered read-out. The SAMPA consumes an area of about 86 mm^2

It comprises positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, which is then digitized by a 10-bit 10 Msamples/s ADC. After the ADC, a digital signal processor allows baseline shifts correction and zero suppression; unprocessed direct throughput of the full data stream is also possible. The data read-out takes place, either continuously or in triggered mode, by enabling up to eleven 320 Mbps SLVS serial links, allowing a data throughput of up to 3.2 Gbps.

The CSA shaping time can be configured to operate at 160 ns, with sensitivity of 20 mV/fC or 30 mV/fC (TPC case), or at 300 ns, with a sensitivity of 4 mV/fC (MCH case).

Second SAMPA submission included the fist complete designed ASIC chip and a set of mini-chips containing the different functional sub-blocks (analog stage, ADC, SLVS drivers, etc.).

Results of the tests performed on both the functional blocks and on prototypes from the first complete ASIC will be presented, and compared with the simulation results. The chip performance and specifications will be fully discussed.

Authors: VELURE, Arild (University of Bergen (NO)); CAVALCANTE DE SOUZA SANCHES, Bruno (Universidade de Sao Paulo (BR)); HERNANDEZ HERRERA, HUGO DANIEL (Universidade de Sao Paulo (BR)); BREGANT, Marco (Universidade de Sao Paulo (BR)); OLIVEIRA WEBER, Tiago (Universidade de Sao Paulo (BR))

Co-authors: PILYAR, Alexander (Joint Inst. for Nuclear Research (RU)); OSKARSSON, Anders (Lund University (SE)); LJUBICIC, Ante (Brookhaven National Lab (USA)); AYALA PABON, Armando (Universidade de Sao Paulo (BR)); REHMAN, Attiq Ur (University of Bergen (NO)); ESPAGNON, Bruno (Universite de Paris-Sud 11 (FR)); BRITTON, Charles (Oak Ridge National Laboratory); MORAES, Danielle (Universidade de Sao Paulo (BR)); SILVERMYR, David (Lund University (SE)); ROEHRICH, Dieter (University of Bergen (NO)); DE CARVALHO, Dionisio (Universidade de Sao Paulo (BR)); WANLIN, Eric (Universite de Paris-Sud 11 (FR)); TAMBAVE, Ganesh Jagannath (University of Bergen (NO)); NOEL, Guillaume (Universite de Paris-Sud 11 (FR)); BRULIN, Gwenael (Universite de Paris-Sud 11 (FR)); MJOERNMARK, Jan-Ulf (Lund University (SE)); READ, Kenneth (Oak Ridge National Lab (ORNL)); ROEED, Ketil (University of Oslo (NO)); TUN-LANOE, Khaing Mon Mon (Universite de Paris-Sud 11 (FR)); ULLALAND, Kjetil (University of Bergen (NO)); OSTERMAN, Lennart Hans Ander (Lund University (SE)); GAMEIRO MUNHOZ, Marcelo (Universidade de Sao Paulo (BR)); RUSSO, Patrice (Universite de Paris-Sud 11 (FR)); ZAPOROZHETS, Sergey (Joint Inst. for Nuclear Research (RU)); MAHMOOD, Sohail Musa (University of Oslo (NO)); VERASHCHAHIN, Stsiapan (Joint Inst. for Nuclear Research (RU)); CHAMBERT, Valerie (Universite de Paris-Sud 11 (FR)); Prof. VAN NOIJE, Wilhelmus A.M. (Escola Politécnica da Universidade de São Paulo (BR))

Presenter: BREGANT, Marco (Universidade de Sao Paulo (BR))

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