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Software and Firmware co-development using High-level Synthesis

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Accelerating trigger applications on FPGAs (using VHDL/Verilog) in CMS experiments at LHC-CERN warrants consistency between each trigger firmware and its corresponding C++ model. This tedious and time consuming process of convergence is exacerbated during each upgrade study. High-level synthesis, with its promise of increased productivity and C++ design entry bridges this gap exceptionally well. This paper explores the "single source code"approach using Vivado-HLS tool for redeveloping the upgraded CMS Endcap Muon Level-1 Track finder (EMTF). Guidelines for tight latency control, optimal resource usage and compatibility with CMSSW are outlined in this paper.

Summary

Acceleration of trigger applications in CMS experiments in the Large Hadron Collider at CERN has been traditionally performed on FPGAs using hardware description languages (HDLs) such as VHDL/Verilog. Specifics of the large-scale high-energy physics experiments require that each trigger firmware design must be accompanied by a software model that can be used for analyzing its performance, verification of hardware functionality, and other tasks. These software models must be designed in C++ and be compatible with the CMS software framework, CMSSW.

Since CMS upgrades firmware algorithms and trigger hardware at regular intervals, the software models must be constantly kept synchronized with firmware algorithms. The typical approach is to write these models by hand. Since the trigger firmware designs are substantially complex, creating and maintaining the software models that exactly match firmware behavior is a major challenge. The final convergence between the firmware and software model is especially tedious; it usually takes months to find and fix small mismatches.

Since 2002, the CSC Track-finder system of the CMS Endcap Muon Level-1 trigger has maintained the C++/RTL model consistency by using a homemade VPP library which automatically generates C++ and Verilog files from a single source code. This approach worked extremely well for less complex firmware design of the legacy system, providing full consistency between firmware and software model automatically. However, the recent hardware upgrade brought much larger FPGAs and much more complex firmware algorithms, and VPP has become inadequate for this task.

Recent advancements in high-level synthesis tools (HLS) hold the promise of high productivity through the use of design entry in C++ that reduces the difficulty for developing and managing code complexity at the HDL level. However, the major challenge in using HLS is to be able to use C++ constructs to perform fine-grained control of the generated firmware in such a way that it satisfies the constraints of CMS trigger applications:

• Stringent latency requirements.
• Limited FPGA resources.
• Compatibility with CMSSW.

In this paper, we present our exploration into using a "single source code"approach in which we perform software and firmware co-development using Vivado HLS, a C++-based high-level synthesis tool used for Xilinx FPGAs. Vivado HLS enables us to have a single source code which can be used as the C++ model for verification by physicists and to generate the RTL model to synthesize firmware for the FPGA.

Based on the lessons learned in our exploration, we developed design patterns and guidelines to execute the

fine-grained control of the generated firmware. The results are very promising:
• The code of the upgraded CMS Endcap Muon Level-1 Track Finder (EMTF) was redeveloped in Vivado HLS.
• All latency constraints were met in all modules of the EMTF algorithm.
• HLS resource usage was comparable to (and, in some cases, better than) resource usage of manually written Verilog code.
• Based on the developed guidelines, minor changes were made to the coding style, resulting in all HLS code being compatible with CMSSW.

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