Versatile Link PLUS Transceiver Development

Csaba SOOS
EP-ESE-BE

on behalf of the VL+ collaboration

Outline

- Versatile Link PLUS project introduction
  - Key differences between VL and VL+
  - Link architecture
- VL+ front-end module
  - Variants
- Commercial module customisation
  - Customisation roadmap
- Custom module development
  - Prototype test results
- Summary

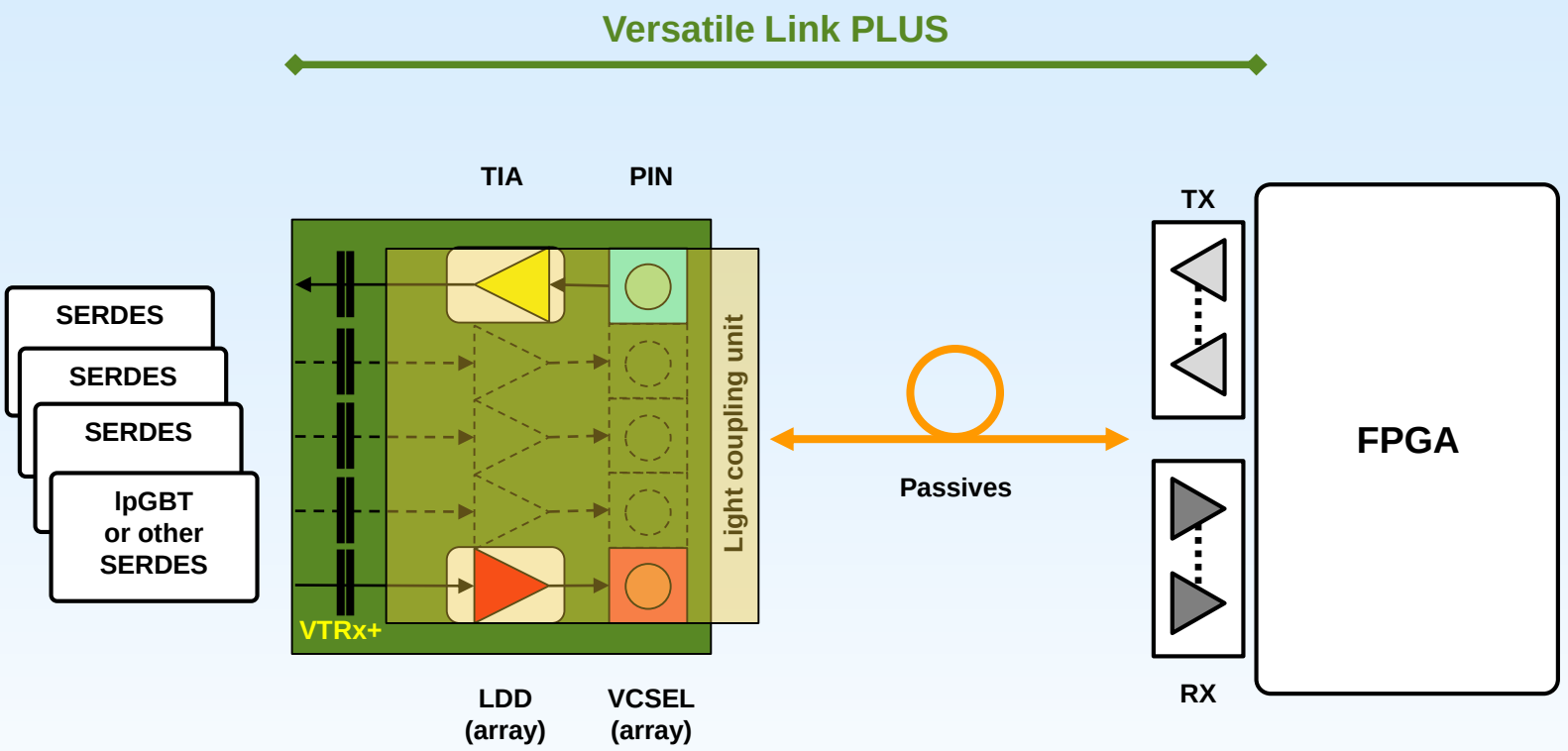
Introduction to Versatile Link PLUS

- The Versatile Link PLUS project (VL+) targets the phase II upgrades of the ATLAS and CMS experiments
- VL+ was officially announced at ACES 2014 and started on 1 Apr 2014. It is subdivided in three phases of 18 months each:
  - Phase 1: proof of concept (Apr 2014 – Oct 2015)
  - Phase 2: feasibility demonstration (Oct 2015 – Apr 2017)
  - Phase 3: pre-production readiness (Apr 2017 – Oct 2018)
- **Collaboration between CERN, FNAL, Oxford, and SMU**

	Versatile Link	Versatile Link PLUS
Optical mode	Single- and multi-mode	Multi-mode
Flavours	1Tx+1Rx, 2Tx	Configurable at build time up to nTx(+1Rx)
Radiation level	Calorimeter grade	Tracker grade
Form factor	SFP+	Custom miniature
Data rate	Tx/Rx: 5 Gb/s	Tx: 5/10 Gb/s, Rx: 2.5 Gb/s

Table : Key differences between VL and VL+

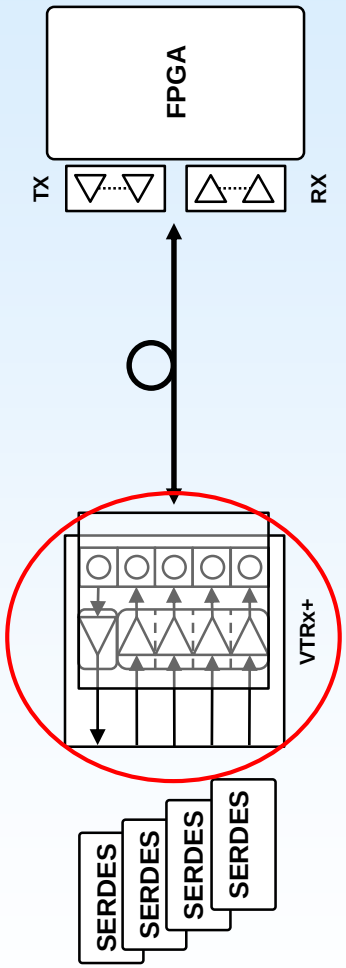
Versatile Link PLUS architecture



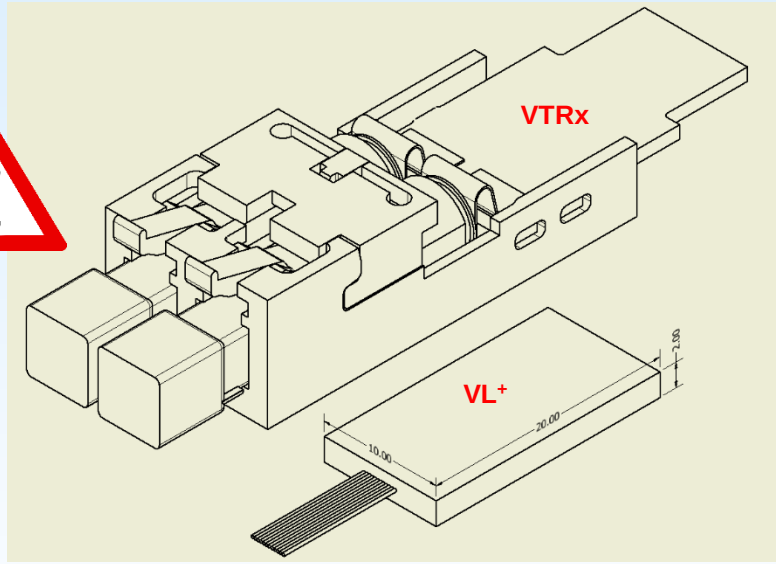
On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

VL+ front-end module

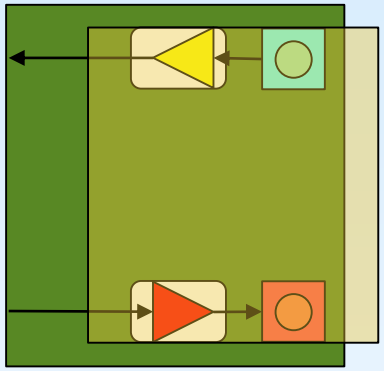


- Versatile
  - Up to 4Tx + up to 1 Rx, configurable at build time or by masking channels
  - 4Tx + 4Tx may become feasible (TBD)
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturised
  - Target dimensions 20 x 10 x 2 mm
- Pluggable
  - Either optical or electrical (or both) connector
- Data-rate:
  - Tx: up to 10 Gb/s
  - Rx: up to 5 Gb/s
- Environment
  - Temperature: -35 to + 60 °C
  - Radiation (based on Tracker requirements, TBD)
    - Total Dose: 1 MGy qualification (investigations up to 2 MGy)
    - Total Fluence: 2×10^{15} n/cm^2 and 1×10^{15} hadrons/cm^2

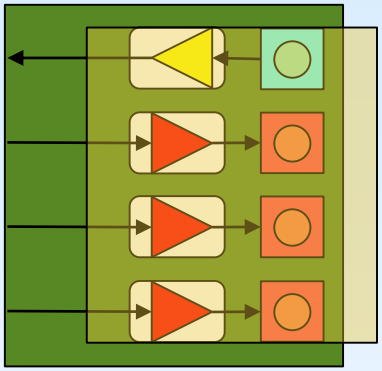


VL+ front-end module variants

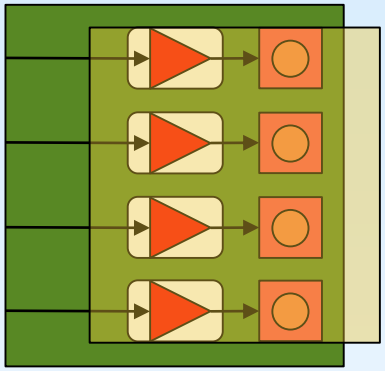
Discrete-based derived from:
- **Light peak**
- **USB-3**
- **Thunderbolt**



1 TX + 1 RX

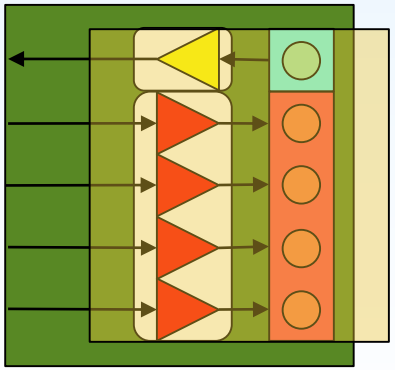


3 TX (single channel LDDs) + 1 RX

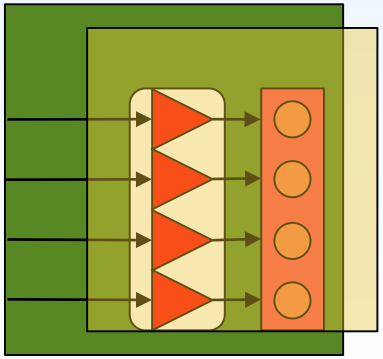


4 TX (single channel LDDs)

Array-based derived from:
- **QSFP+ engine**
- **Mid-Board engine**



1/3/4 TX (using LDD array) + 1 RX



4/8 TX (using LDD arrays)

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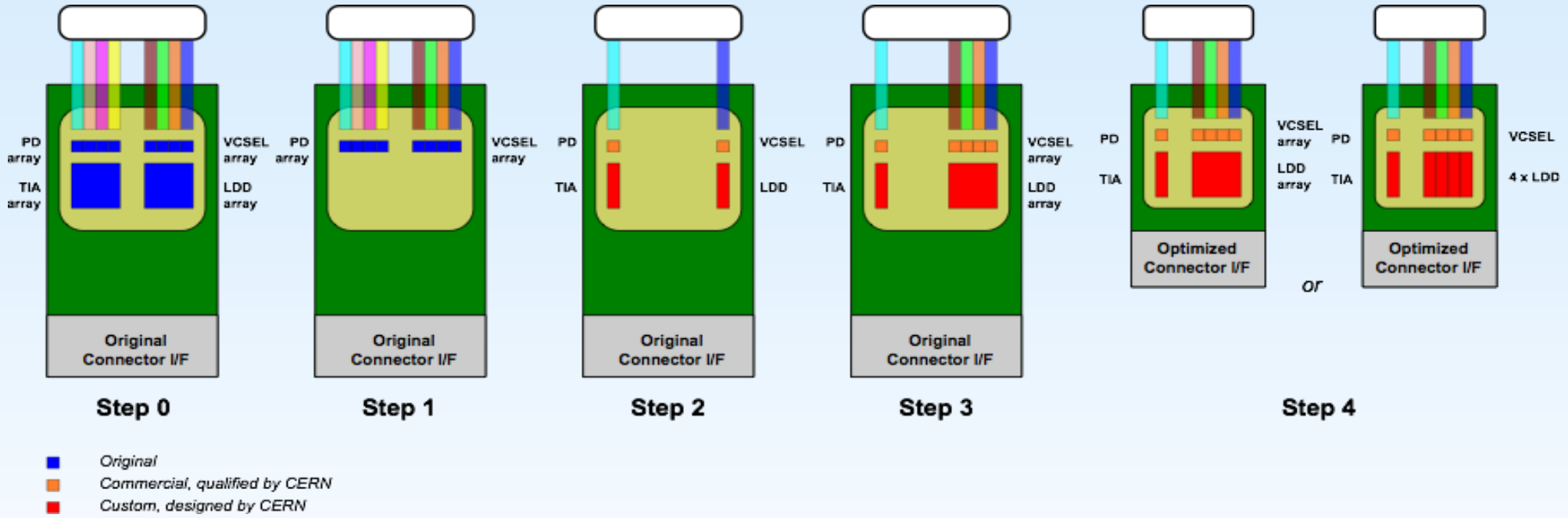
Dual approach

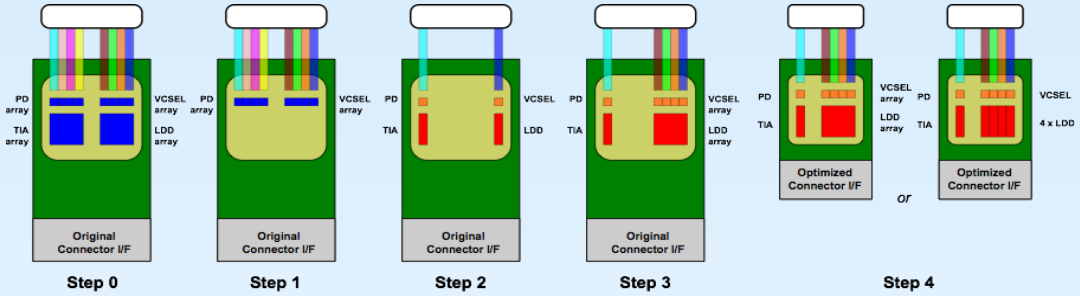
- Modification of existing commercial modules
  - Working in close collaboration with various industrial partners
    - Minimise customisation to retain cost benefit from volume production
- In-house design of module
  - Working in close collaboration with suppliers of optical coupling blocks
  - Working in close collaboration with industrial partner on integration
    - CERN-designed PCB
    - CERN-specified or procured opto-die
    - CERN-specified or procured ASICs (LDD, TIA-LA)
  - Potentially the path to highest level of affordable customisation

Customisation steps



- Progression from standard component to full-custom object suitable for CERN project needs
  - Start with evaluation of standard component and sub-components (Steps 0/1) on a per-vendor basis

Commercial roadmap

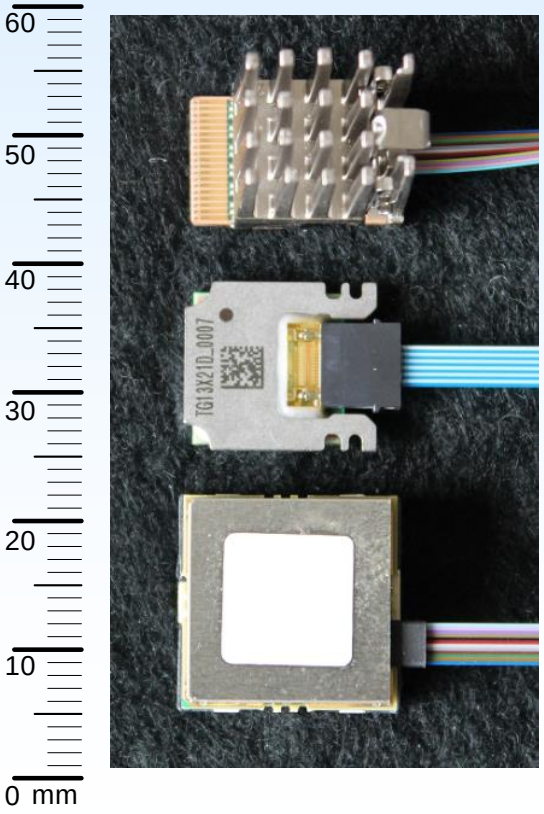


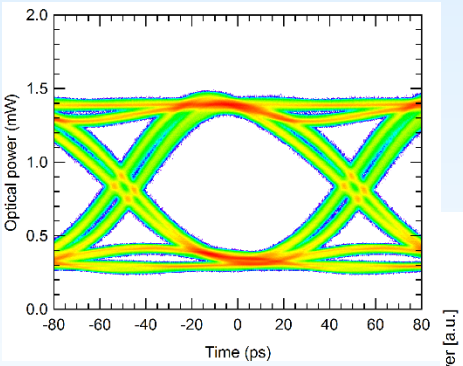
- Development *(until 2018)*
  - CERN Market Survey
    - CERN issues Technical Requirement & Questionnaire
    - Companies return completed Questionnaire
    - CERN reserves the right to order samples (Steps 0, 1) and/or ASIC drop-ins to existing parts for evaluation (Steps 2, 3)
    - CERN qualifies companies having required technology
  - CERN Price Enquiry
    - Qualified companies receive full technical specification for development
    - Qualified companies bid for development (Step 4)

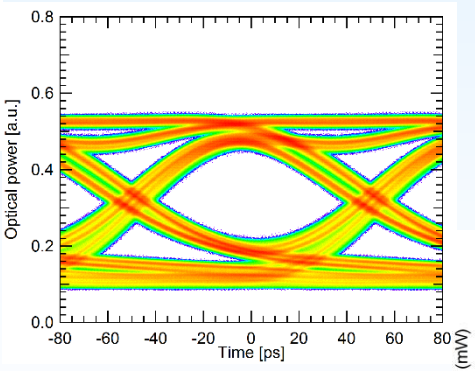
- Production *(2019 onwards)*
  - Companies having successfully completed development (on time, in budget) will be invited to tender for full production
  - One or two lowest cost bidder(s) will receive production contract

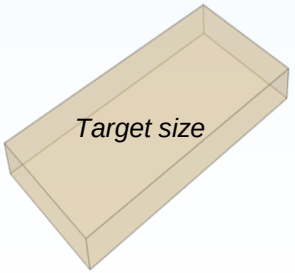
Testing candidate commercial modules

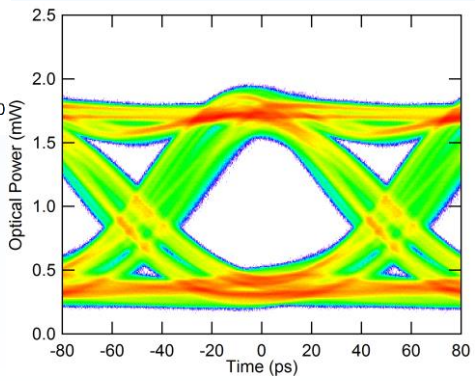
- First samples from various module vendors have been functionally tested in the laboratory (Step 0). More samples are coming.
- Modules containing only optical components have been requested for environmental tests (Step 1)





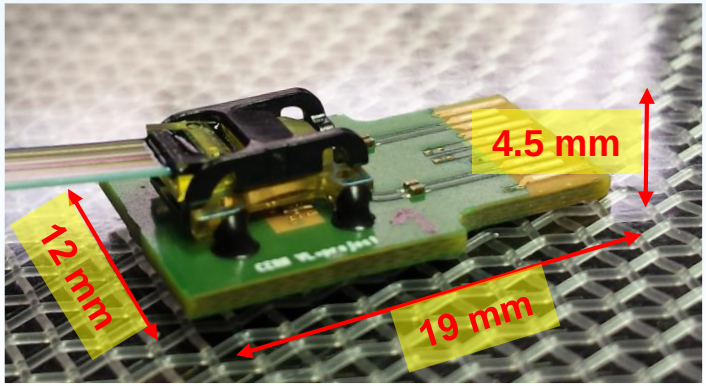




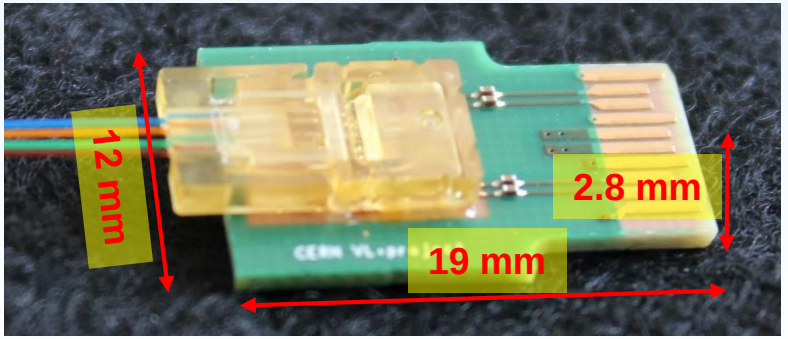


Custom VL+ front-end prototypes

- In-house design and development of full custom module
- First two prototypes are based on same active components
  - Single-channel laser driver (commercial) and CERN radiation tolerant TIA (GBTIA)
  - 14 Gb/s VCSEL/photodiode from Philips Photonics (ULM)
- Their optical coupling blocks are different
  - V1 is using US conec's Mechanical Optical Interface (MOI) + Prizm
  - V2 is using a low-profile optical coupling unit

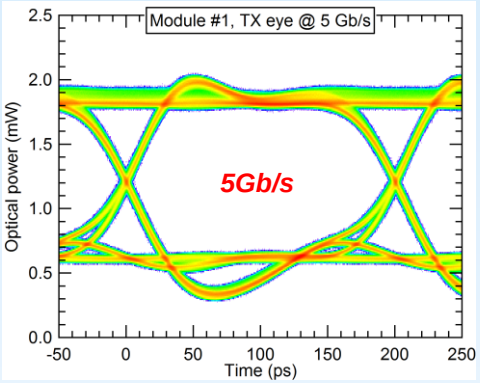


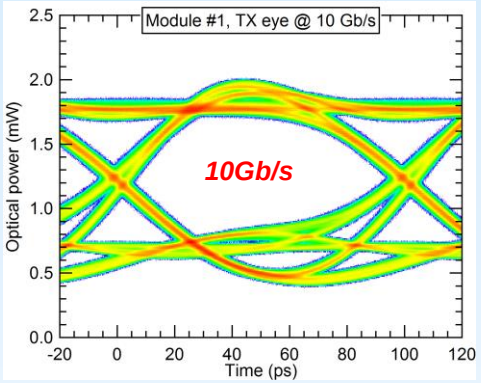
V1

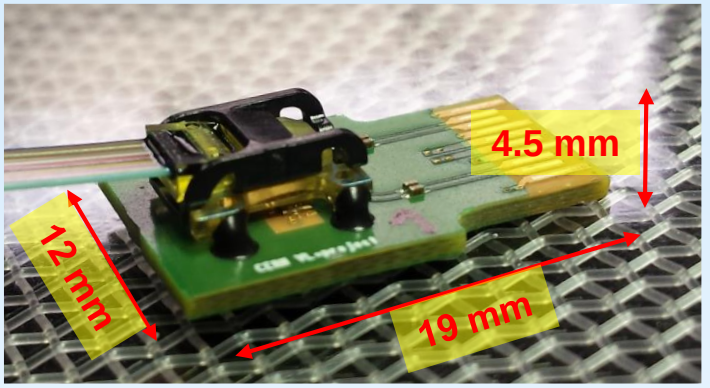


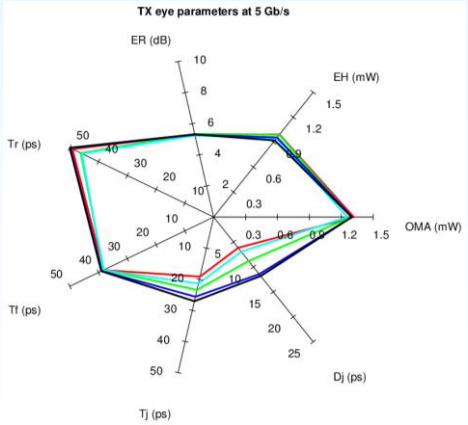
V2

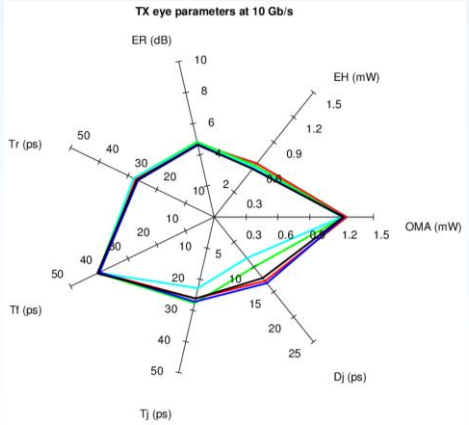
V1 prototype functional tests

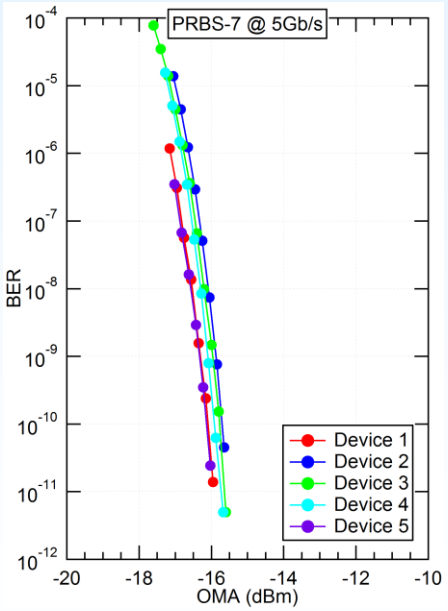




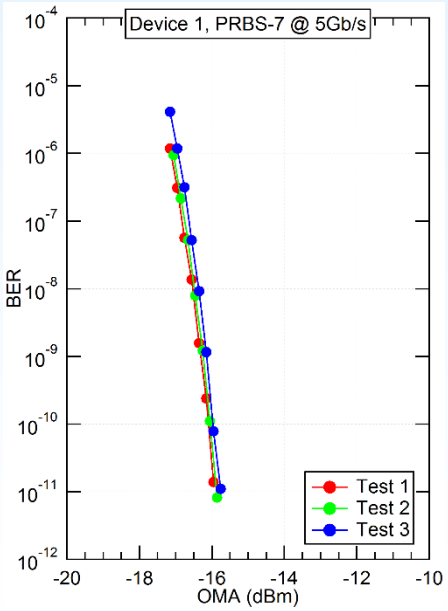








All prototypes



1 device
optical mating/demating

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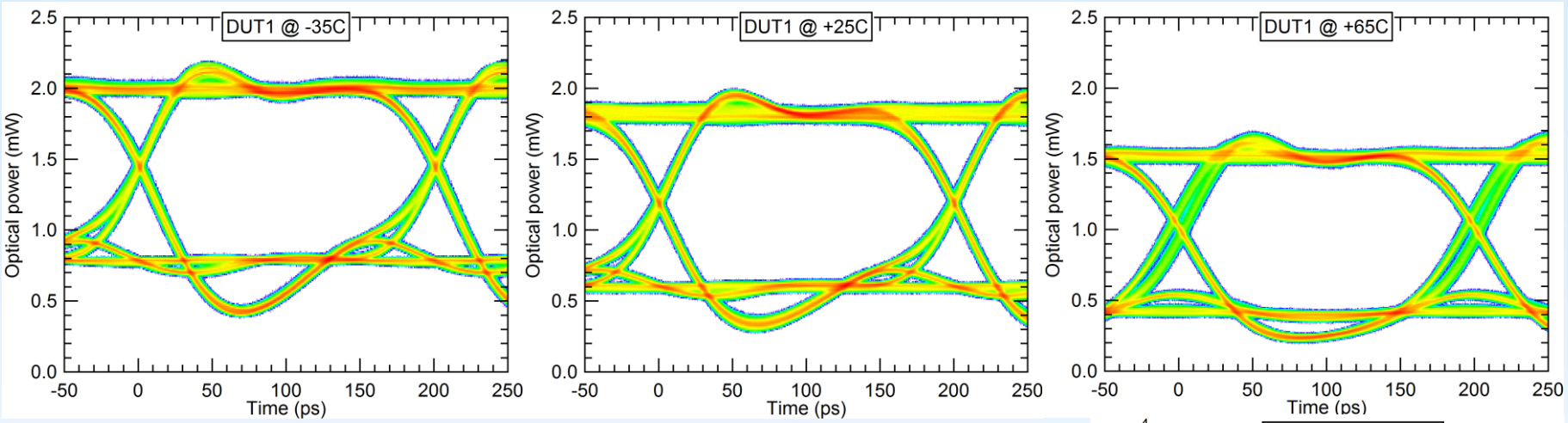
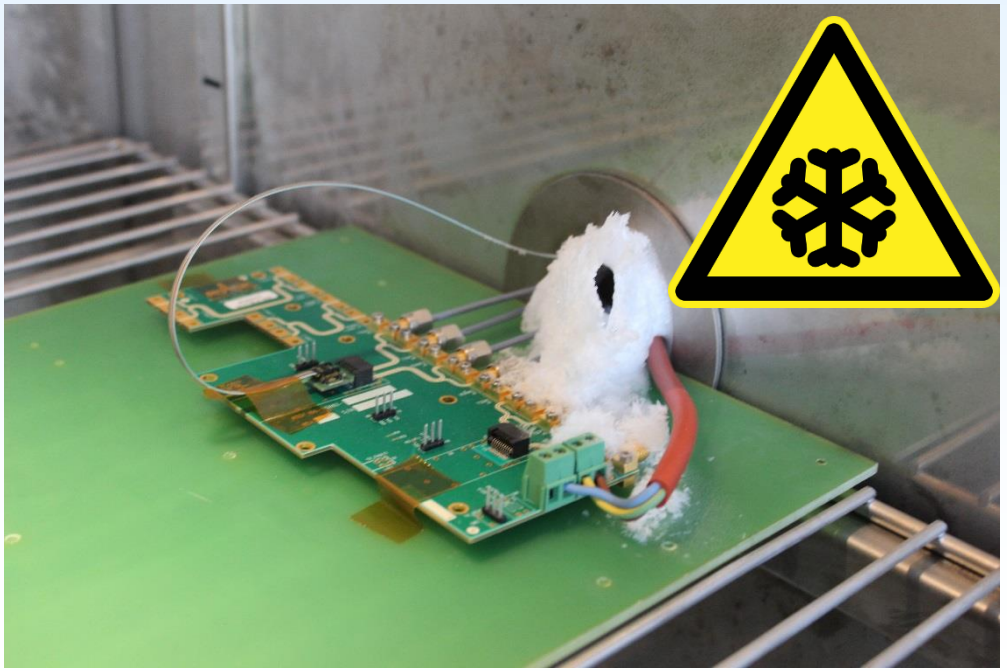
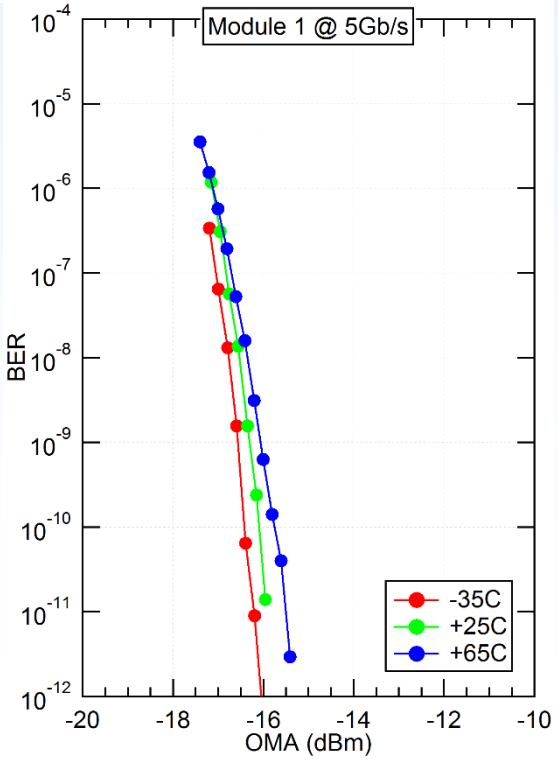
V1 prototype climate chamber test







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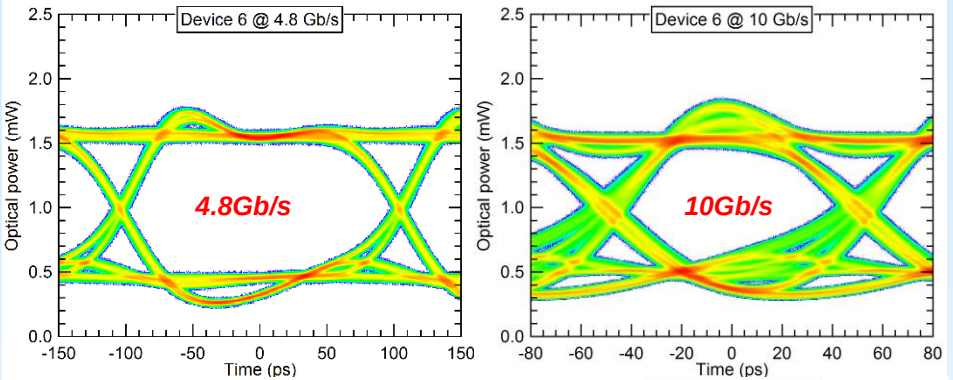
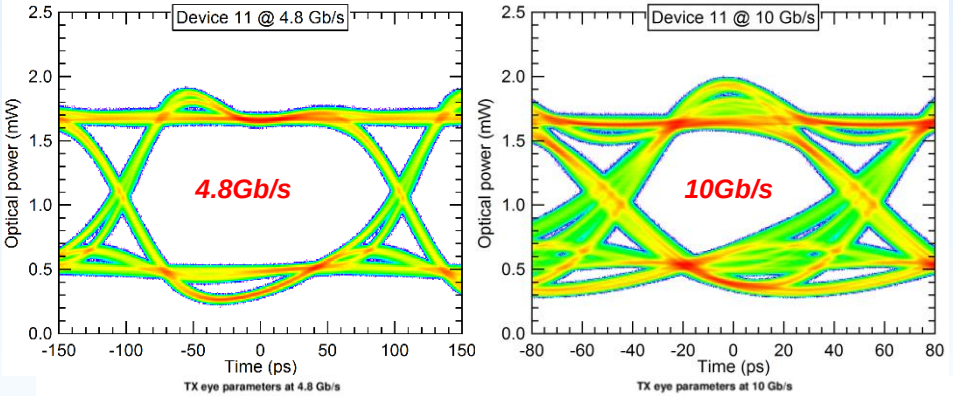
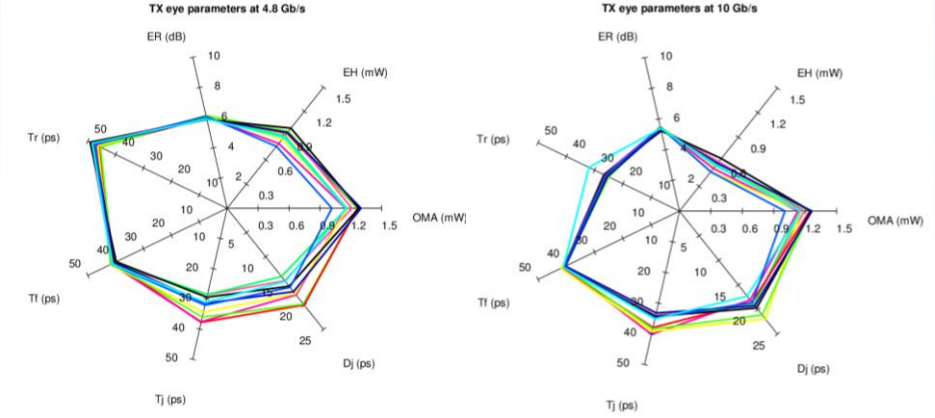
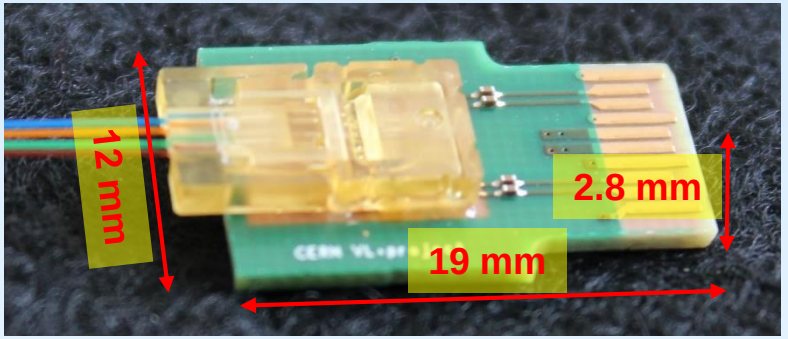
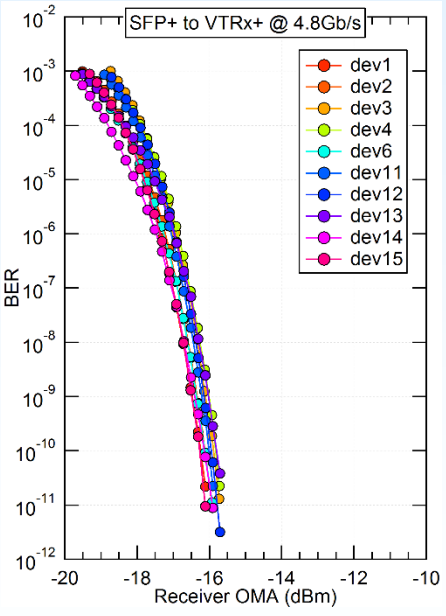
V2 prototype functional test



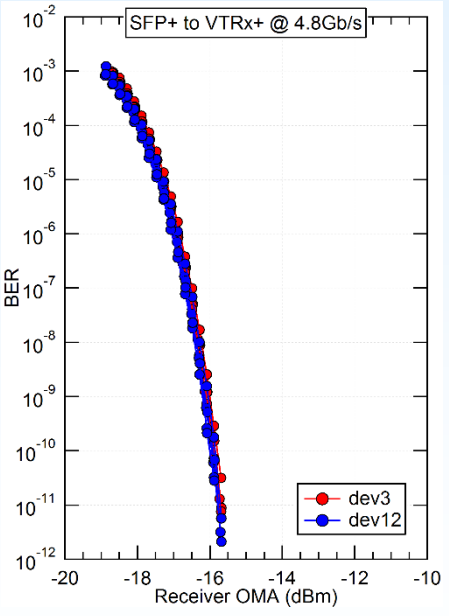








All prototypes



2 prototypes
optical mating/demating

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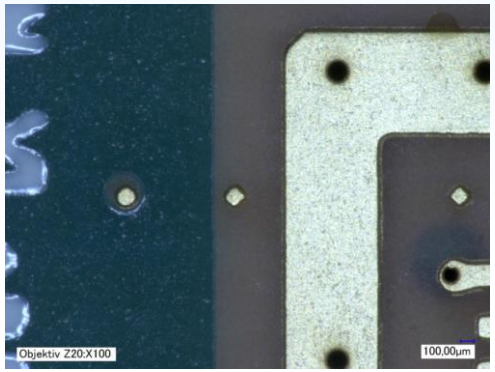
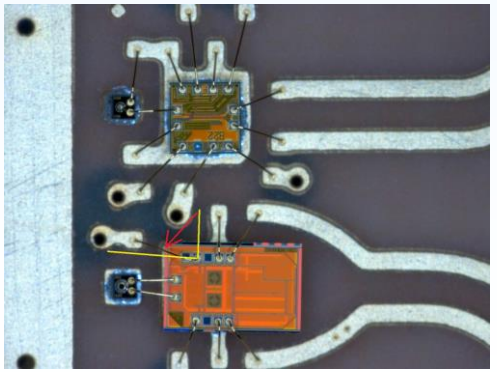
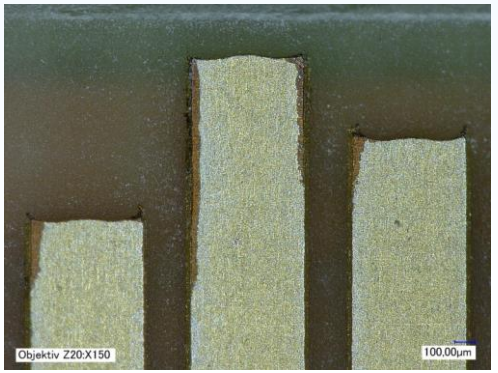
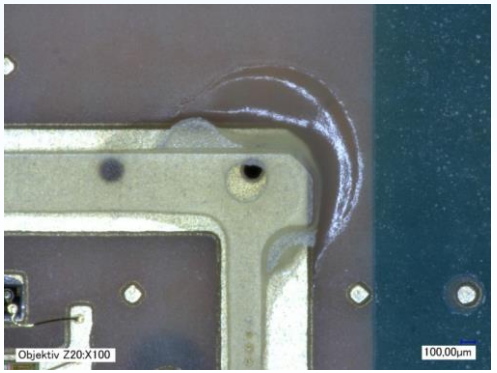
Lessons learnt

- Layout should be improved
  - Larger die pads, better alignment marks
  - Pad position should take into account bonding loops
- PCB quality is crucial
  - Shear test revealed PCB metallization quality issues (V2)
  - Via holes need to be plugged – tooling and air bubbles in adhesives
- Changed PCB manufacturer (V3)
  - Better quality to be confirmed by the assembly house

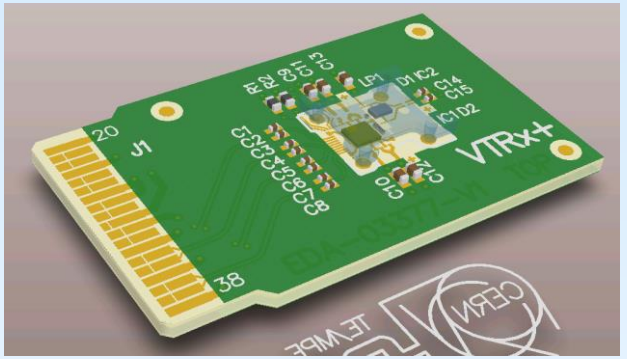


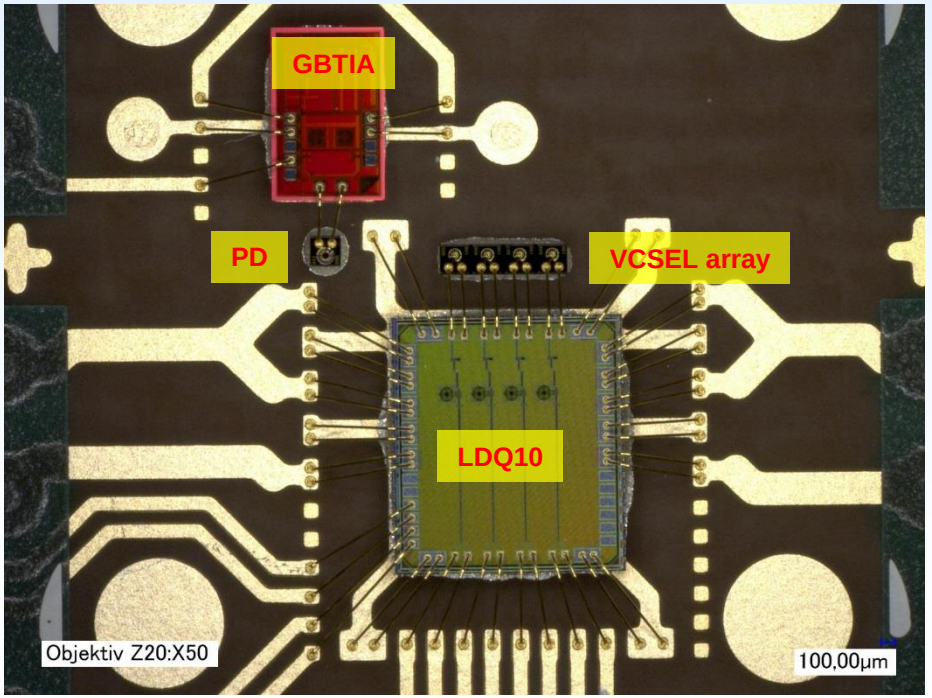





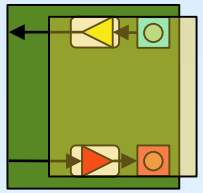
Custom VL+ front-end – V3

- First prototype based on custom ASICs and commercial optical components
  - Quad laser driver (SMU) and CERN radiation tolerant TIA (GBTIA)
  - 14 Gb/s VCSEL array/photodiode from Philips Photonics (ULM)
- US conec's MOI
- QSFP interface
  - 4 Tx + 1 Rx configuration
- Assembled by the same industrial partner
- See the submitted paper for results

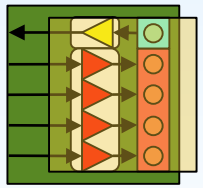




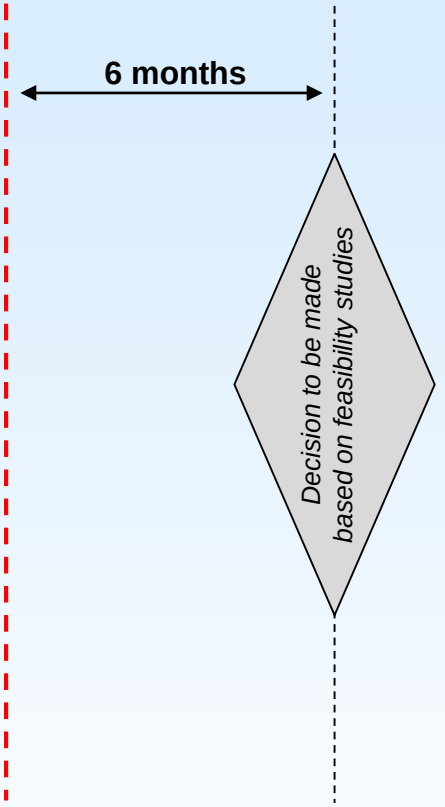
Custom module development roadmap



2ch variant	2ch TRx v1	2ch TRx v2
Opto I/F	MOI	Low-profile
Electrical I/F	SFP+	SFP+
Rx	CERN TIA	CERN TIA
Tx	Commercial LDD	Commercial LDD



4ch variant	4ch TRx v1
Opto I/F	MOI
Electrical I/F	QSFP
Rx	GBTIA
Tx	LDD array



Q3'15	Q4'15	Q1'16	Q2'16	Q3'16	Q4'16	Q1'17

Legend:

MOI	**– Mechanical Optical Interface**
GBTIA	**– CERN receiver ASIC**
GBLD10+	**– CERN single-channel VCSEL driver ASIC**
LDD array	**– 4-channel Laser Diode Driver array**

Customisation Outlook

- Build new prototype based on custom ASICs
  - GBTIA + GBLD10+ (LDQ10 as fall-back)
- Investigate solutions enabling lower height
  - Ultra low-profile connector, interposer or soldering
  - Thin substrate
  - Flexible substrate
- Market Survey for finding more assemblers
- Start reliability and environmental (T, irradiation) tests

Summary

- We made a lot of progress in the 2nd phase of the Versatile Link PLUS project
- Market survey has been launched to identify firms willing to work with CERN on transceiver customisation
- 3 full custom prototypes have been designed by CERN and have been manufactured by an industrial partner
- Functional tests carried out in the laboratory prove the good performance of the assembled prototypes
- Further iteration is required to satisfy the needs of the most exacting applications
- Feasibility demo shall take place by Q2/2017