Fabrication of the first 3D Vertical JFET at the IMB-CNM

A rad-hard switch for the ATLAS Inner Tracker

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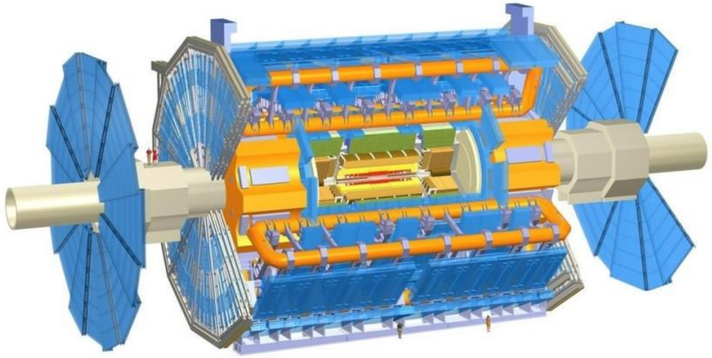
Outline

- **Motivation**
  - Controlled switch for the powering scheme of the ATLAS upgrade ITk
- **Introduction**
  - Custom Silicon V-JFET based on 3D trenched technology:
    - *Main Features, Operation and Design*
- **First Fabricated Batch**
  1. Design of experiments
  2. Process Technology
  3. Electrical Performance
  4. Performance at low temperature
  5. Performance after ionizing irradiation (gamma)
- **Conclusions and future work**

Motivation – 1. Powering Scheme in the ITk

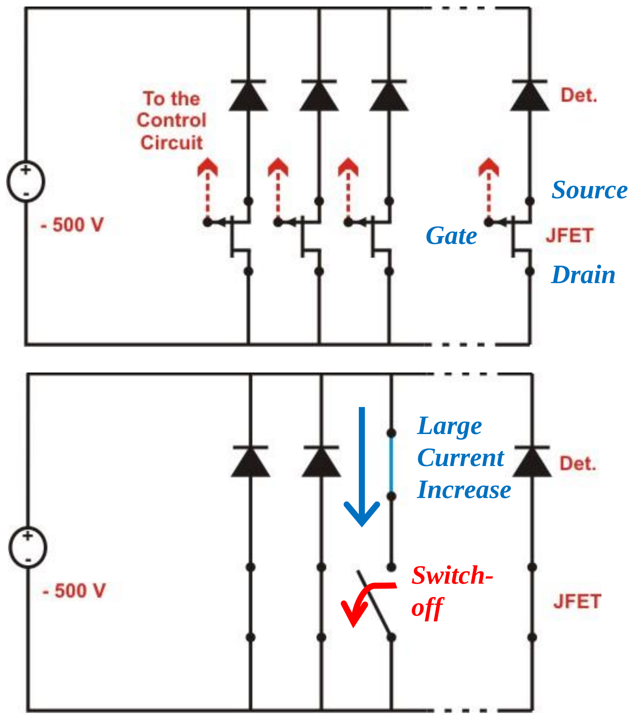


ATLAS experiment @ CERN

Upgrade for High Luminosity

- Higher performance, Higher compactness, Higher radiation hardness…

<u>Switch Goal</u>: *To switch-off a **malfunctioning sensor** when it demands too much current to the power supply*



- **Powering scheme for the strips detectors of the Inner Tracker (the HV-MUX system) requires radiation-hard switches.**
  - **500 – 700 V detector bias**
  - **Forward current: > 5 mA**
  - **Reverse current: < 1 mA (after irradiation)**
  - **Maximum radiation levels:**
    - **Fluence: 2×10^{15} 1-MeV eq. neutrons/cm^2**
    - **Total Ionizing Dose: 50 Mrad(Si)**

Targeted production of 20k devices

Motivation – 2. Controlled Switch Candidates

Silicon

- Insulated Gate Transistors (**MOSFET**, **IGBT**): Gate oxide degradation by ionization damage prevents their use.
- **Thyristors**: Difficult turn-off and complex control circuitry. Not feasible for the application.
- **JFET**: Optimal candidate, but:
  - N-type substrates too sensitive to radiation displacement damage (undergo type inversion under high fluences).
  - P-type JFET: lack of commercially available devices.

Silicon Carbide

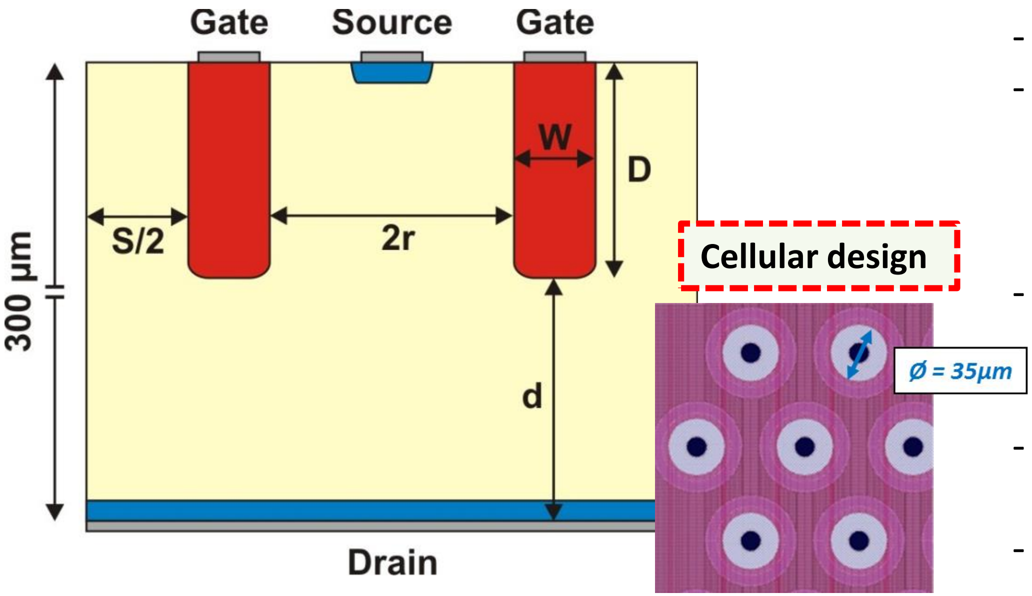
- Commercial **JFETs** have been tested: Most of them fail. The only surviving device is no longer sold.

Gallium Nitride

- Commercial **HEMTs** have been tested: Good performance of one candidate, but:
  - Normally-Off device: need for continuous control voltage.
  - Technology not mature; long term radiation damage in GaN still to be fully understood.

Introduction – 1. Silicon Custom V-JFET

- **Custom Silicon Vertical JFET based on the 3D-trench technology implemented at CNM-Barcelona for 3D detectors.**

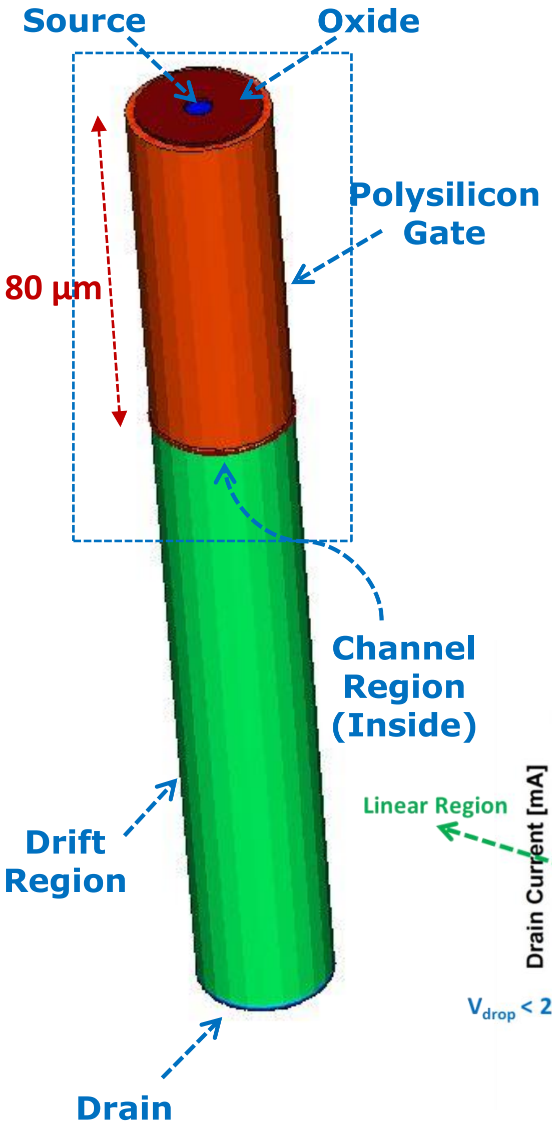


- **Each cell presents a conduction channel, surrounded by a deep trench (with circular or hexagonal layout), which constitutes de gate electrode.**
- **The channel current is modulated by the depletion region extended from the gate-substrate reverse-biased junction**

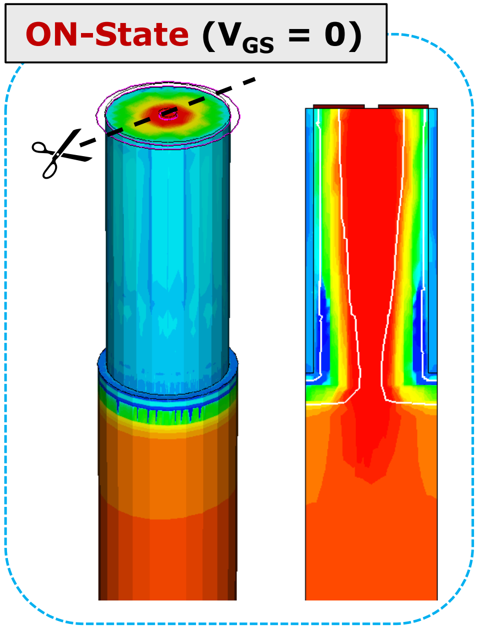
- **Features:**
  - **Depletion mode device** → (Normally ON)
  - **3D Device** with **Vertical Conduction**
    - → High voltage capabilities
    - → Rad-hard against ionization
    - → Low switching-off voltage
  - **P-type**
    - → Rad-harder against displacement (at least, damage mechanisms are known)
  - **Cellular design**
    - → Adaptable Current capability
  - **Custom made**
    - → Optimization for the requirements

Figures of merit in terms of several geometric parameters evaluated for an optimum design (2D TCAD simulation)

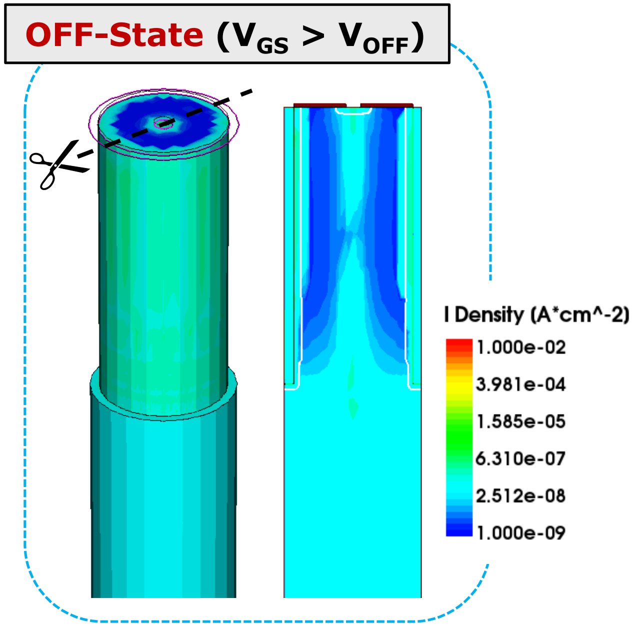
Introduction – 2. V-JFET cell: How it works?

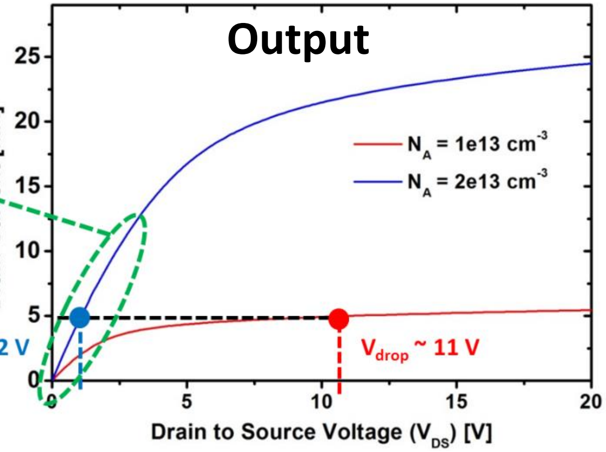


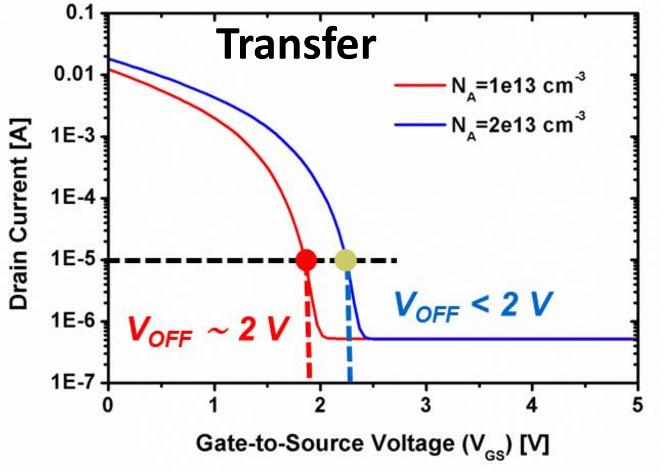
ON-State ($V_{GS} = 0$)



OFF-State ($V_{GS} > V_{OFF}$)

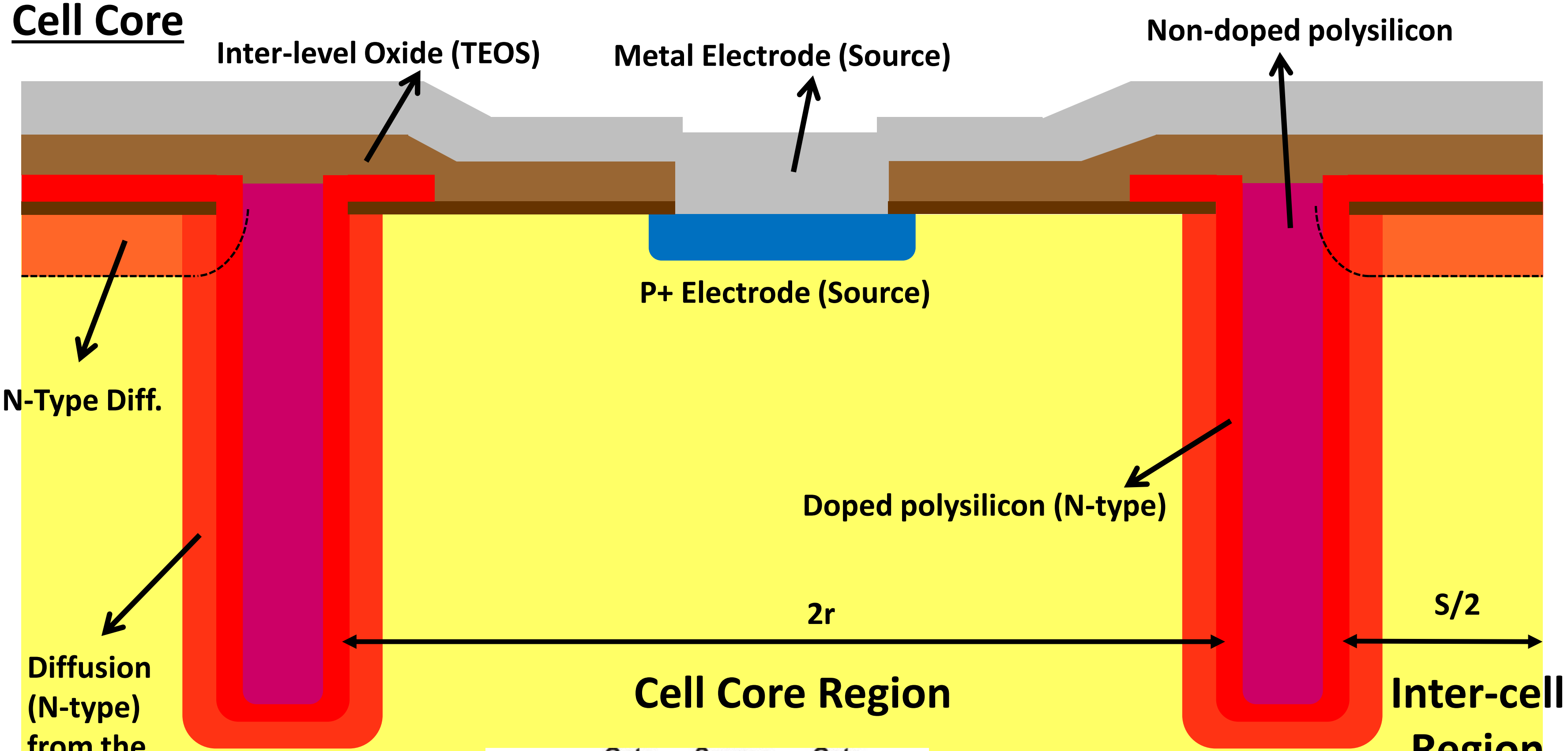






Introduction – 3. Device Structure

Cell Core



Inter-level Oxide (TEOS)

Metal Electrode (Source)

Non-doped polysilicon

P+ Electrode (Source)

N-Type Diff.

Doped polysilicon (N-type)

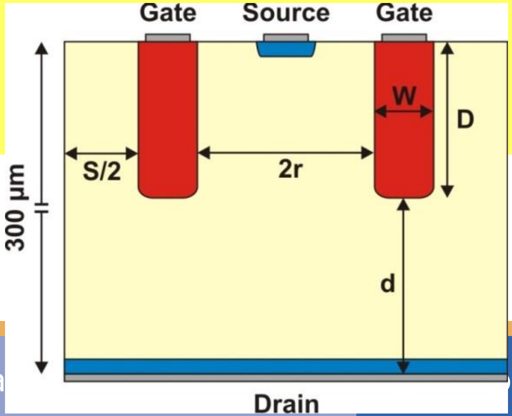
2r

S/2

Diffusion (N-type) from the Doped polysilicon

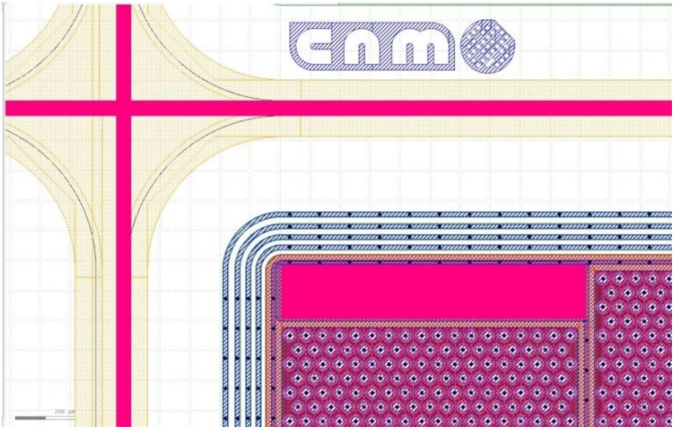
Cell Core Region

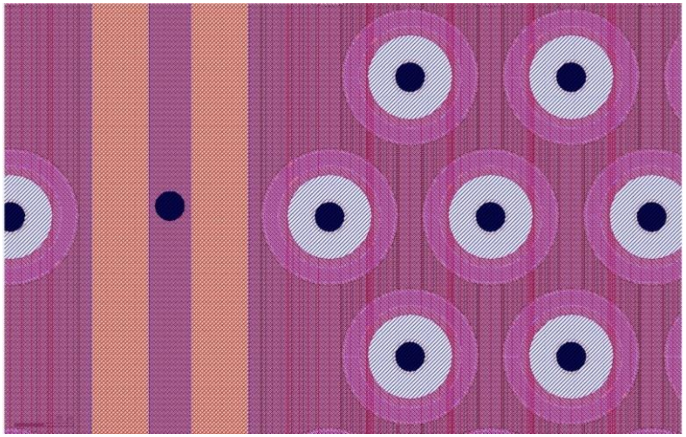
Inter-cell Region

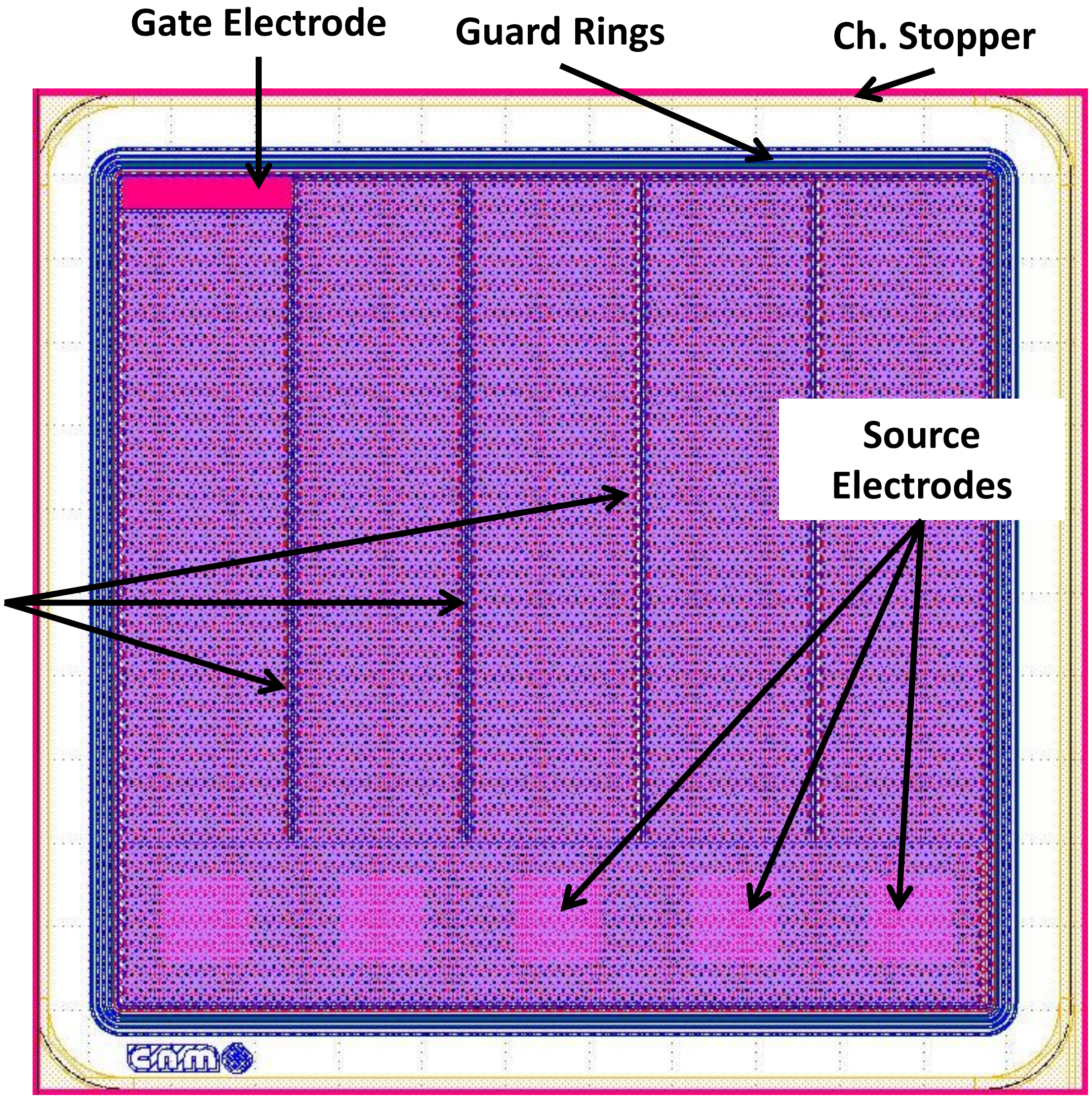


Introduction – 4. Device Layout

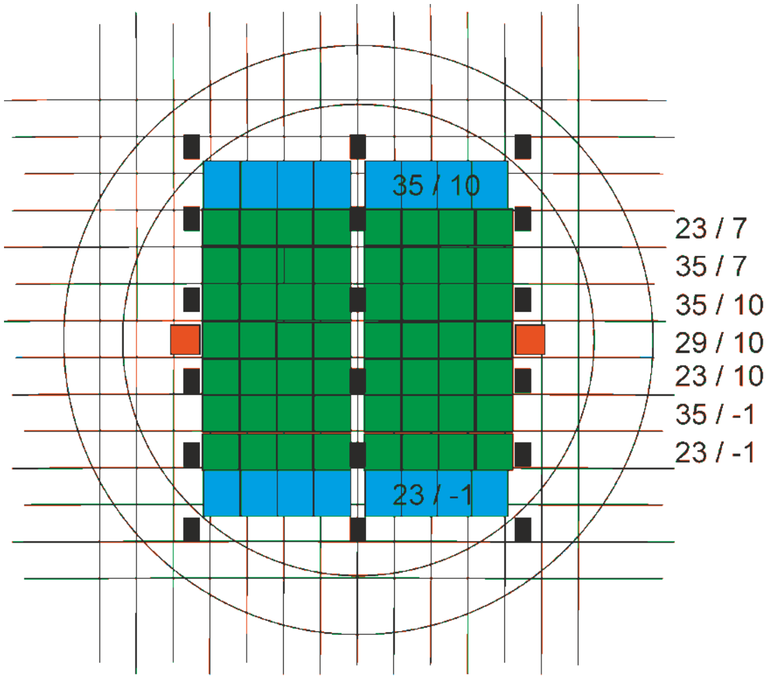
7 photolithographic levels



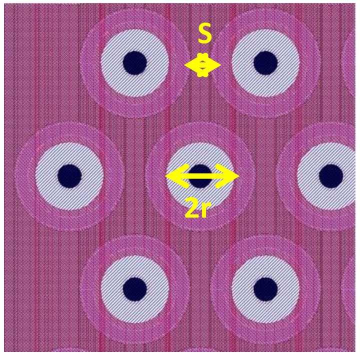




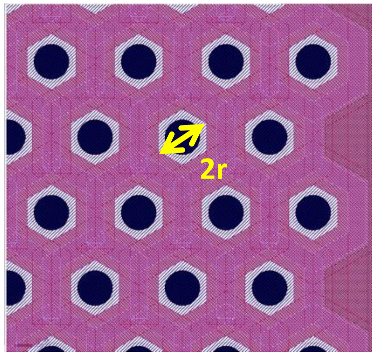
First Batch – 1. Design of Experiments



Circular



Hexagonal



Design

Device Design (parameter values)

- 7 Designs with different 2r and/or S (6x6 mm²) (green)

S\2r	23	29	35
10	X	X	XX
7	X		X
0 (Hex)	XX		X

- 2 Additional designs with 8.9x6 mm² (blue)

Technology

P-Spray Strategy

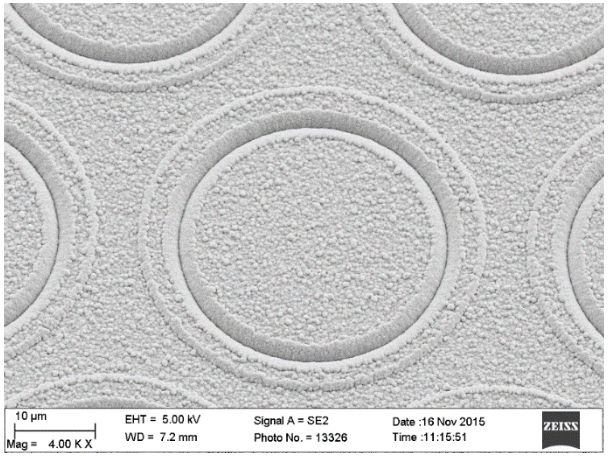
	Dose [cm^{-2}]
w/o P-Spray	-
With P-Spray	1e12
With P-Pray	5e12

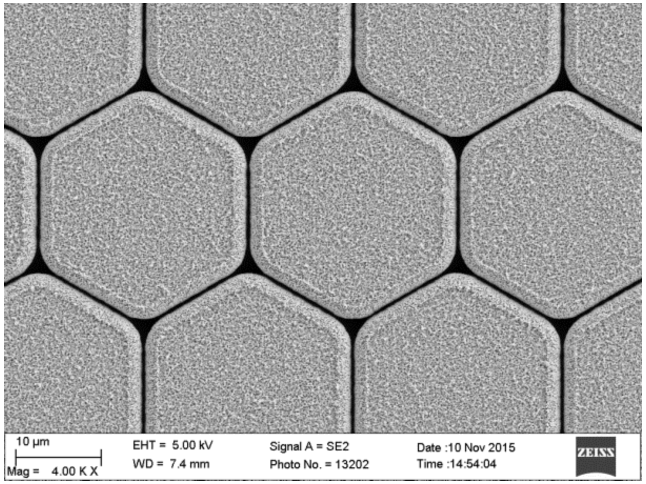
Substrate Doping

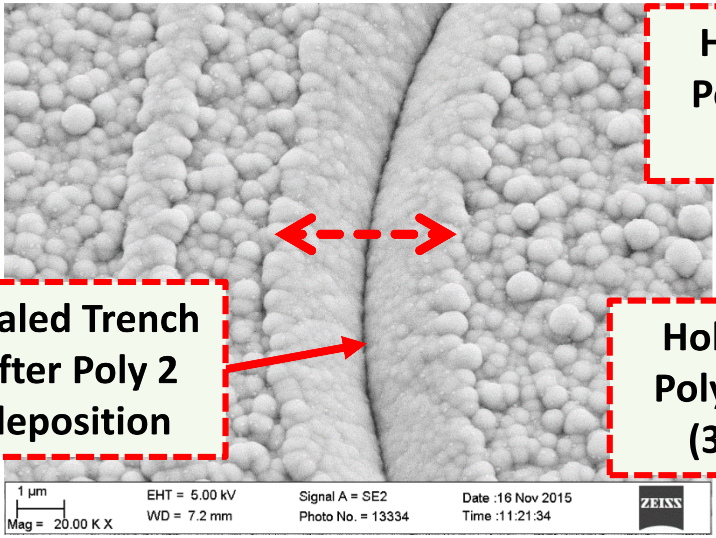
- "Low-Resistivity" (150-500 Ω·cm) → Lower V_{drop}
- ~~"High-Resistivity" (500-1000 Ω·cm) → Lower V_{OFF}~~

First Batch – 2. Process Technology

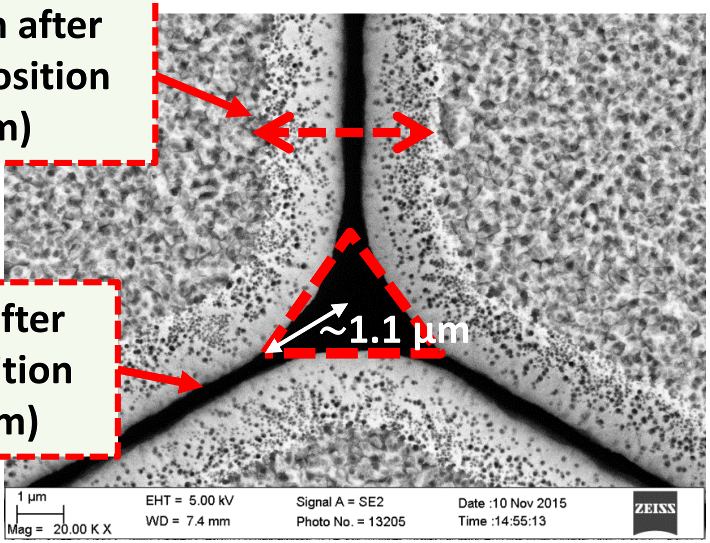
- **Circular designs became sealed; honeycomb designs were not completely filled**







Sealed Trench after Poly 2 deposition

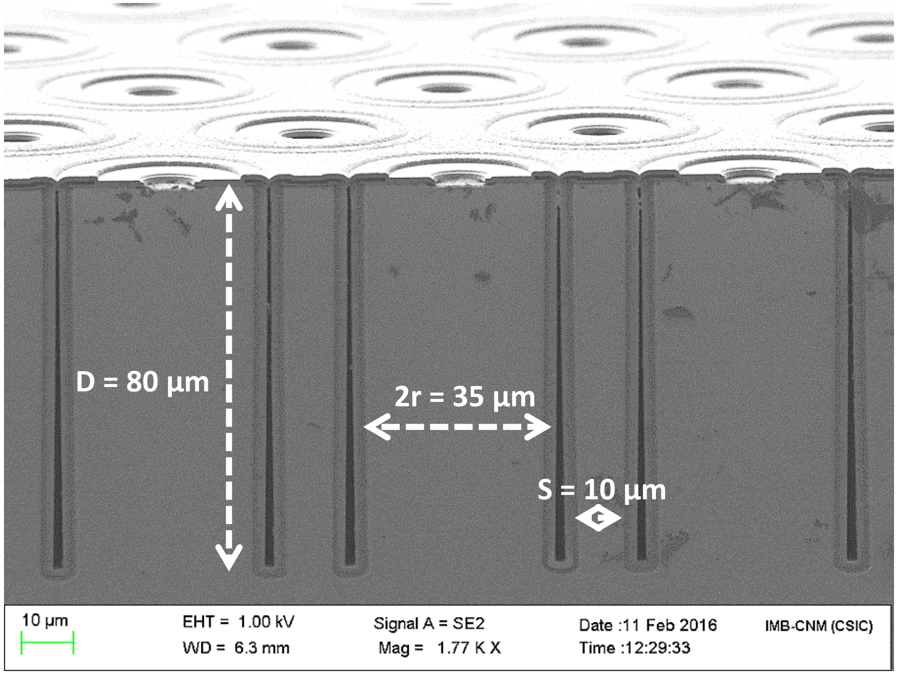


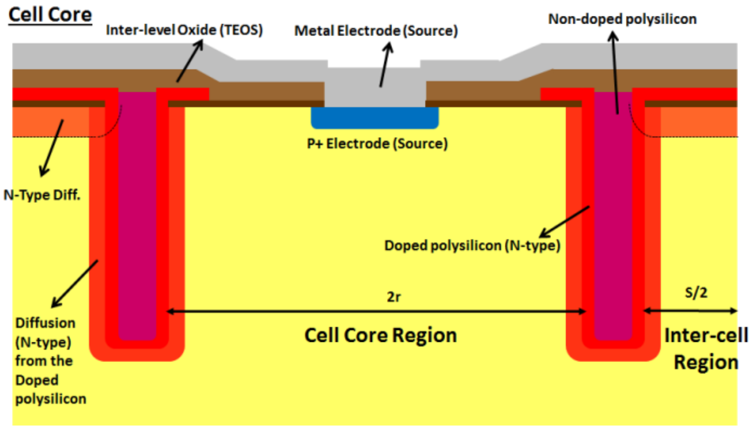
Hole width after Poly 1 deposition (< 3 µm)

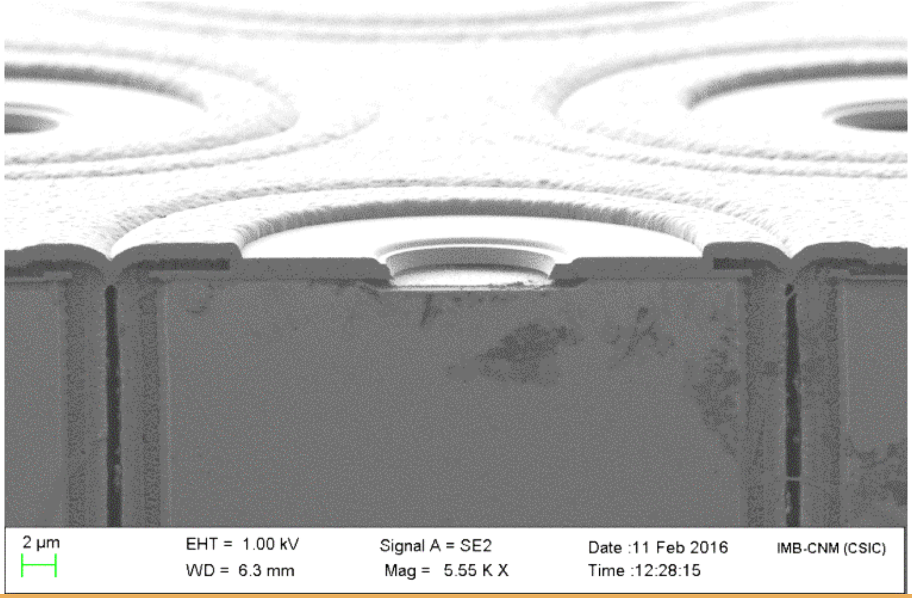
Hole width after Poly 2 deposition (350-480 nm)

First Batch – 2. Process Technology

- **Cross Section (SEM images)**



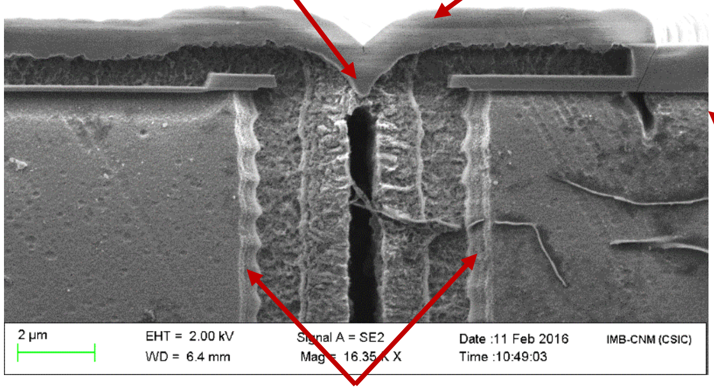




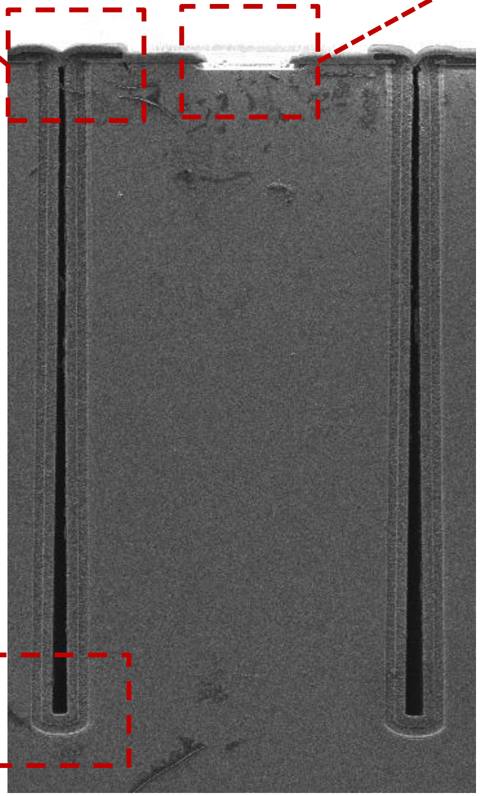
First Batch – 2. Process Technology

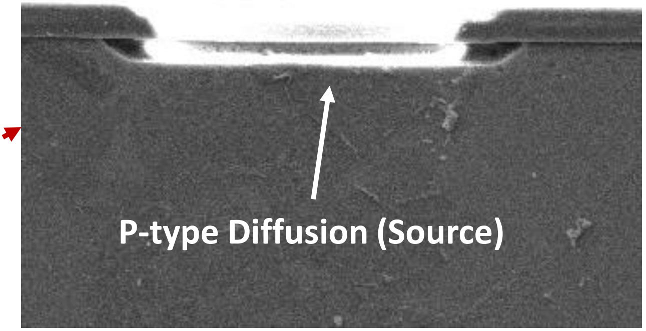
Trenches are sealed

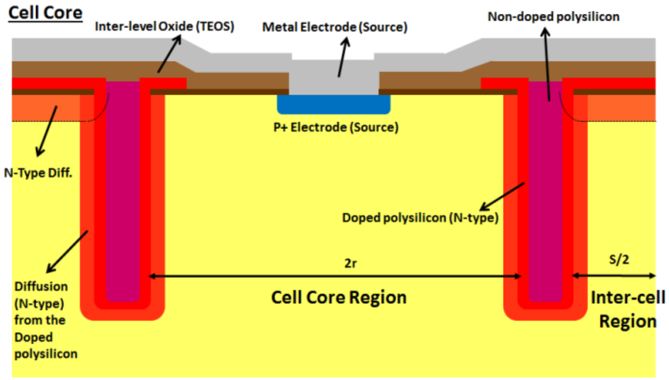
Inter-level Oxide

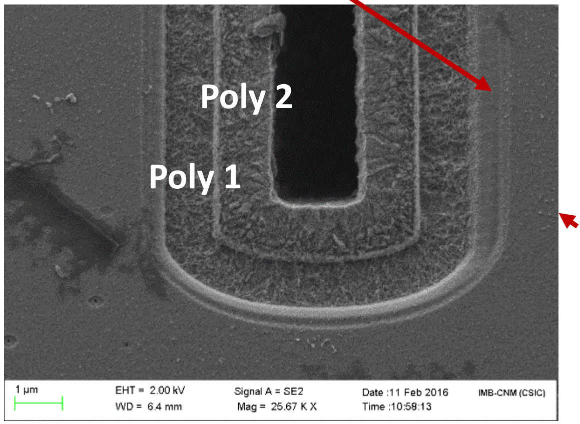


N-type diffusion from Poly 1



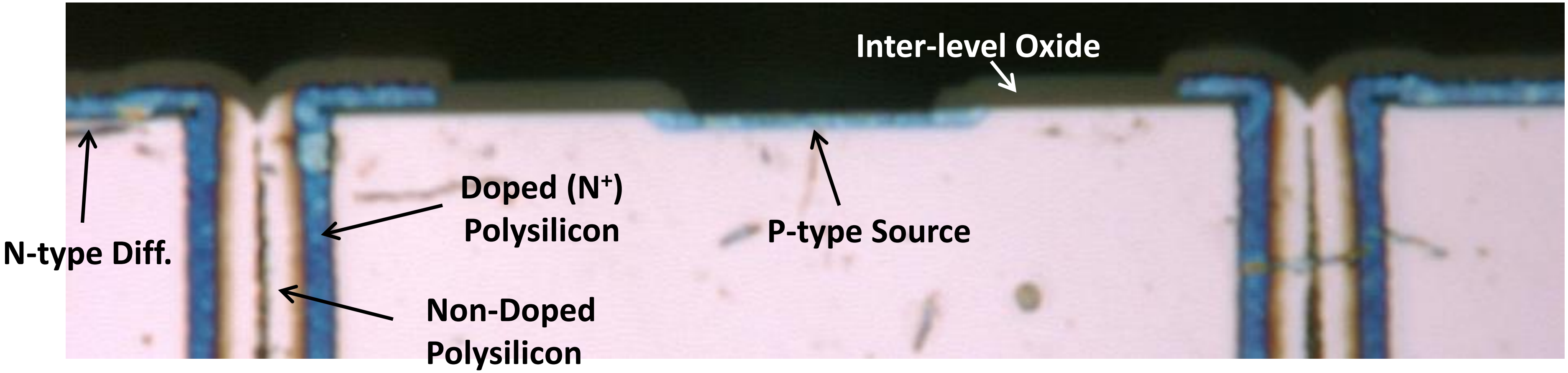


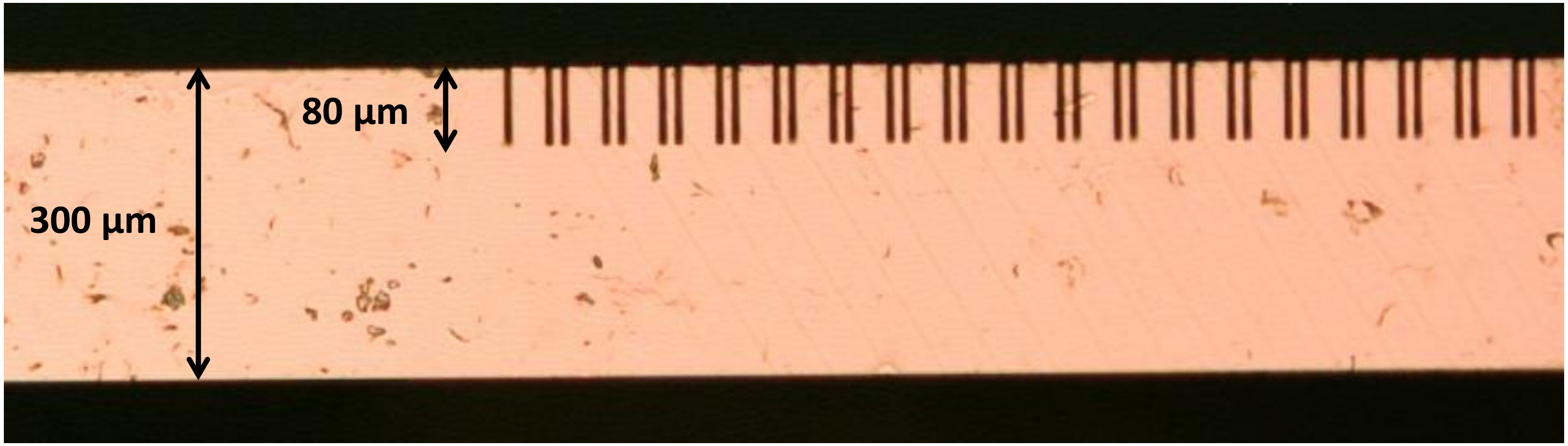




First Batch – 2. Process Technology

- **Optical microscope**

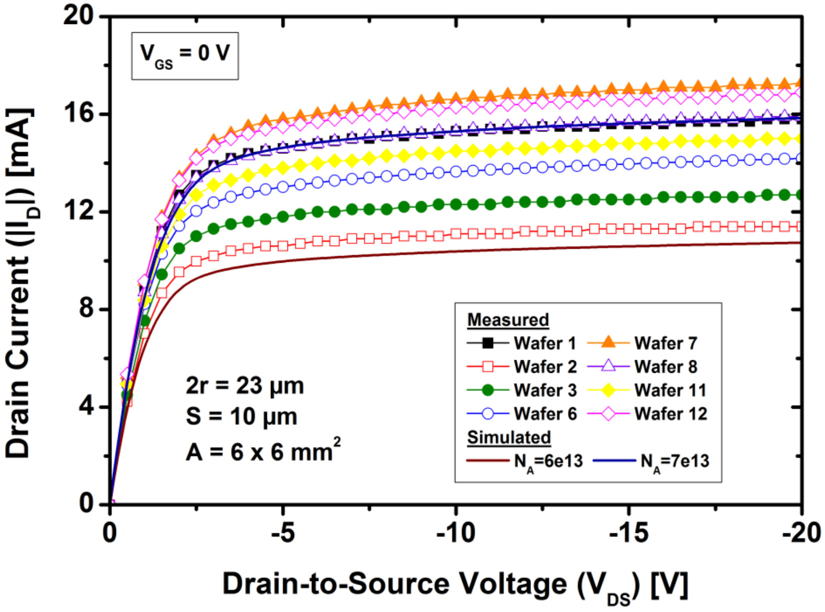




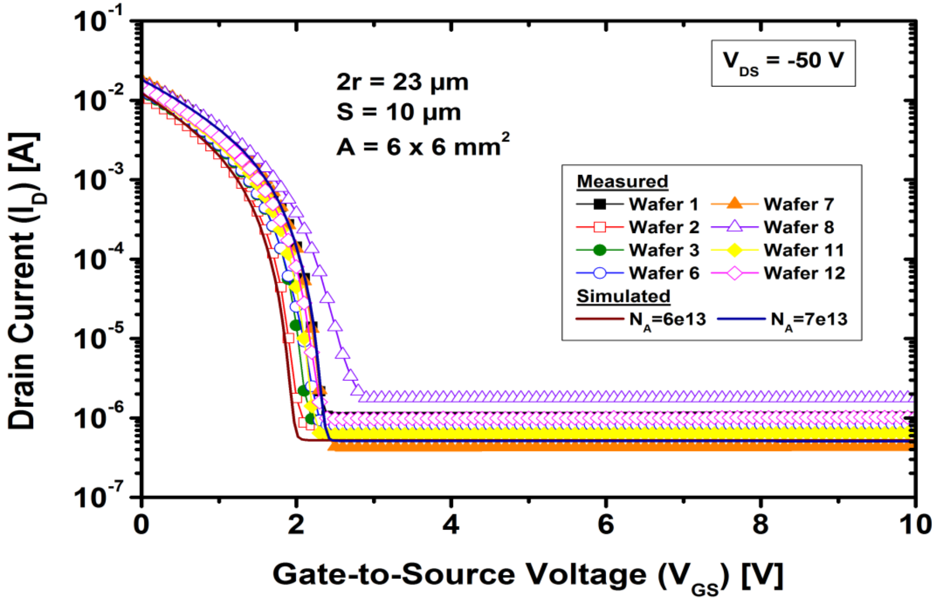
First Batch – 3. Electrical Performance

2r = 23 µm; s = 10 µm

Output Characteristic



Transfer Characteristic



- **Narrow* channel devices:**
  - ✓ **High enough current**
  - ✓ **Low enough V_{OFF}**
  - → **Close to target device**
- **Good agreement with simulations**
  - → **Confirms simulation results**
- **Good starting point for fine optimization**

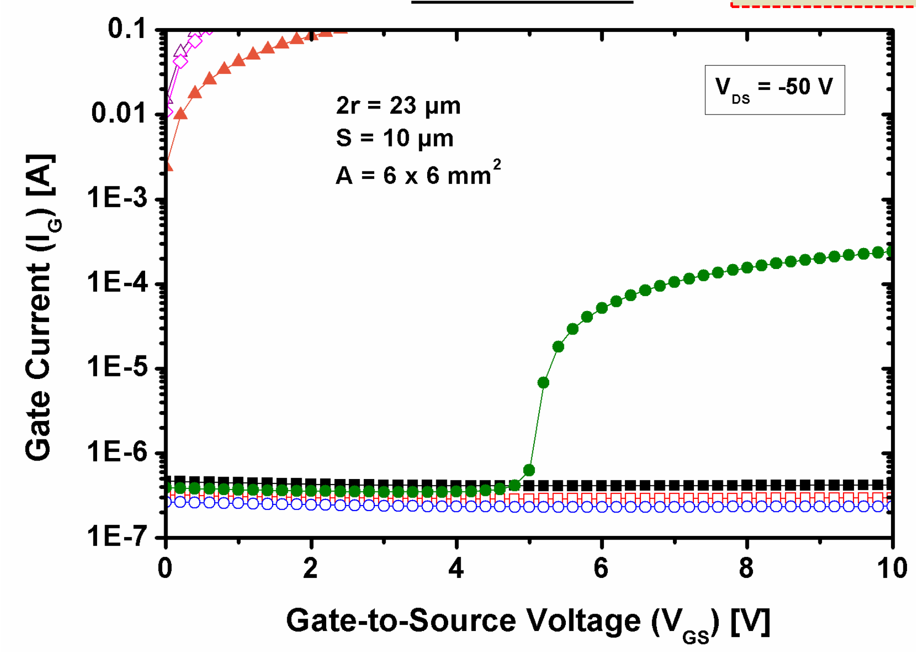
	I_{DSS} (I_{DS}@V_{DS}=-50V)	V_{drop} (V_{DS} @I_{DS}=5mA)	V_{OFF} (V_{GS} @ I_{DS} =10 µA)	I_{OFF} (I_{DS}@V_{GS}=10V)
Measured	12 – 18 mA	0.46 – 0.64 V	1.90 – 2.55 V	0.4 – 1.7 µA
Sim (6e13)	11 mA	0.68 V	1.85 V	0.5 µA
Sim (7e13)	17 mA	0.50 V	2.25 V	0.5 µA

* Wider cannel devices show good characteristics but V_{OFF} is higher than required

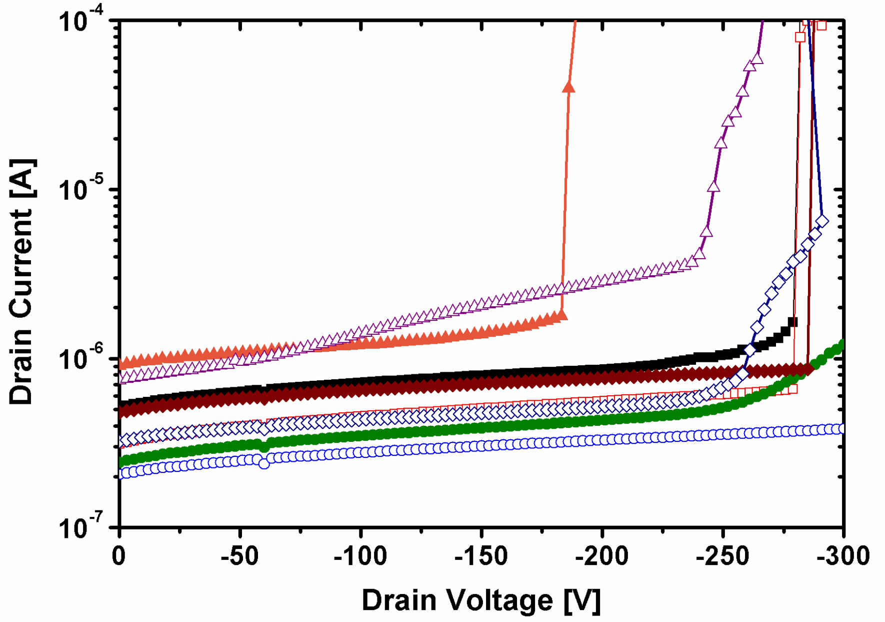
First Batch – 3. Electrical Performance

2r = 23 µm; s = 10 µm

Gate current



Voltage capability



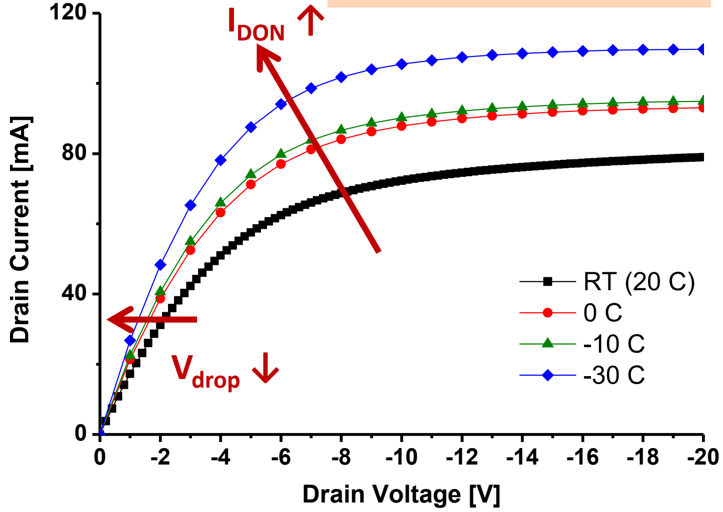
- **Most devices show Gate current < 1 µA**
- **Some devices show high Gate current**
- **Other devices show I_G increase when biased in the off-state**
  - ➢ Inter-level oxide pin-holes may totally or partially short Source and Gate Metals

- **Breakdown voltage < 300 V**
  - ➢ Edge termination (with 4 floating guard rings) is not optimized for the used substrate doping

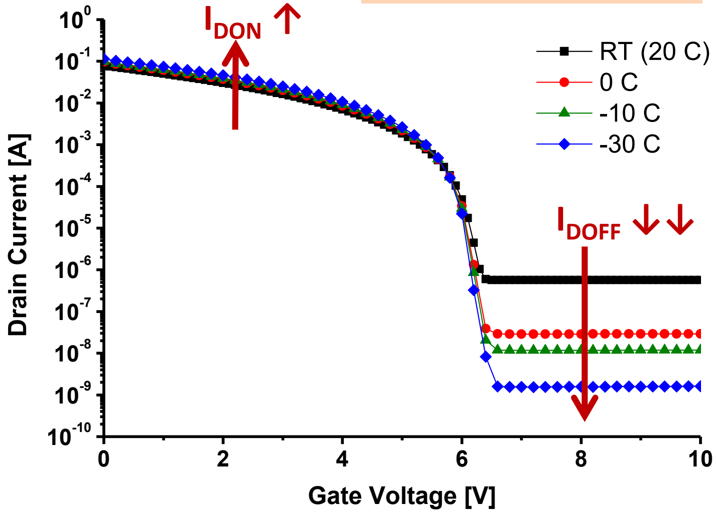
Future improvements:
- Batch with higher substrate resistivity (On going)
- Improved inter-level oxide quality (On going)
- Revisited edge termination strategy

First Batch – 4. Performance at low Temperature

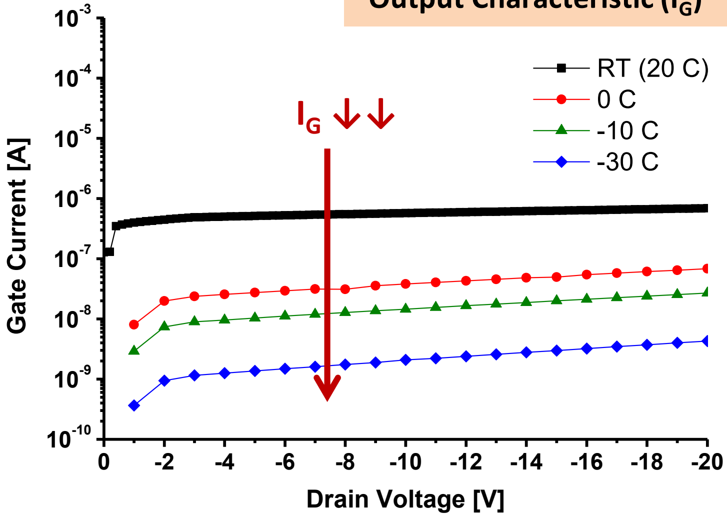
Output Characteristic (I_D)



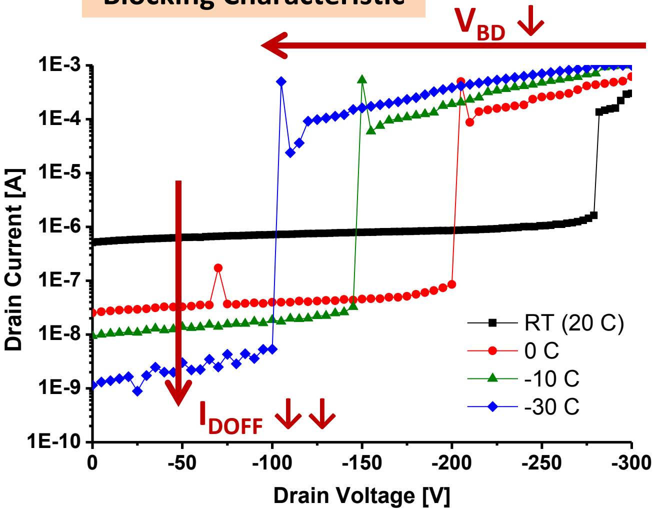
Transfer Characteristic



Output Characteristic (I_G)

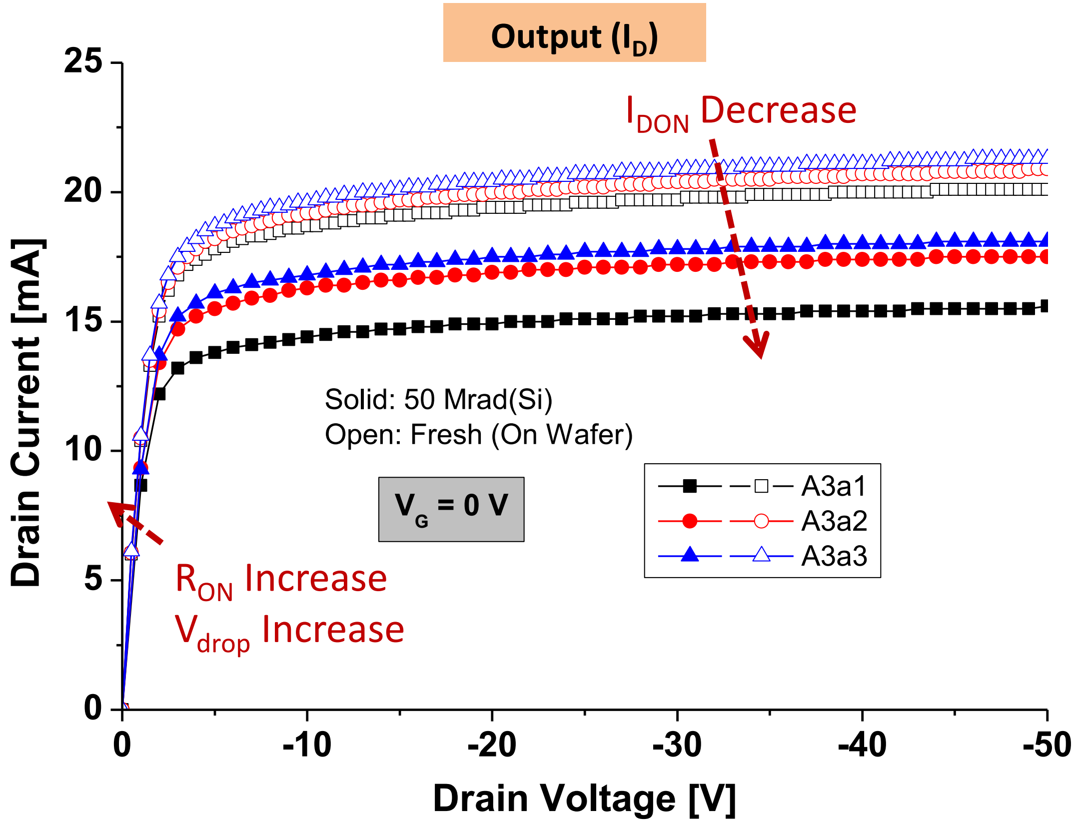


Blocking Characteristic



First Batch – 5. Performance after ionizing irradiation

Gamma irradiations at the CIEMAT (Madrid): up to 100 Mrad(Si)



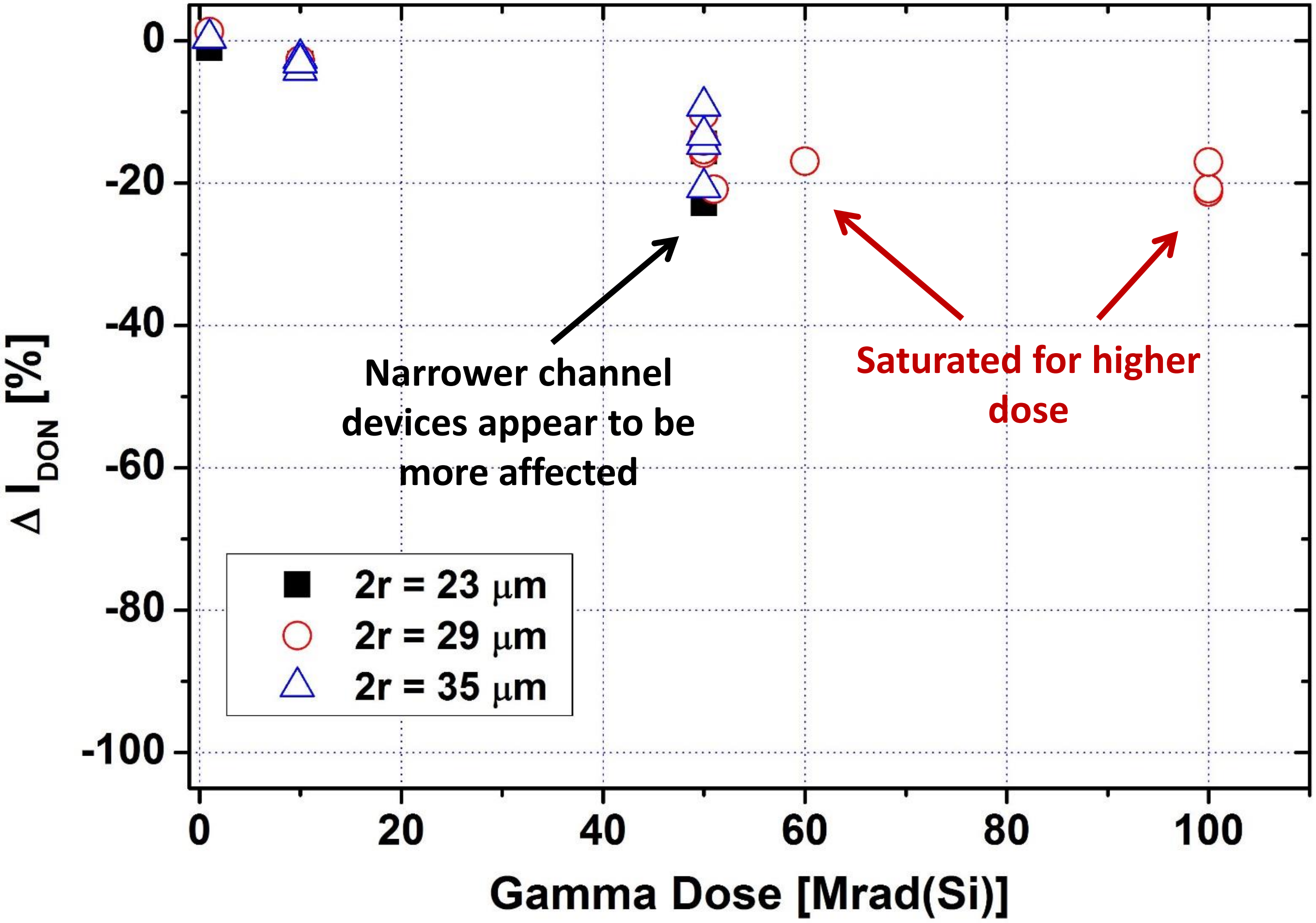
1. **Notable reduction of the On-State Drain Current**
2. **R_{ON} (and V_{drop}) become slightly increased**
3. **The other FoM result unaffected**

Bottom line:

Devices are fully operative and meeting specs after100 Mrad(Si) ionizing irradiation

First Batch – 5. Performance after ionizing irradiation

- **Reduction of the On-State Drain Current**

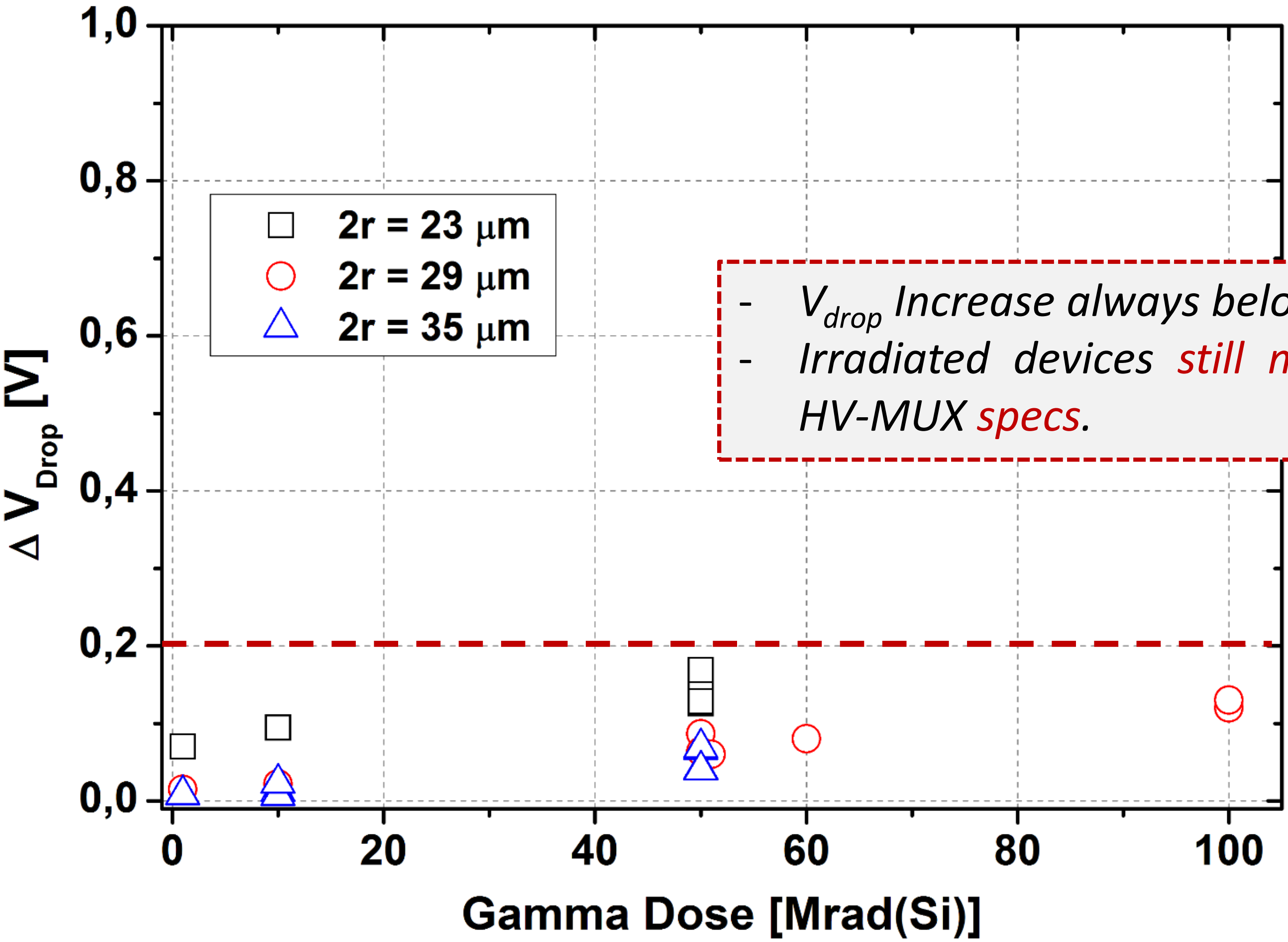


Narrower channel devices appear to be more affected

Saturated for higher dose

First Batch – 5. Performance after ionizing irradiation

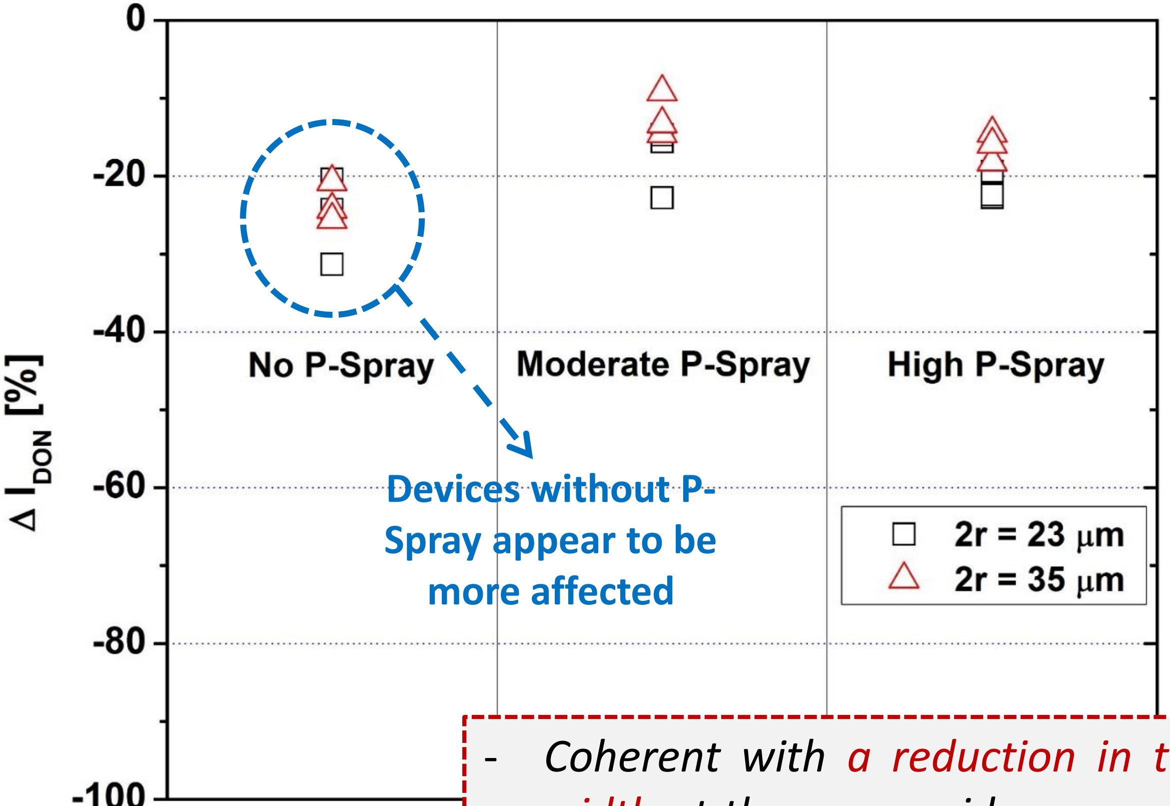
- <u>Consequence:</u> Increase of the voltage drop (V_{drop}) in the sensor bias



- *V_{drop} Increase always below 0.2 V*
- *Irradiated devices still meeting the HV-MUX specs.*

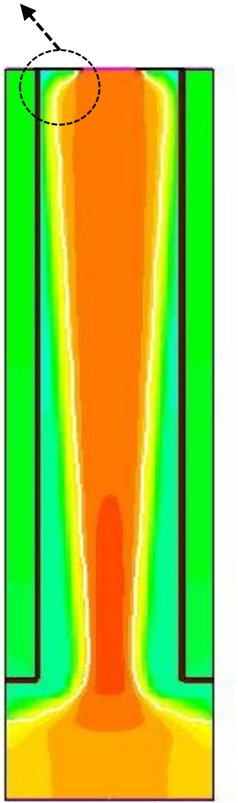
First Batch – 5. Performance after ionizing irradiation

- **Reduction of the On-State Drain Current**



Devices without P-Spray appear to be more affected

Possible channel narrowing?

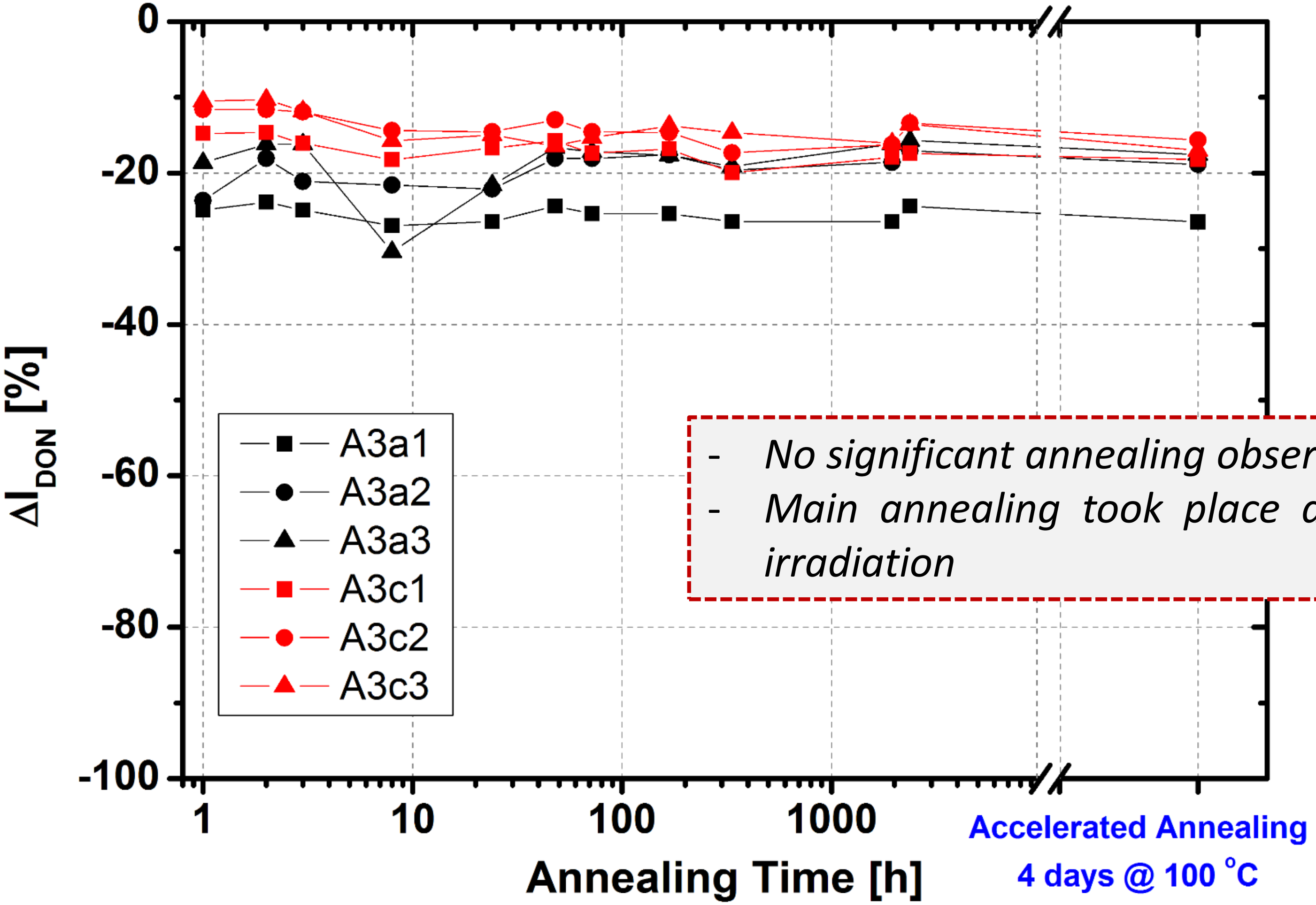


Current density

- *Coherent with a reduction in the channel width at the source side, as a consequence of the accumulated charge in the oxide.*

First Batch – 5. Performance after ionizing irradiation

- **Annealing**



- *No significant annealing observed*
- *Main annealing took place during irradiation*

Conclusions and Future Work

- A Silicon Custom Vertical JFET (V-JFET) is being developed at the CNM.
  - → **Based on a 3D trenched technology**
  - → **Candidate as a rad-hard switch for the HV-MUX powering scheme of the ATLAS ITk**
- First prototype batch has been already fabricated and fully characterized:
  1. Technological process:
     - → **Devices based on a circular cell design were satisfactorily fabricated**
     - → **Trench etching and filling steps are fully controlled.**
  2. Electrical performance:
     - → **On state and transfer characteristics already meet the HV-MUX specifications for the narrower cell devices**
     - → **High Gate leakage (in some devices) and low Breakdown voltage have been measured**
       - **Fully understood**
       - **Will be solve in future batches**
     - → **Performance at low temperature is in accordance with expectations**

Conclusions and Future Work

- First prototype batch has been already fabricated and fully characterized (II):

3. Performance after ionizing irradiation:
   → **Devices were irradiated with gammas up to 100 Mrad(Si)**
   - **Reduction of the forward current**
   - **Coherent with a surface narrowing of the channel**
   - **Not significant for the device application**

Future work

- Further Irradiations, on going
  → **Neutron irradiation to test displacement damage**
  - **Up to 2 x 10^{15} n_{eq}/cm^2**
  - **Already done, soon measured**

  → **Pion irradiation**
  - **Up to 1 x 10^{15} n_{eq}/cm^2**
- Second batch is under fabrication
  → **Higher substrate resistivity**
  - **Higher Breakdown voltage**

  → **Improved inter-level oxide**

Thank you!