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Fabrication of the first 3D Vertical JFET at the IMB-CNM

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A new vertical JFET technology, based on a 3D trenched design, has been developed at the IMB-CNM. Conceptually introduced in TWEPP 2015, these transistors are conceived to work as radhard switches in the HV powering scheme of the ATLAS ITk strip detectors. The first fabricated wafers have been fully characterized and the results are presented here. Device performance is very close to specifications and shows excellent agreement with simulations. Radiation tolerance is currently under study. No noticeable effect has been seen from gamma irradiations; the impact of neutron and proton irradiation will be discussed in the final contribution.

Summary

The current HV powering scheme for the strip detectors in the ATLAS upgrade ITk requires the use of slow-controlled switches to disconnect malfunctioning sensors from the bias, allowing normal operation of the remaining sensors in the same power line. Switches should survive high radiation environment, being able to sustain $>500\text{V}$ and drive several mA. As presented in TWEPP2015 conference, IMB-CNM (Barcelona) has developed a new silicon vertical JFET technology, which can fulfil the HV switch specifications.

The VJFETs present a cellular design; each cell has a p-type silicon channel surrounded by a deep trench, typically less than $100\mu\text{m}$ depth. Filled with highly doped n-type polysilicon, the trenches act as the transistor gate. Source electrode is implemented with a highly doped p-type implant at the top centre of each cell, whereas a blanket p+ implant creates the drain electrode at the back of the wafer, far enough from the trench to assure the device voltage capability. The transistor is normally operating in on-state (with $V_G=0\text{V}$), allowing current flow through the channel. If the gate is biased above a threshold value (V_{OFF}), the channel becomes fully depleted and the current flow is drastically reduced, unbiasing the corresponding sensor. The use of high resistivity substrate keeps V_{OFF} below 3V, whereas the high number of parallel cells (more than 10k) ensures a high enough current drive to keep the voltage drop across the device below 1V. In addition, the substrate choice and the vertical configuration enhance the radiation hardness of the transistors, both against displacement and ionizing damage.

The first batch has been fabricated in the IMB-CNM clean room, with a relatively low resistivity substrate ($180\text{-}650\Omega\cdot\text{cm}$), looking for the highest current capability. Several device layouts were considered, including different channel diameters (23, 29 and $35\mu\text{m}$). Characterization results show $V_{\text{OFF}} < 2\text{V}$, for the narrower channel devices, with on-state current higher than 15mA and $V_{\text{drop}} < 0.5\text{V}$, already meeting the specifications. In addition, the measured curves exhibit an excellent fit with TCAD simulations.

Most devices exhibit early breakdown at the blocking mode (High V_{DS} , with $V_G > V_{\text{OFF}}$) motivated by the moderate resistivity of the silicon substrates. This is now under study and will be carefully addressed in the final contribution, including IR thermography analysis, simulation prospects for higher resistivity substrates and additional measurements.

Concerning radiation hardness, the first prototypes have been gamma irradiated up to 10Mrad(Si), with no noticeable effects on their characteristics, as predicted from simulations. 50Mrad(Si) irradiation has been also scheduled and the results will be presented in the final contribution. Neutron and proton irradiation are also programmed to study the impact of displacement damage on the VJFET performance.

An additional batch is now under fabrication, with higher resistivity substrates, in order to increase the voltage capability and reduce the VOFF of the wider channel devices, thus obtaining a full compliance with the specifications. The characterization of the second batch will be also included in the final contribution.

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