Edge TCT study on irradiated AMS H35 CMOS devices for the ATLAS ITk

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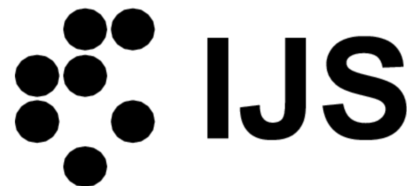
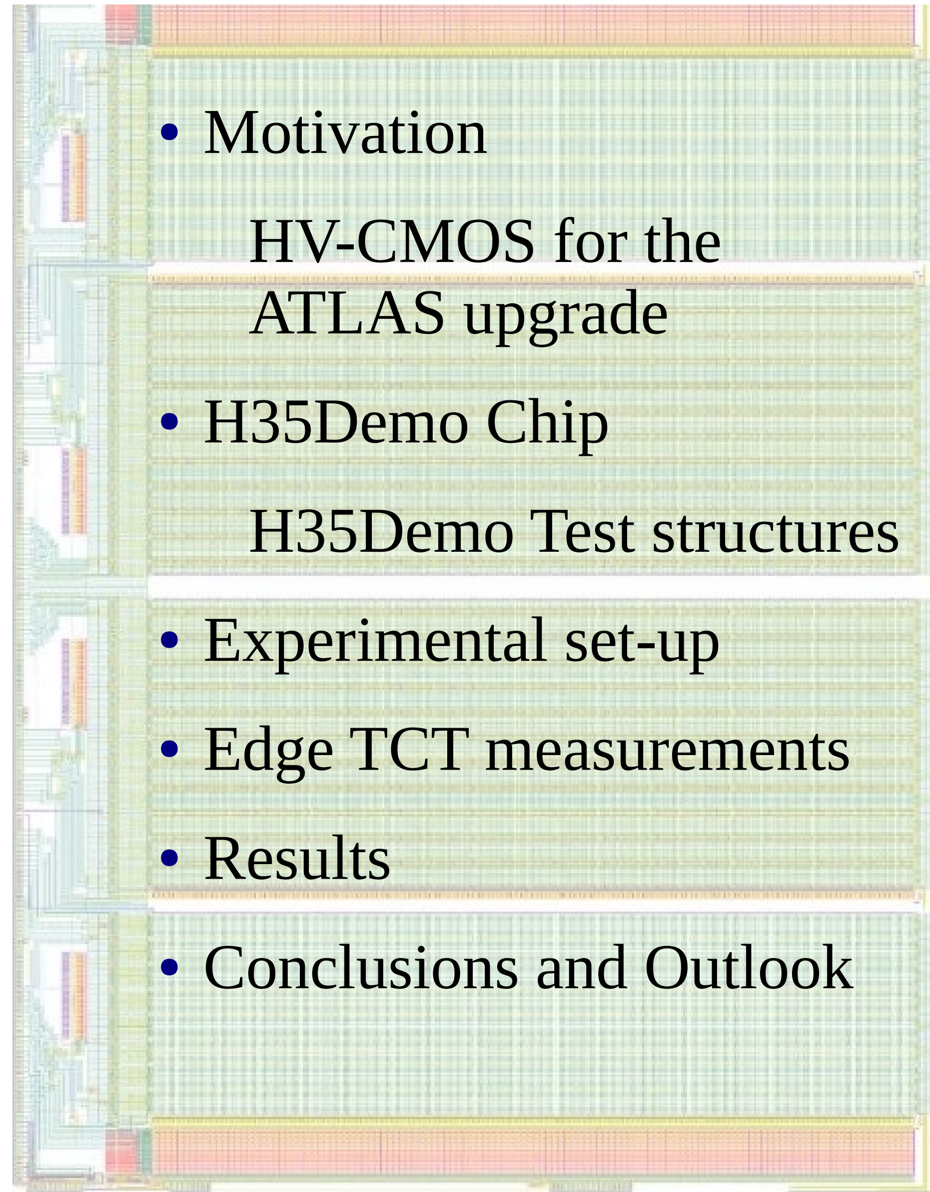


TWEPP 2016
26-30 September 2016

Outline



- Motivation
  - HV-CMOS for the ATLAS upgrade
- H35Demo Chip
  - H35Demo Test structures
- Experimental set-up
- Edge TCT measurements
- Results
- Conclusions and Outlook

Motivation

HV-CMOS for the ATLAS upgrade

LHC upgrade to High Luminosity LHC scheduled for beginning 2024

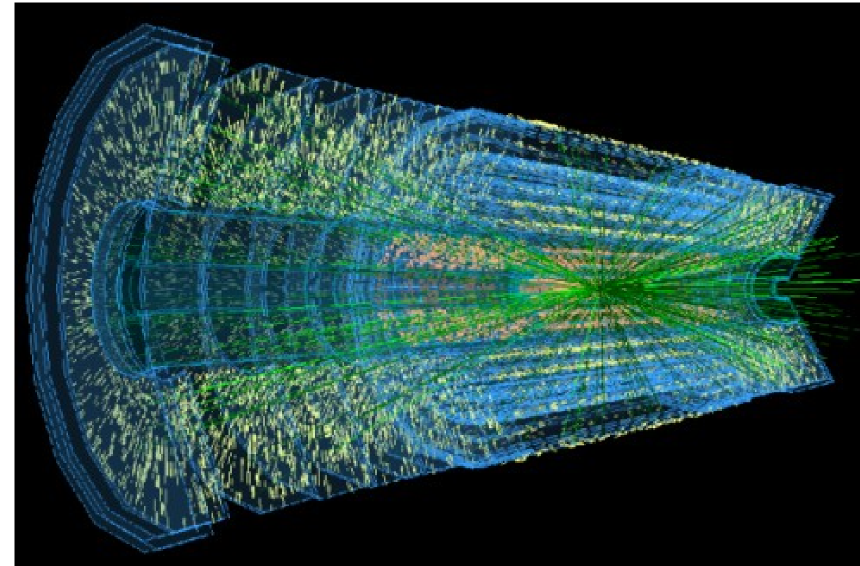
Plan to increase the luminosity by an order of magnitude up to 10^{35} $cm^{-2}s^{-1}$

Detector challenges:

Trigger pileup - particle multiplicity
pileup rejection- radiation hardness

ITK - tracker upgrade for HL-LHC

- 5 layers Pixels detector



Sketch of an event in ATLAS at HL-LHC

The **innermost pixel layer** will be required to stand up to a fluence of **$2{\cdot}10^{16}$ n_{eq}/cm^2**, the **outermost layer ~ 10^{15} n_{eq}/cm^2**

A total area of **~10 m^2 of pixel detectors** will be installed

HV-CMOS technology being investigated in ATLAS as a cost-effective option for the HL-LHC upgrade

ATLAS groups are investigating the performances of:

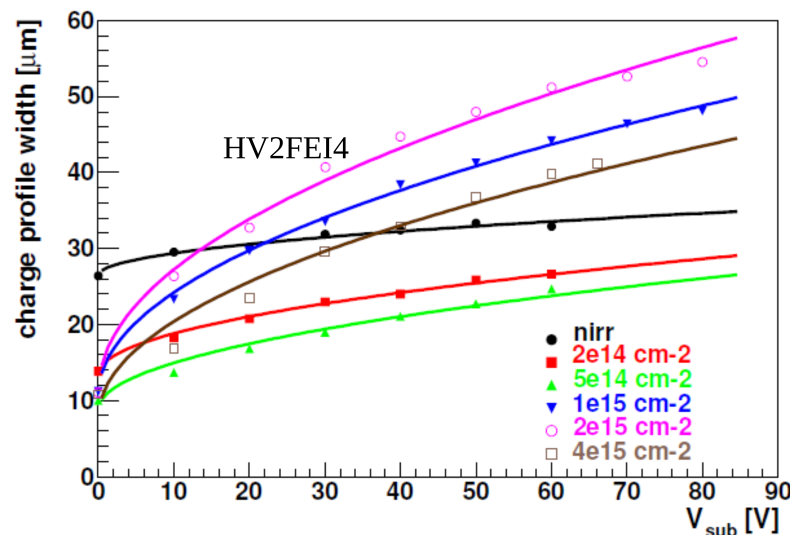
- Devices from different foundries
- Different approaches:
  passive – AC coupled – monolithic

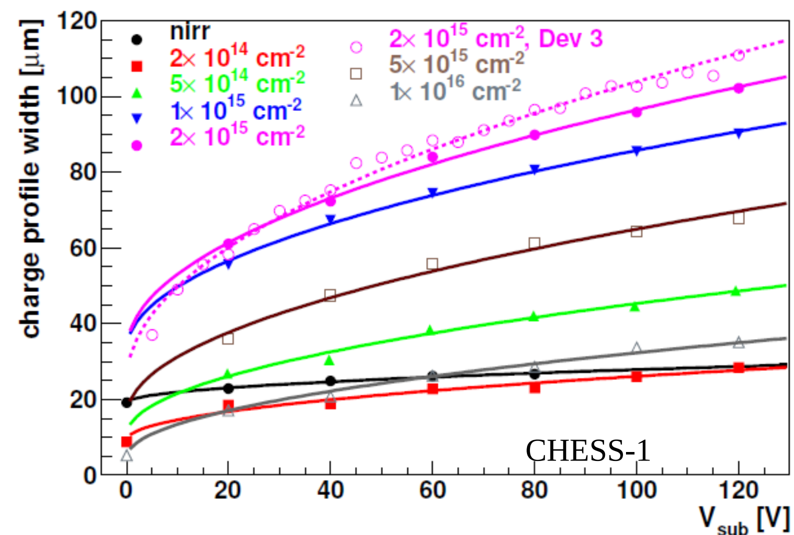
HV-CMOS for HEP

Several productions from different foundries have been made
Each with its production technology and wafer resistivity:

- AMS 350nm, ρ = 20Ω·cm (CHESS-1)
- AMS 180nm, ρ = 10Ω·cm (HV2FEI4)
- LFoundry 150nm, ρ = 2kΩ·cm
- X-FAB 180 nm, ρ = 100Ω·cm

Interesting results have been obtained but it is hard to compare devices from different foundries because of different technologies, substrate doping and well properties

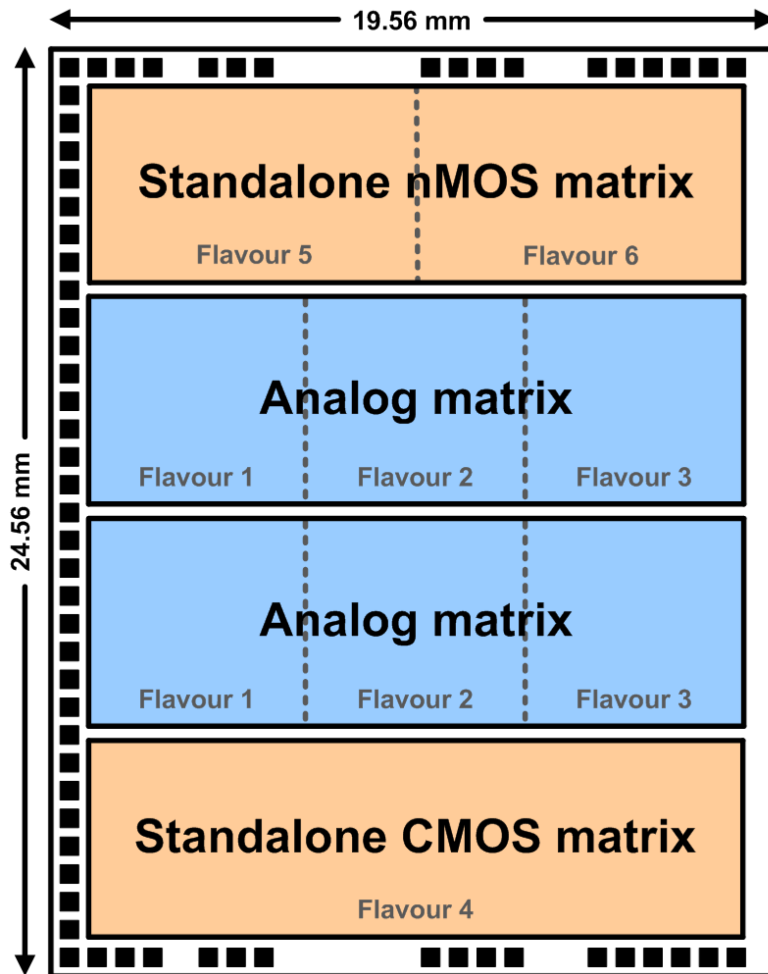




G Kramberger, 27th RD50 Workshop

H35Demo Chip

A large area demonstrator chip in the AMS .35μm HV-CMOS technology produced on wafers of different resistivity 20 Ωcm (standard), 80 Ωcm, 200 Ωcm, 1 kΩcm



Developed to investigate the feasibility of HV-CMOS devices in HL-LHC

Designed by:

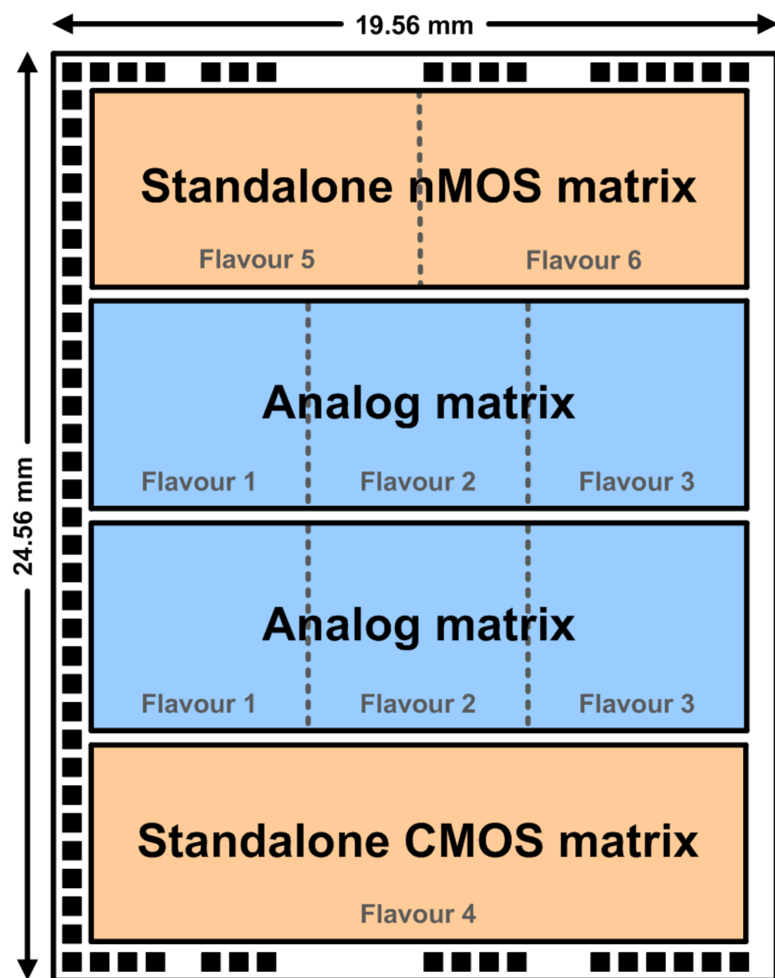
Ivan Peric – KIT
Eva Vilella – University of Liverpool
Raimon Casanova – IFAE

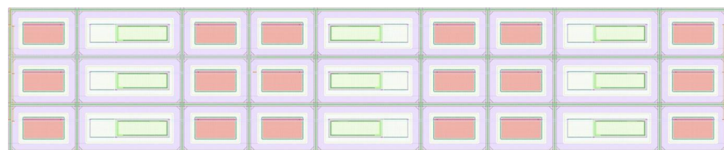
With the purpose of testing:

- Large area chips
- Different in-pixel circuitry options
- Hybrid and standalone readout

Collaboration between KIT, IFAE, University of Liverpool and University of Geneva

H35Demo Chip





Six different pixel matrix flavors:

- Standalone nMOS matrix
  - Digital pixels with in pixel nMOS comparator
  - Two flavors: w/ Time Walk compensation and w/o TW compensation
- Analog matrix (2 arrays)
  - Different flavors in terms of gain and speed
  - To be capacitative coupled to FE-I4 readout chips
- Standalone CMOS matrix
  - Analog pixels with off pixel CMOS comparator

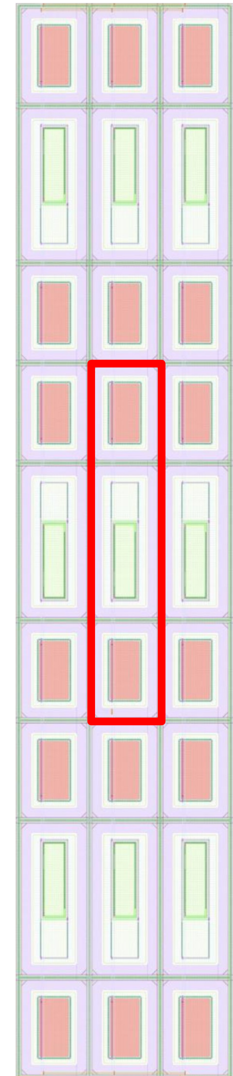
Test structures:

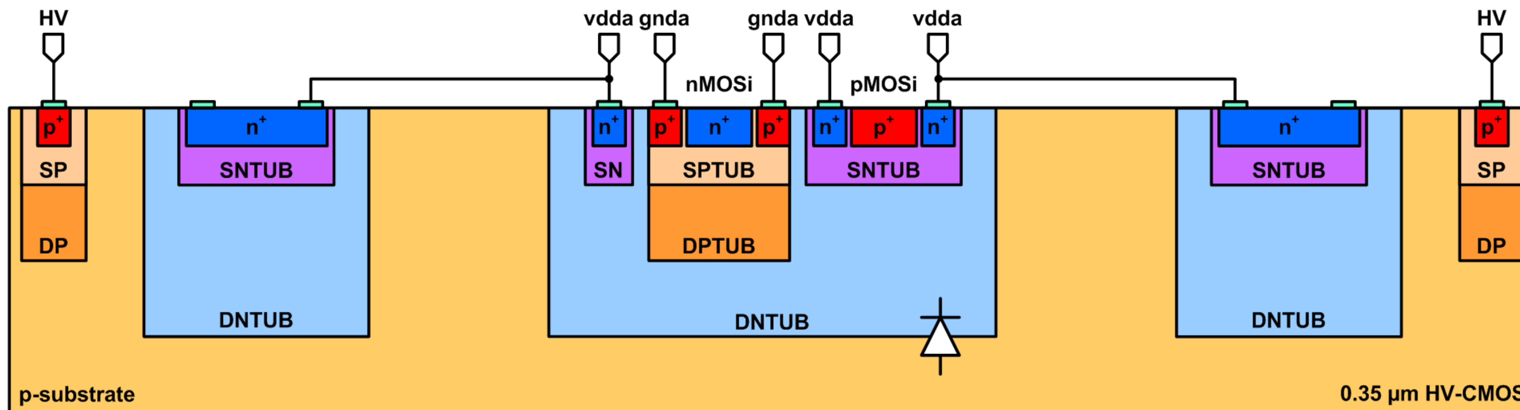
- Central pixel w/ 8 neighbor + output buffer
- Central pixel w/ 8 neighbor
- Structure for capacitance measurement

H35Demo test structure

The tested structure is a matrix of 3x3 pixels of 50·250 μm² each

- 3 deep N wells in each pixel
  - central 50·110 μm²
  - external 50·70 μm²
- no electronics inside the pixels
- deep P well inside the deep N well of the central N well
- deep N wells covered by a layer of polysilicon in the external N wells
- central pixel (marked in red in the figure) is read out individually
- signals of the 8 external pixels are shorted together



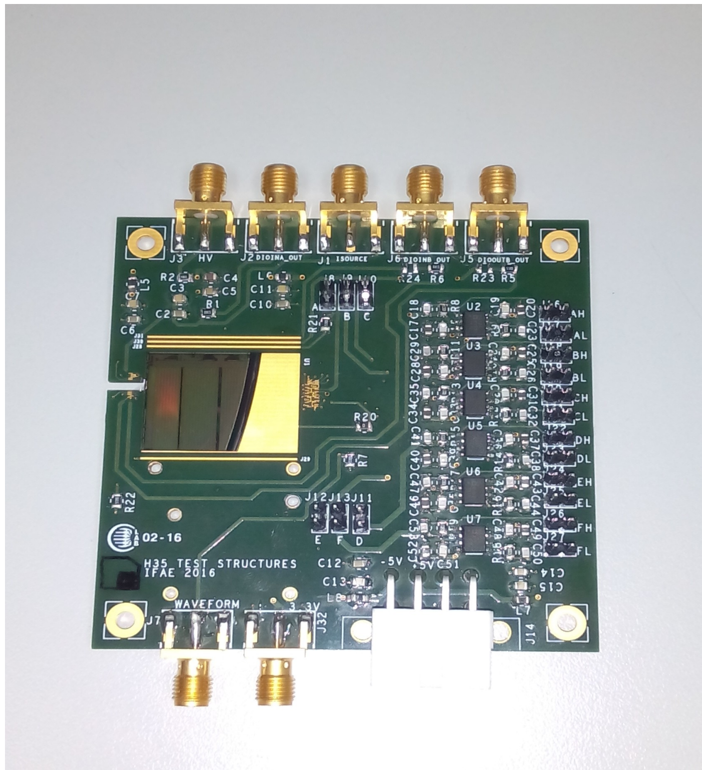


Pixel cross section and sketch of the tested structure*

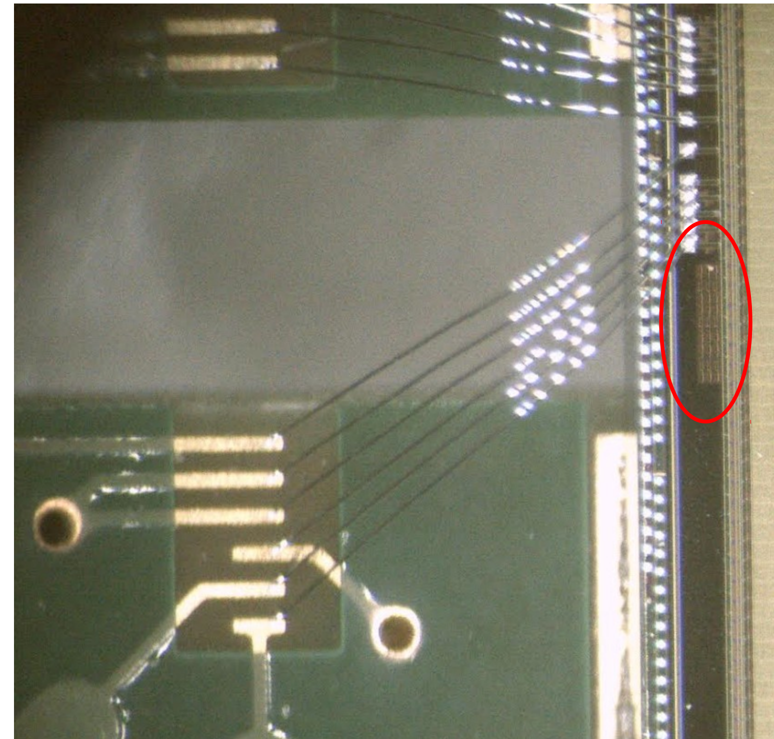
**from Eva Vilella*

H35Demo PCB

The tested devices are from wafers with nominal resistivity of 80 Ω·cm, 200 Ω·cm and 1kΩ·cm



H35Demo chip on the PCB
Designed by C. Puigdengoles



Detail of the test structures

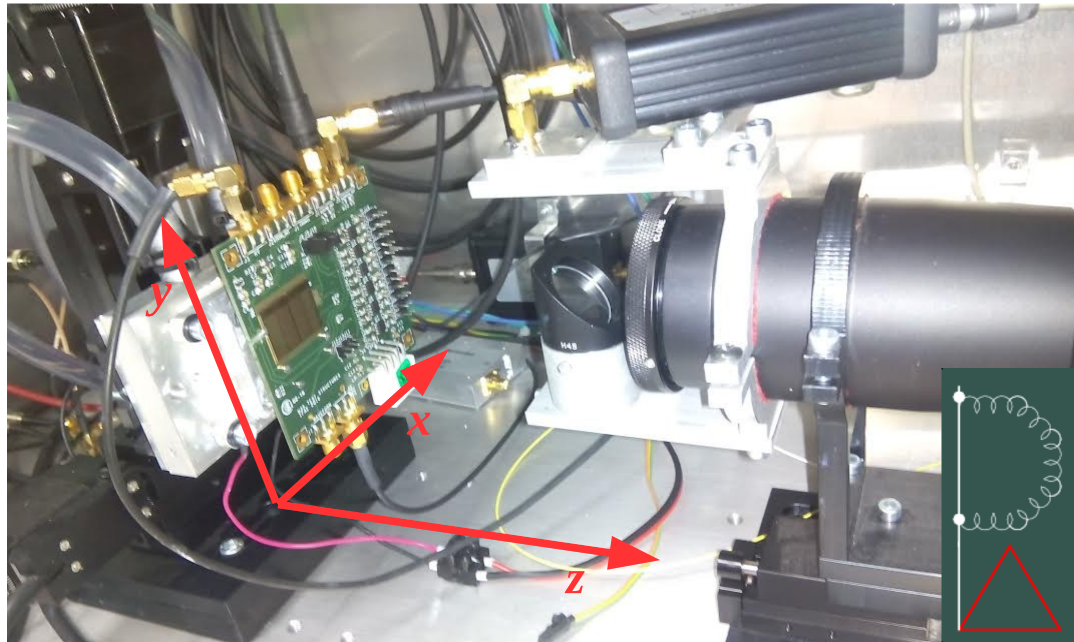
The H35Demo PCB can be used to test both the 3x3 test structures and the capacitance measurement test structure

Transient Current Technique Set-up

Scanning TCT from Particulars

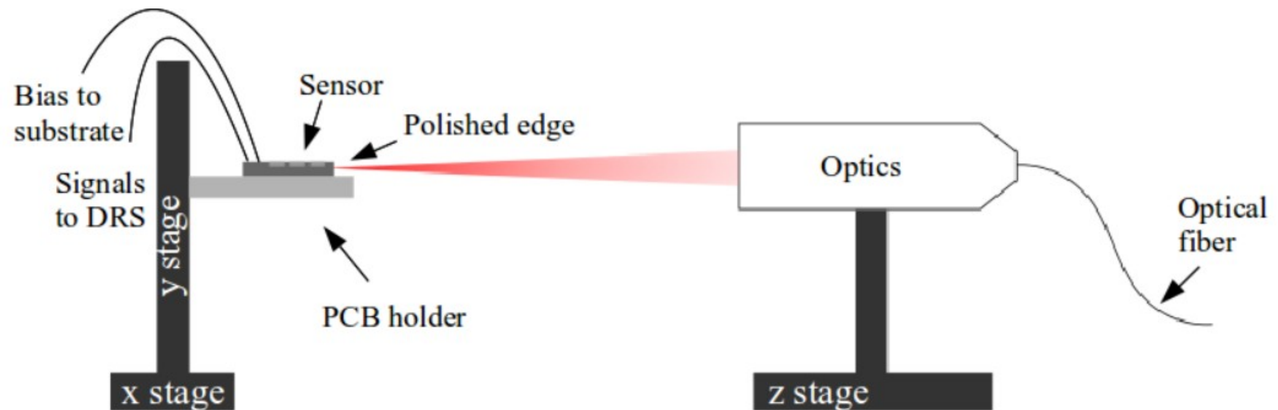
Laser properties
- Red or IR laser (640 nm and 1064 nm)
  - all results shown have been obtained with the IR laser beam
- Beam spot ~5-10 μm FWHM
- Laser pulses of ~500 ps

Readout through DRS4 evaluation board
- 700 MHz bandwidth
- 5 GSPS
- 200 ns sampling depth
- 4 channels
  - 1 - trigger
  - 1 - beam monitor
  - 2 - readout channels

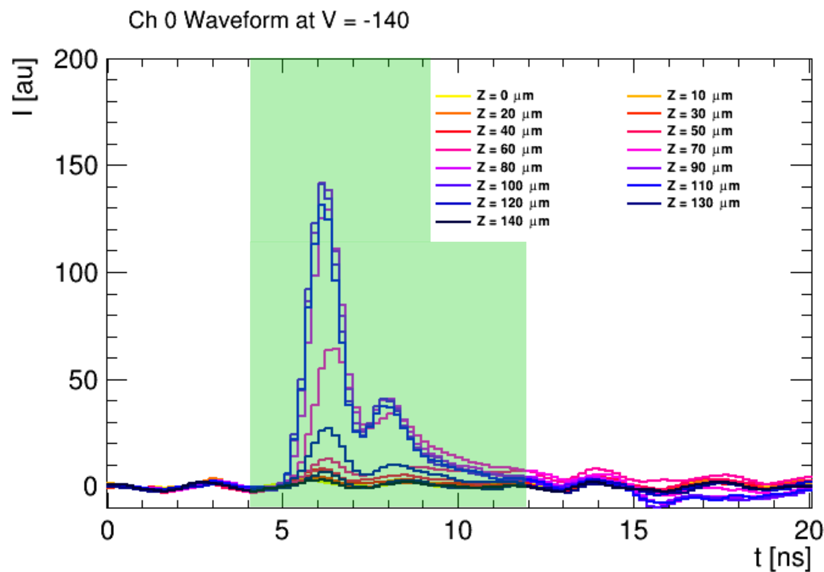


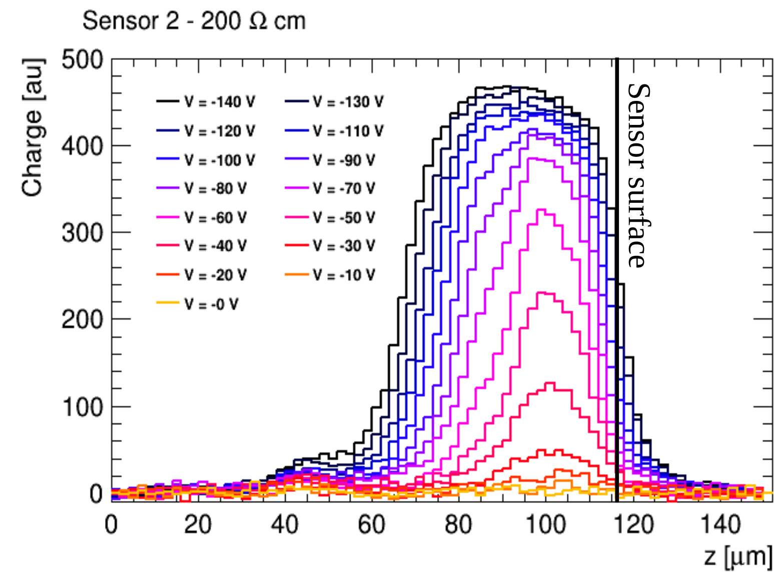
Edge TCT

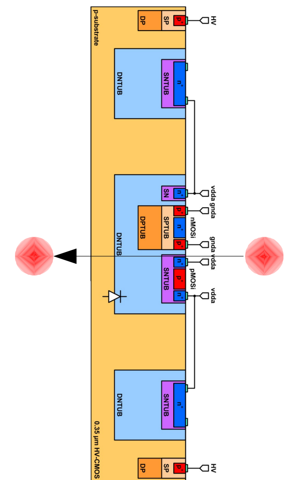
In edge TCT the laser is facing the edge of the chip generating e-h pairs at different depths of the test structure



Sketch of the edge TCT set-up



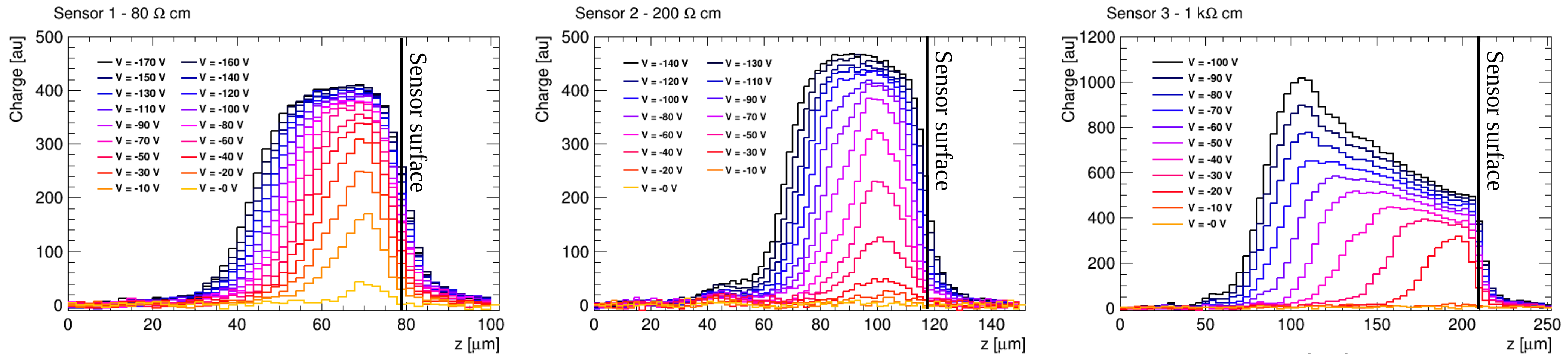


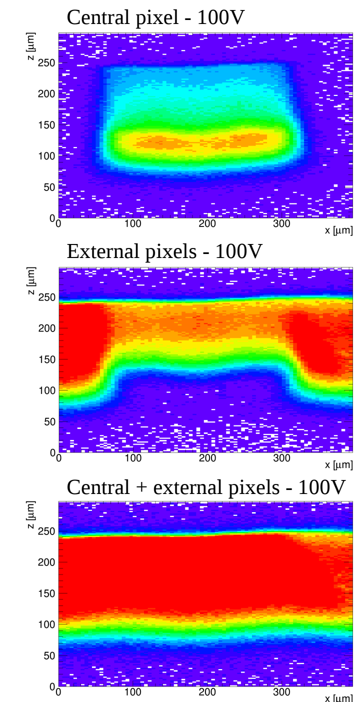


A waveform is stored for each scan position and the collected charge is evaluated by its integral

Charge collection profile

Charge collection profiles of the three DUTs

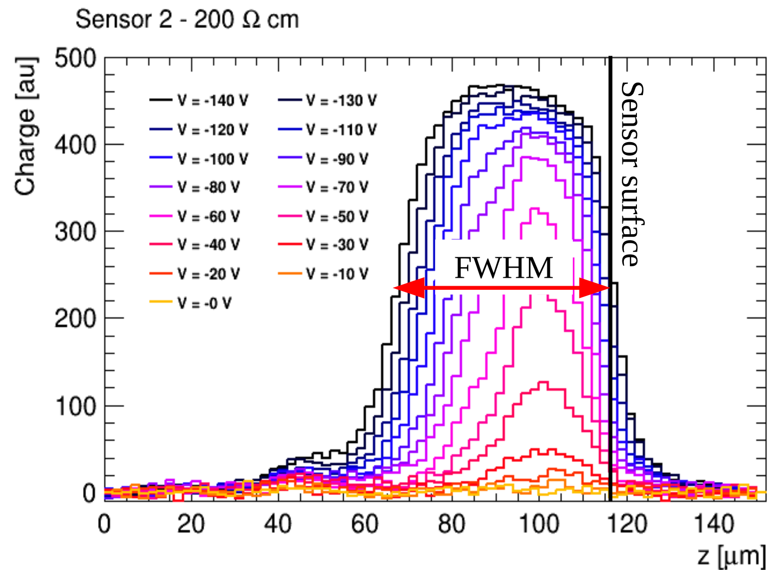


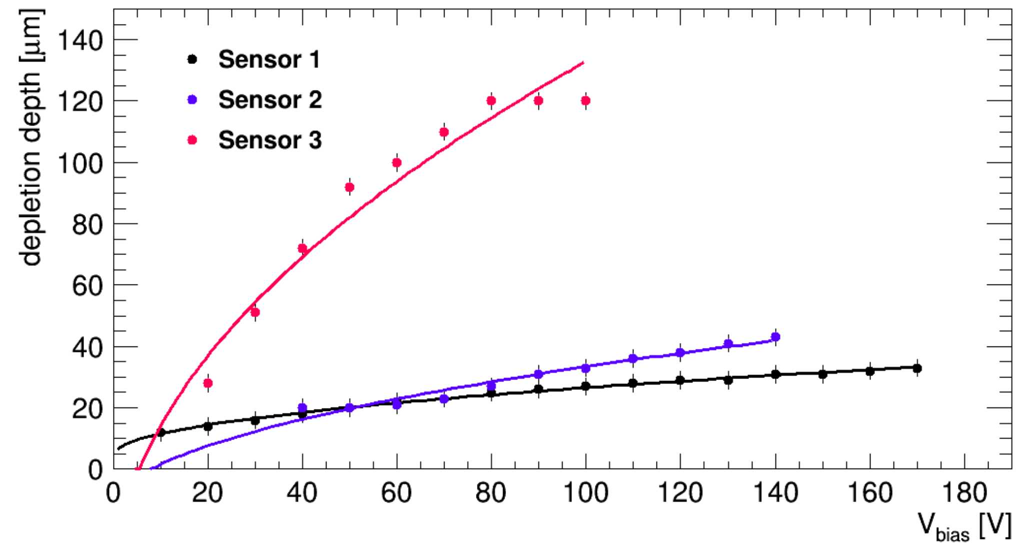


The depletion depth grows with voltage allowing to collect charges generated more deeply into the sensors bulk

In Sensor 3 when the depletion depth reach ~100 µm the central pixel collects the charge generated underneath the other pixels of the matrix

Depletion depth





The depletion depth is taken as the FWHM of the charge collection profile
The central value of an S-curve fit on each side of the curve gives the extremes of the FWHM

The resistivity can be verified fitting *d(V)* with

$$d(V) = d_0 + \alpha\sqrt{\rho V} \quad \text{with} \quad \alpha = \sqrt{2\varepsilon\varepsilon_0\mu}$$

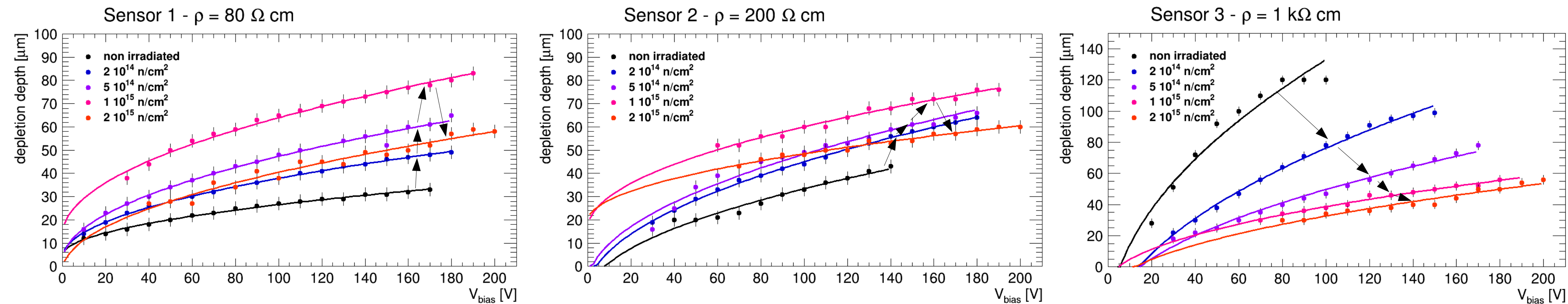
	Nominal ρ	Measured ρ
Sensor 1	80 Ωcm	50 ± 11 Ωcm
Sensor 2	200 Ωcm	230 ± 49 Ωcm
Sensor 3	1k Ωcm	4500 ± 300 Ωcm

Depletion depth - irradiated

Irradiation with neutrons at the JSI TRIGA reactor in Ljubljana

- $2 \cdot 10^{14}$ 1MeV n_{eq}/cm^2
- $5 \cdot 10^{14}$ 1MeV n_{eq}/cm^2
- $1 \cdot 10^{15}$ 1MeV n_{eq}/cm^2
- $2 \cdot 10^{15}$ 1MeV n_{eq}/cm^2

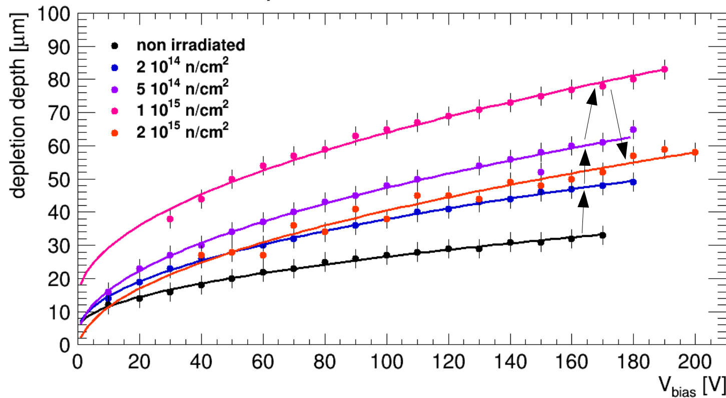
Edge TCT measurements repeated after each irradiation step

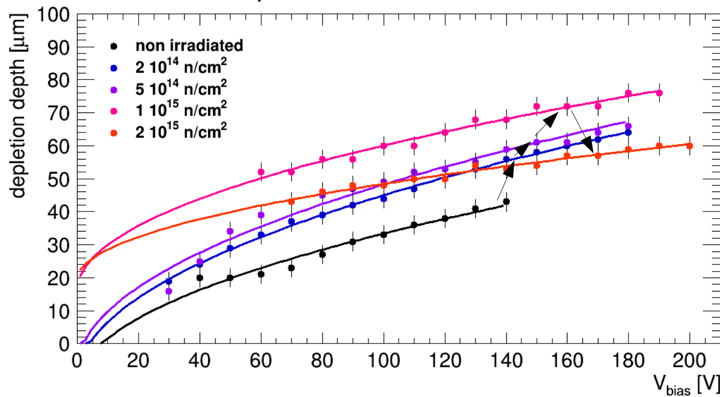


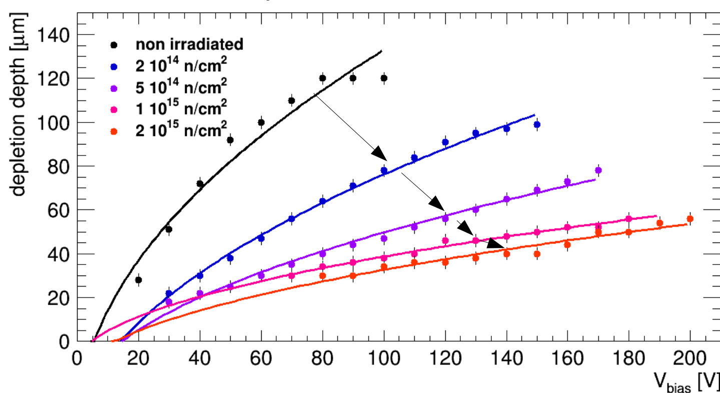
The samples with lower substrate resistivies show an initial increase of the depletion depth with irradiation that decrees at higher fluences

The depletion depth of the 1kΩcm sample reduces with irradiation already at the first step

Depletion depth - irradiated







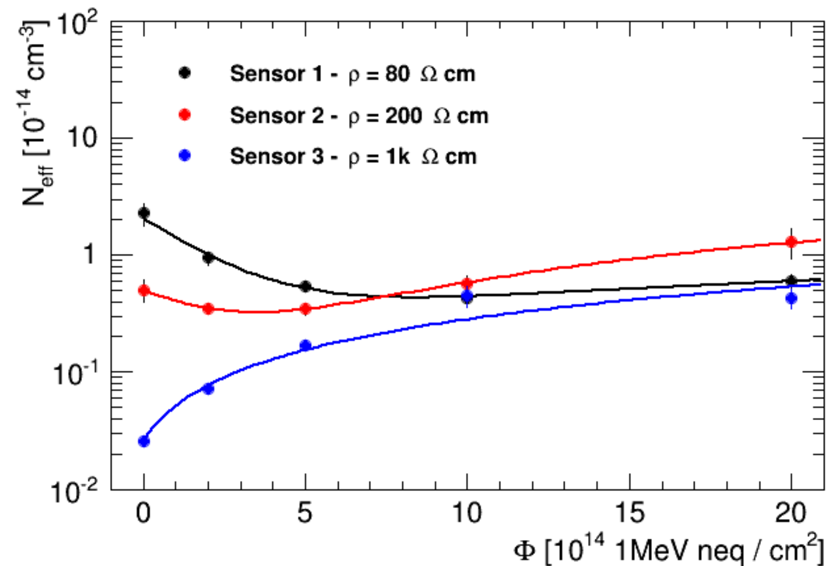
Writing the depletion depth as a function of N_{eff}

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

A change of the slope means a change in N_{eff}

$$N_{eff} = \underline{N_{eff0}} - \underline{N_c \cdot (1 - exp(-c \cdot \Phi_{eq}))} + \underline{g_c \cdot \Phi_{eq}}$$

Initial doping — Acceptor removal — Radiation induced acceptor introduction

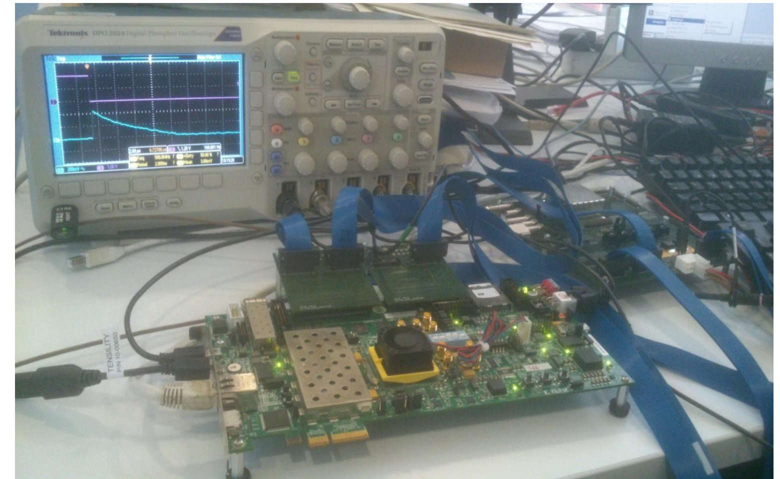


After irradiation to ~10^{15} 1MeV n_{eq}/cm^2 Neff tends to roughly the same value for all resistivities

Matrices readout

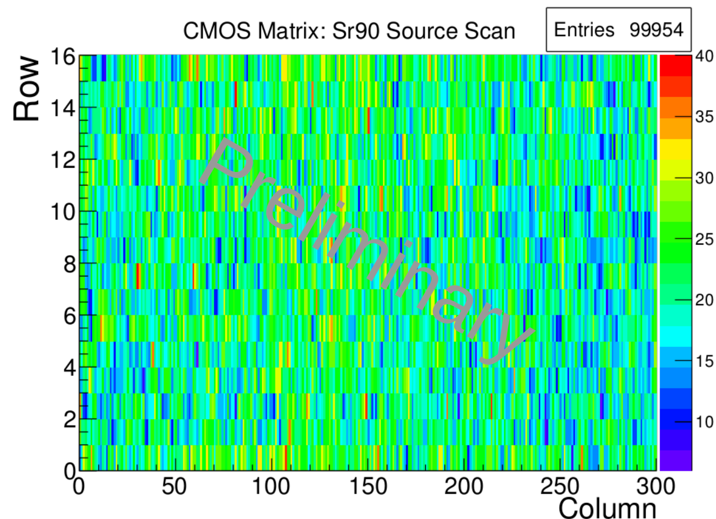
DAQ development at IFAE:

- Readout system for the monolithic CMOS and nMOS matrices based on the Xilinx ZC706
- C++ DAQ software



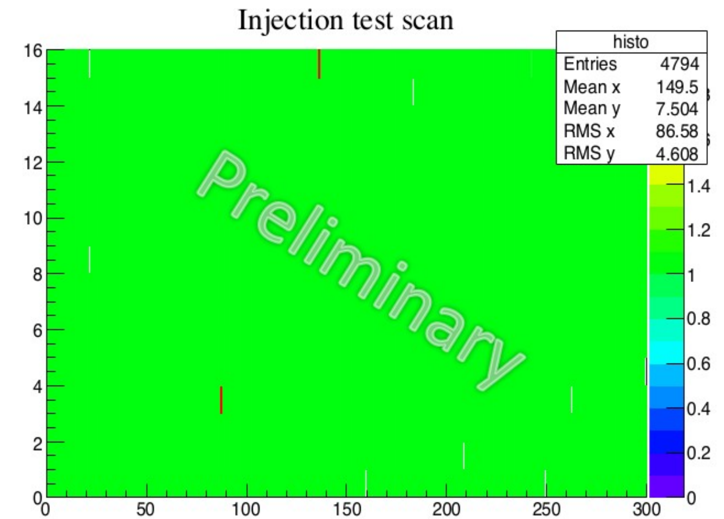
Test of nMOS and CMOS standalone matrices with 90Sr radioactive source

- Roughly tuned chip (only global DACs)
- Tuning not yet implemented



Preliminary results for injection test scan with external pulse generator

- Almost all pixels responding



Analog matrices under investigation with capacitive coupling to FE-I4 chips

Conclusions

- TCT study of H35Demo test structure before and after irradiation is presented
  - Acceptor removal effect observed in sensors of 80 Ωcm and 200 Ωcm
  - $N_{eff} \sim 1 \cdot 10^{-14} cm^{-3}$ after irradiation to 10^{15} 1MeV n_{eq}/cm^2
- Collection layers of at least 30 µm are achievable on chips with any of the tested substrate resistivities
- Communication with standalone matrix successful

Outlook

- Continue the irradiation campaign up to 10^{16} 1MeV n_{eq}/cm^2
- Test the effect of radiation on the analog and digital pixel matrices
- Analog matrices with FE-I4 readout chip will be tested with beam soon

Thanks