



Application of flash-based field-programmable gate arrays in high energy physics

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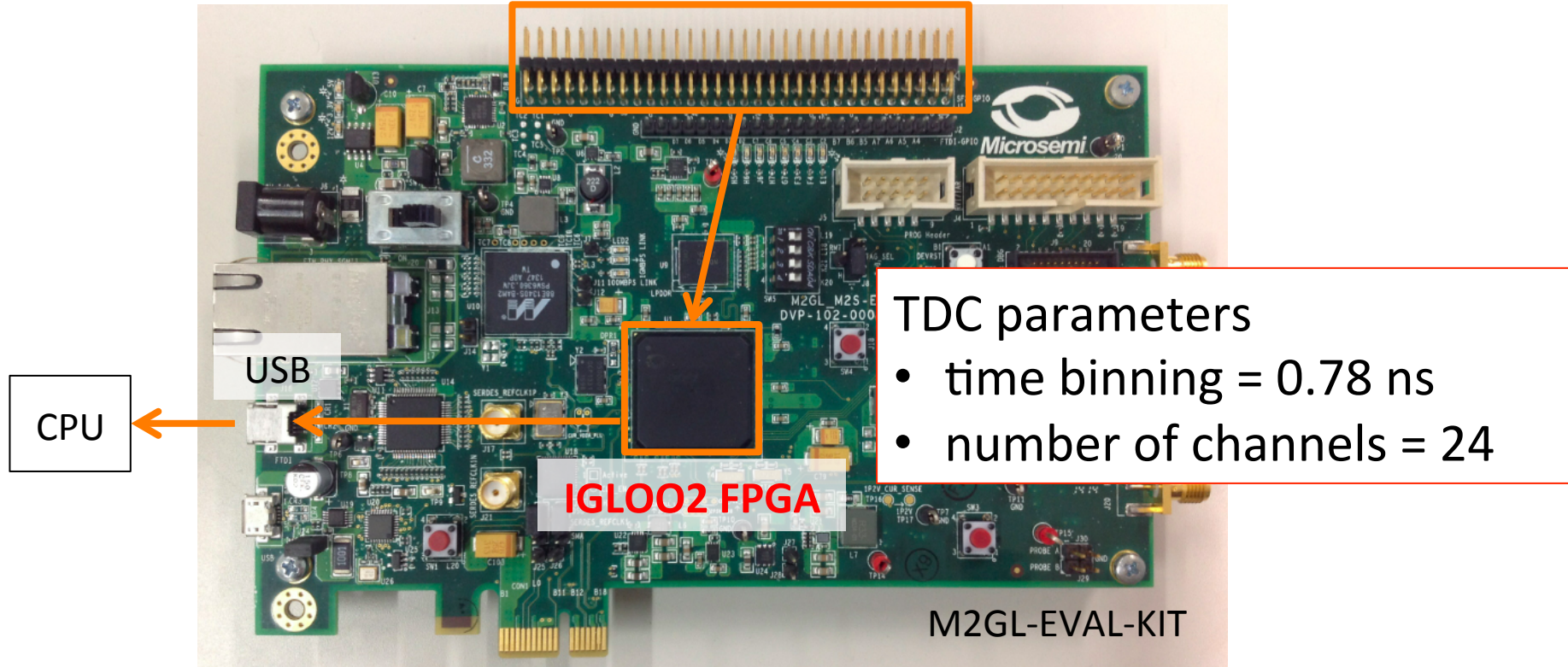
Introduction

- Field-programmable gate arrays (FPGAs) are widely used in the experiments of high energy physics.
- IGLOO2, flash-based FPGA provided by Microsemi, has relatively high radiation tolerance against single event effects with respect to SRAM-based FPGAs.
 - http://www.microsemi.com/document-portal/doc_view/135249-tr0020-smartfusion2-and-igloo2-neutron-single-event-effects-see-test-report
- In this report, to consider about the potential applications of IGLOO2, the following two items are investigated.
 - Performance of TDC
 - Tolerance against Total Ionization Dose (TID)

Demonstration of TDC implemented in IGLOO2 FPGA

Setup of the TDC demonstration

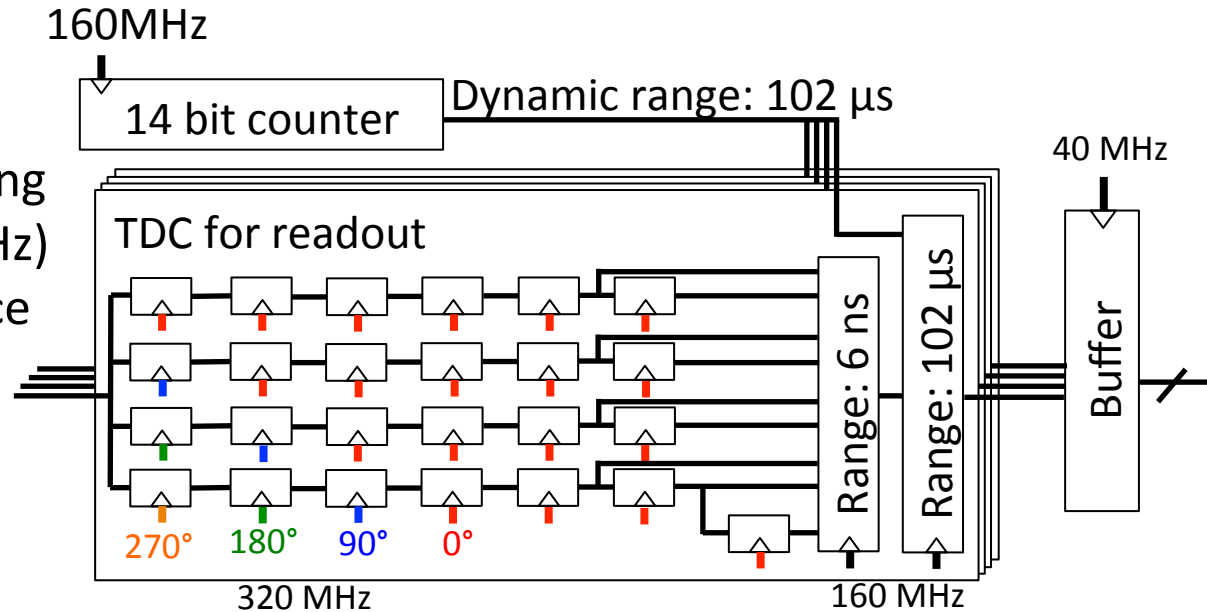
Signal input + 40 MHz reference clock input



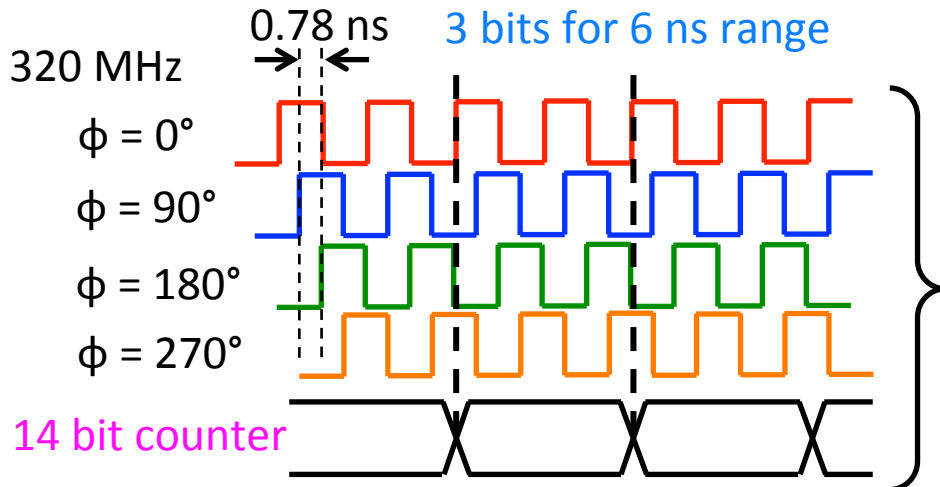
- The TDC is implemented in IGLOO2 FPGA on the evaluation kit (M2GL-EVAL-KIT).
- Performance is evaluated for all of 24 channels.
- Readout with the UART protocol.

Block diagram of the TDC

- Multi-sampling scheme using quad-phase clocks (320 MHz) synchronised with reference clock (40 MHz).
- Maximum frequency supported for the tested FPGA is 400 MHz.



Y. Sano et al 2016 JINST 11 C03053

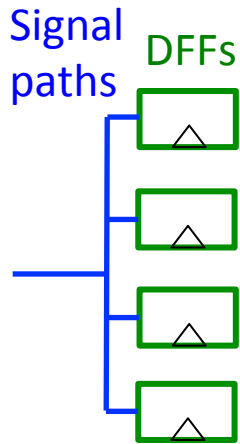


Hit address: 17 bits

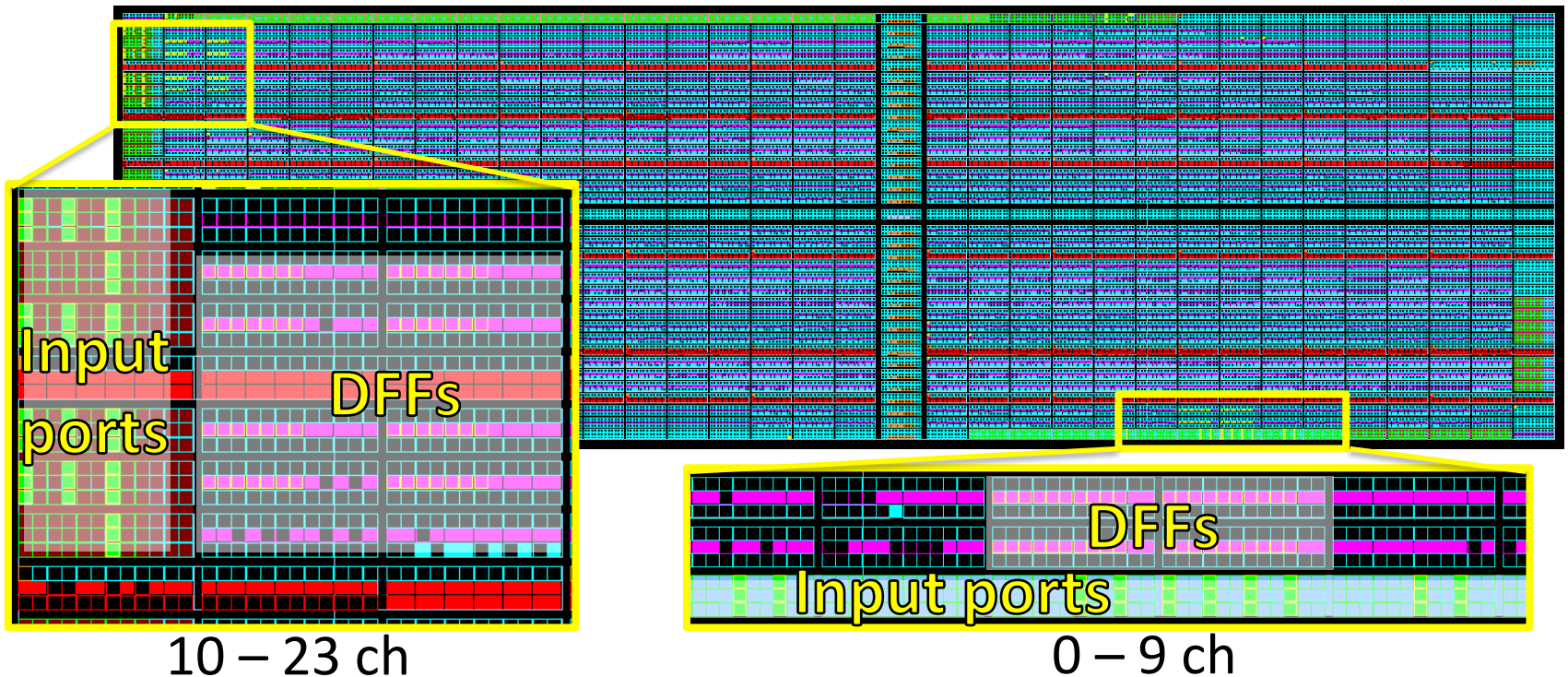
XXXXXXXXXXXXXXXXXXXXXX

Coarse bits from 14 bit counter The lowest significant bits

Constraint on the places of DFFs



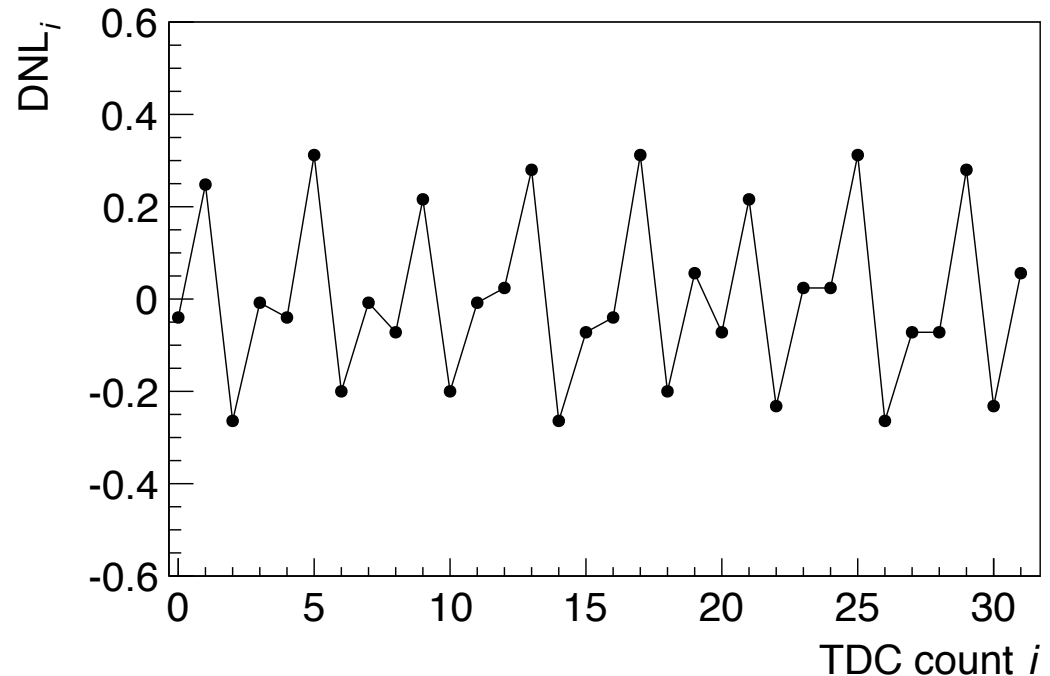
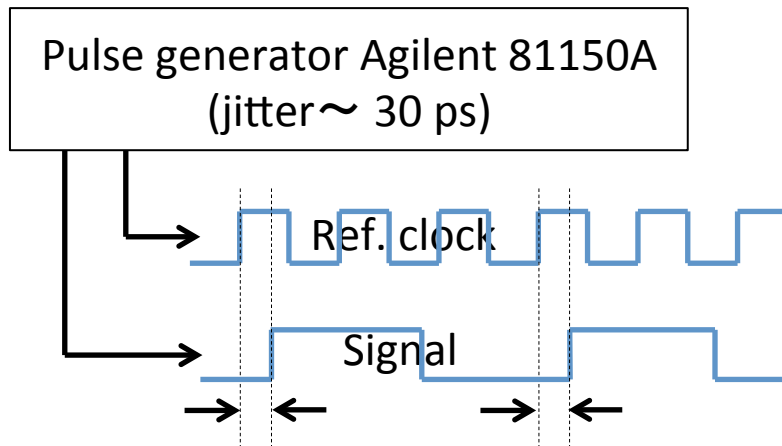
- To suppress the signal path difference, the DFFs are placed near the input ports.
- Signal path difference is within ~ 200 ps.



Differential non-linearity

$$\text{DNL}_i [\text{LSB}] = \frac{T_i - T_{\text{LSB}}}{T_{\text{LSB}}} \quad \left\{ \begin{array}{l} T_{\text{LSB}}: \text{ideal time binning} \\ T_i: \text{measured time binning} \end{array} \right.$$

The time difference between the reference clock and the signal is scanned.

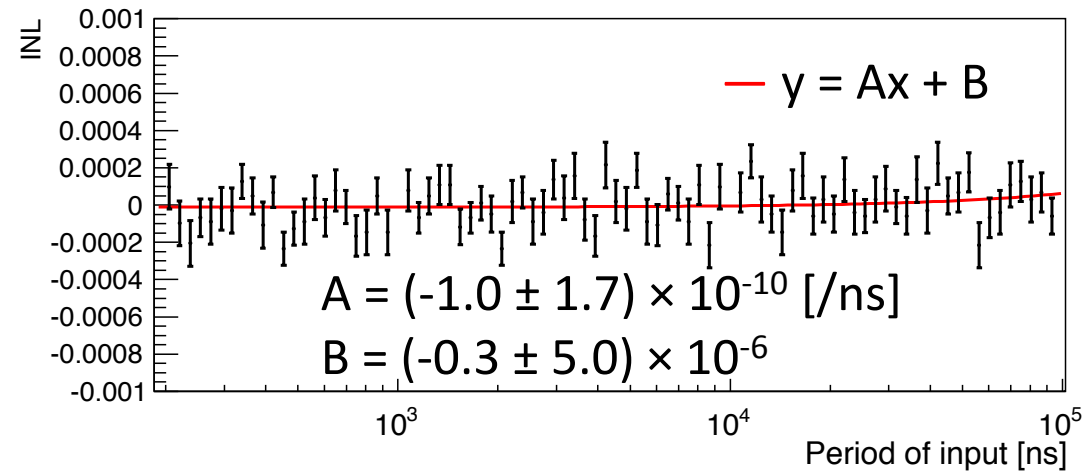
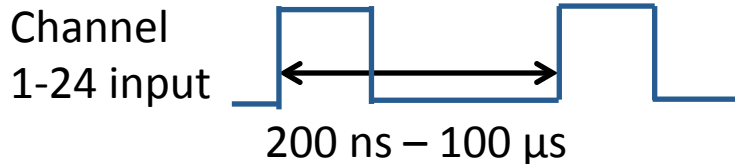


- Measured DNL_i is ≤ 0.4 LSB for all the measured bins of the 24 channels.
- The measured DNL is consistent with the signal path difference derived from the Microsemi Libero design tool (~ 200 ps at maximum).

Integral non-linearity

$$\text{INL}[\text{LSB}] = \frac{\langle T_{\text{measured}} \rangle - T_{\text{ideal}}}{T_{\text{LSB}}} \quad \left[\begin{array}{l} T_{\text{ideal}}: \text{ideal time} \\ \langle T_{\text{measured}} \rangle: \text{mean of measured time} \end{array} \right.$$

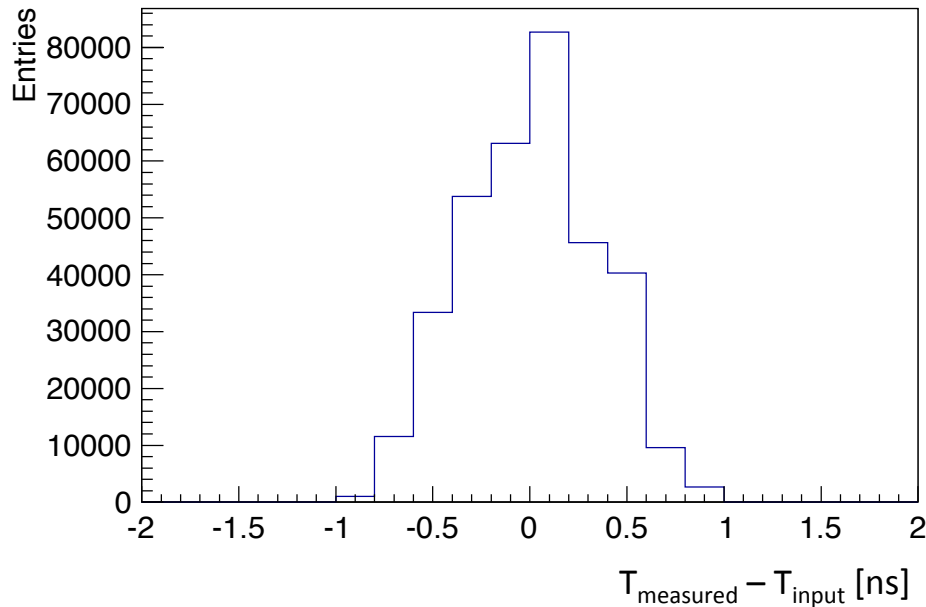
Time difference between the leading edges is measured.



- Measured INL is consistent with zero in the full dynamic range (102 us).
- Similar result is obtained for all of the 24 channels.

Time resolution

Distribution of $T_{\text{measured}} - T_{\text{input}}$ for channel 1



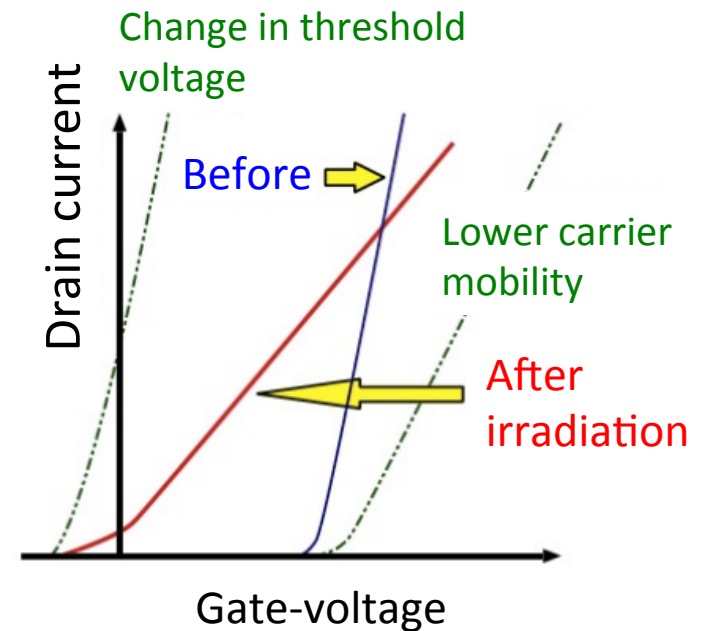
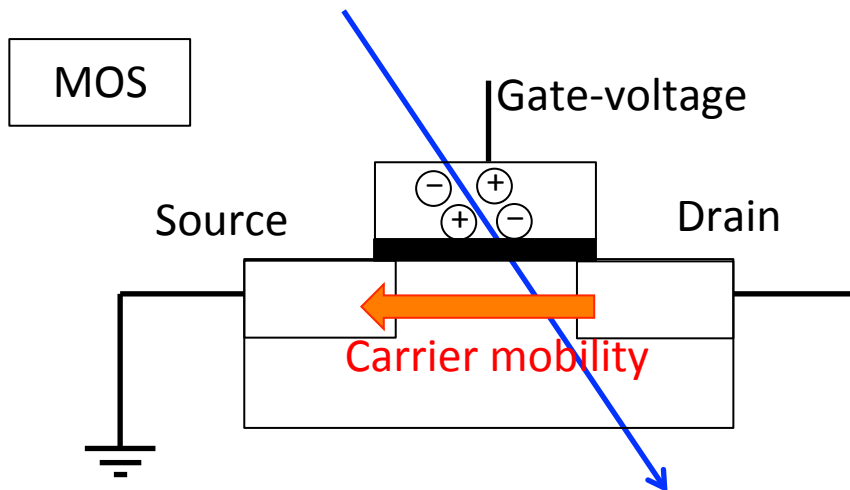
- No overflow, no underflow
- RMS = 0.35 ns
- RMS/ $\sqrt{2}$ = 0.25 ns

- Time resolution for the measurement of single leading edge is evaluated to be 0.25 ns.

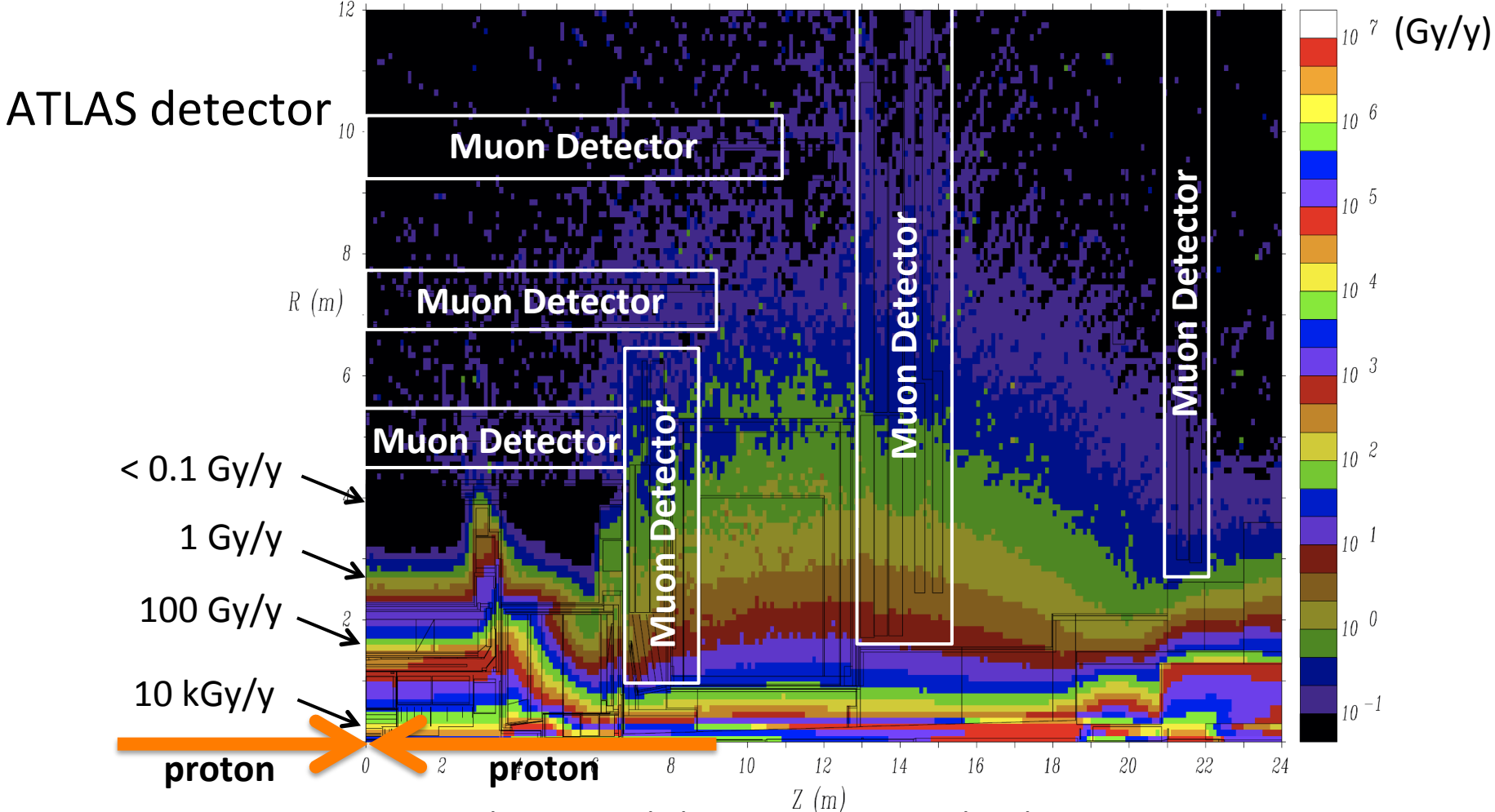
TID test of the IGLOO2 FPGA

TID effects on FPGAs

- Change in the threshold voltage
 - Leak current due to the charges in insulator layer
- Smaller saturation current
 - Lower carrier mobility due to the charges in insulator layer



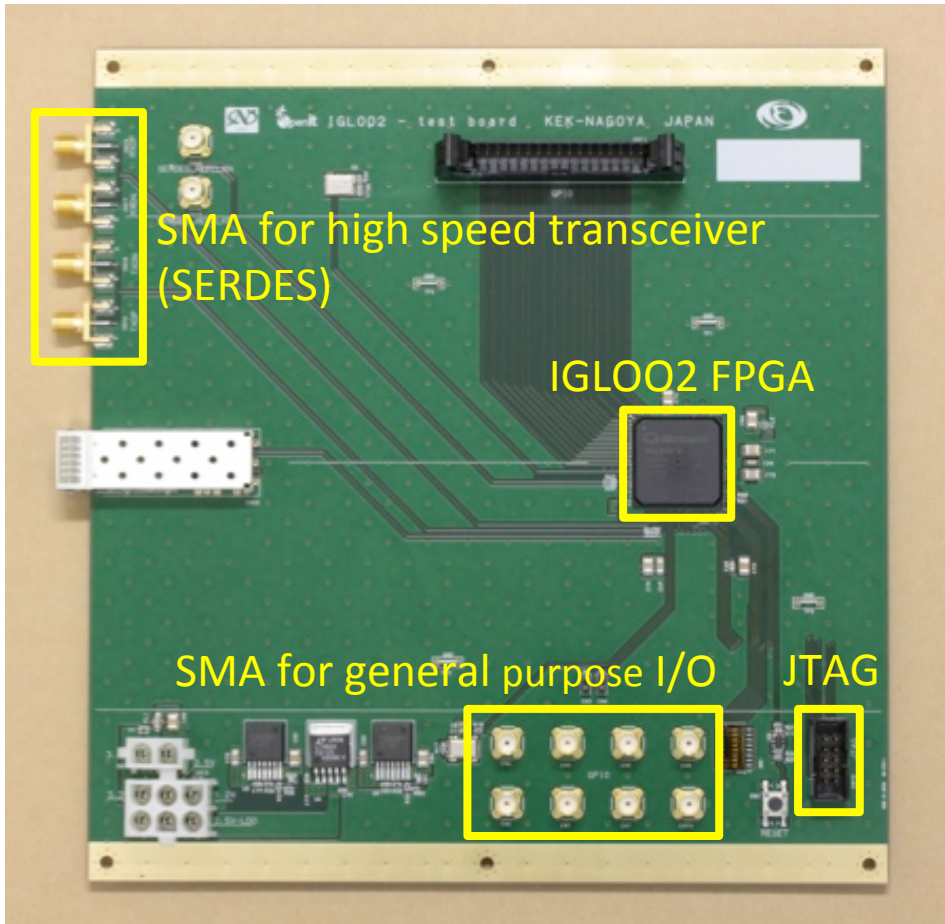
Example of TID level



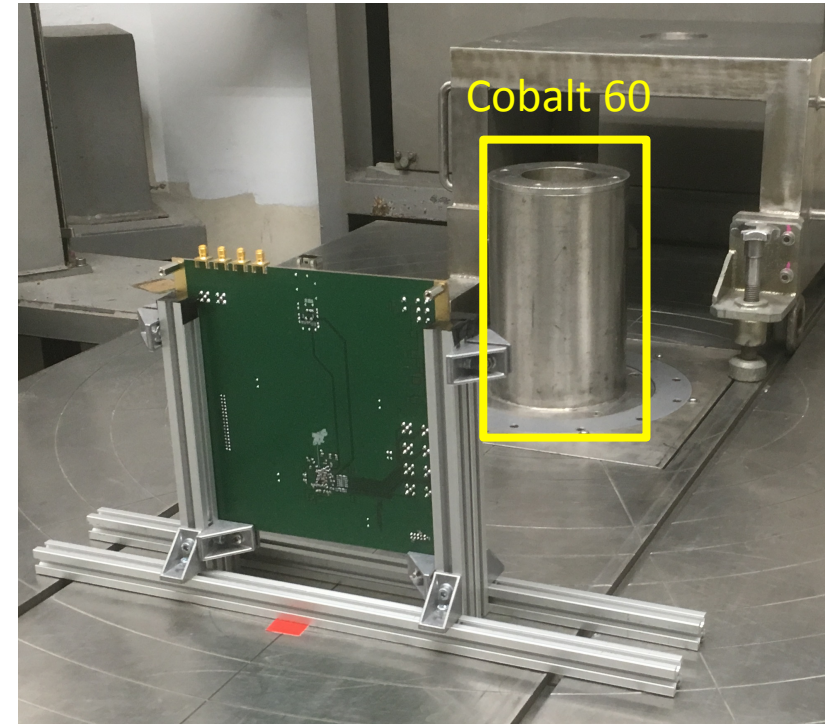
ATLAS Radiation Hard Electronics 3.1.2 Final Radiation Maps
<http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm>

Muon detector in barrel : $O(0.1)$ Gy/y
 Muon detector in endcap : $O(10)$ Gy/y

Irradiation test board



Test setup



- Irradiated at Cobalt 60 irradiation facility at Nagoya University
- 8 boards irradiated.
- Irradiation rate: $\sim 0.1 - 1 \text{ Gy / min}$

Items of TID test on the IGLOO2 FPGA

– Configuration memory

- Extraction of FPGA's ID
- Firmware download
- Verification of the downloaded firmware

– Ring oscillator (array of 501 NAND circuit)

- Period and power consumption

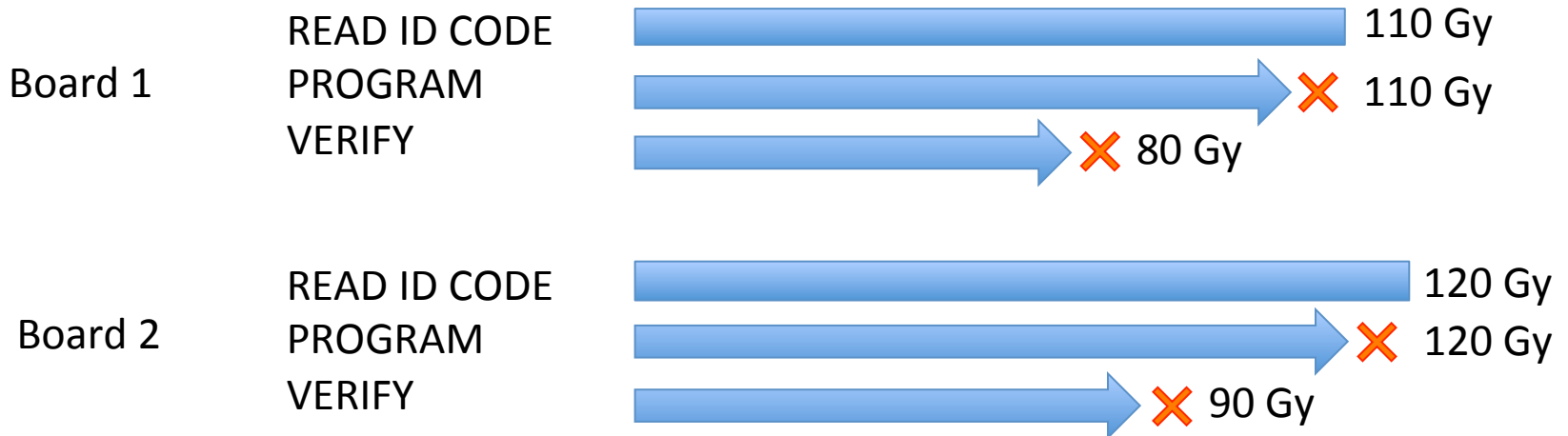
– High speed transceiver (SERDES)

- Bit error rate

Results for configuration memory

- Irradiation with step of 10 Gy
- Execute the following commands of Microsemi Libero design tool
 - READ ID CODE : Extraction of FPGA's ID
 - PROGRAM : Firmware download
 - VERIFY : Verification of the downloaded firmware

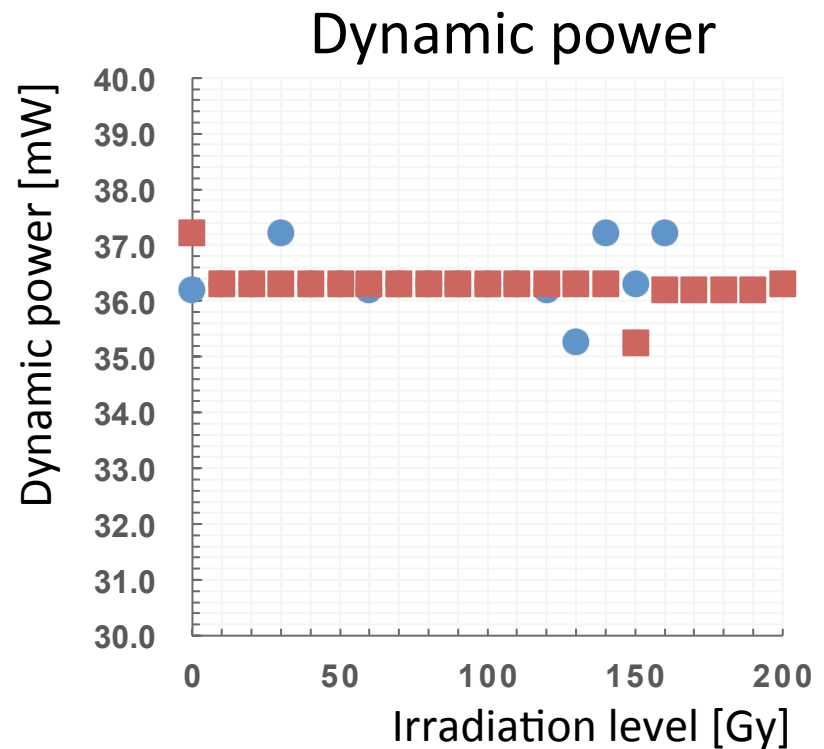
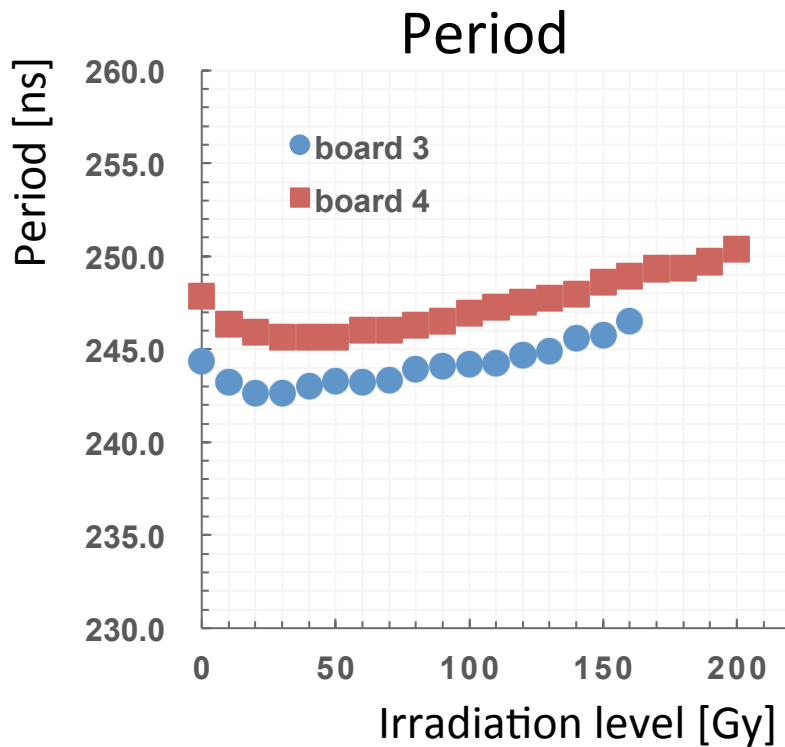
• Results



- 80 – 90 Gy : “VERIFY Error” occurred
- 110 – 120 Gy : “PROGRAM Error” occurred

Results for ring oscillator

- Measure the period and the power consumption of the ring oscillator beyond the limit of firmware download.
- Firmware download only performed before the irradiation



- No oscillation observed after the irradiation of ~ 200 Gy.
- A slight change on the ring oscillator cycle observed.

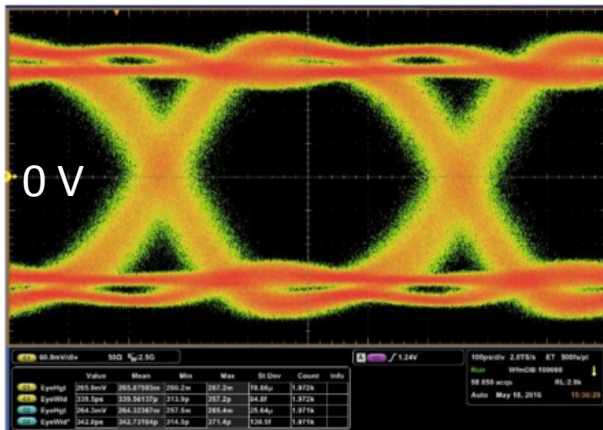
Results for SERDES

- Bit error checked with the loop back of pseudo random data.
- Firmware download only performed before the irradiation.

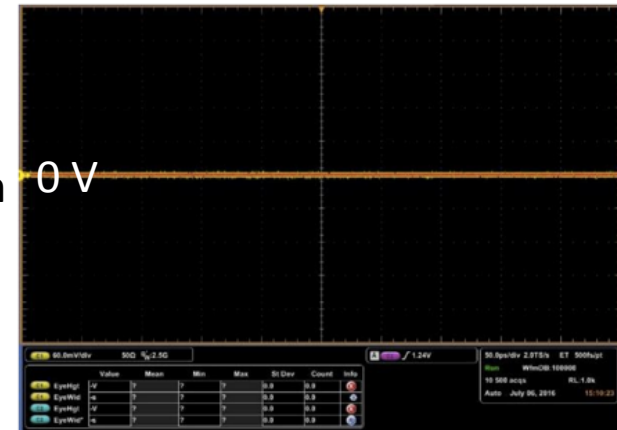
Total Dose	2 Gbps Bit error rate [/s]	4 Gbps Bit error rate [/s]
0 Gy	$< 8 \times 10^{-13}$	$< 4 \times 10^{-13}$
100Gy	$< 8 \times 10^{-13}$	$< 4 \times 10^{-13}$
200 Gy	Not functional	Not functional

- SERDES not functional after the irradiation of 200 Gy.
 - The eye diagram of the output from SMA for SERDES

Before
irradiation



After irradiation
of 200 Gy

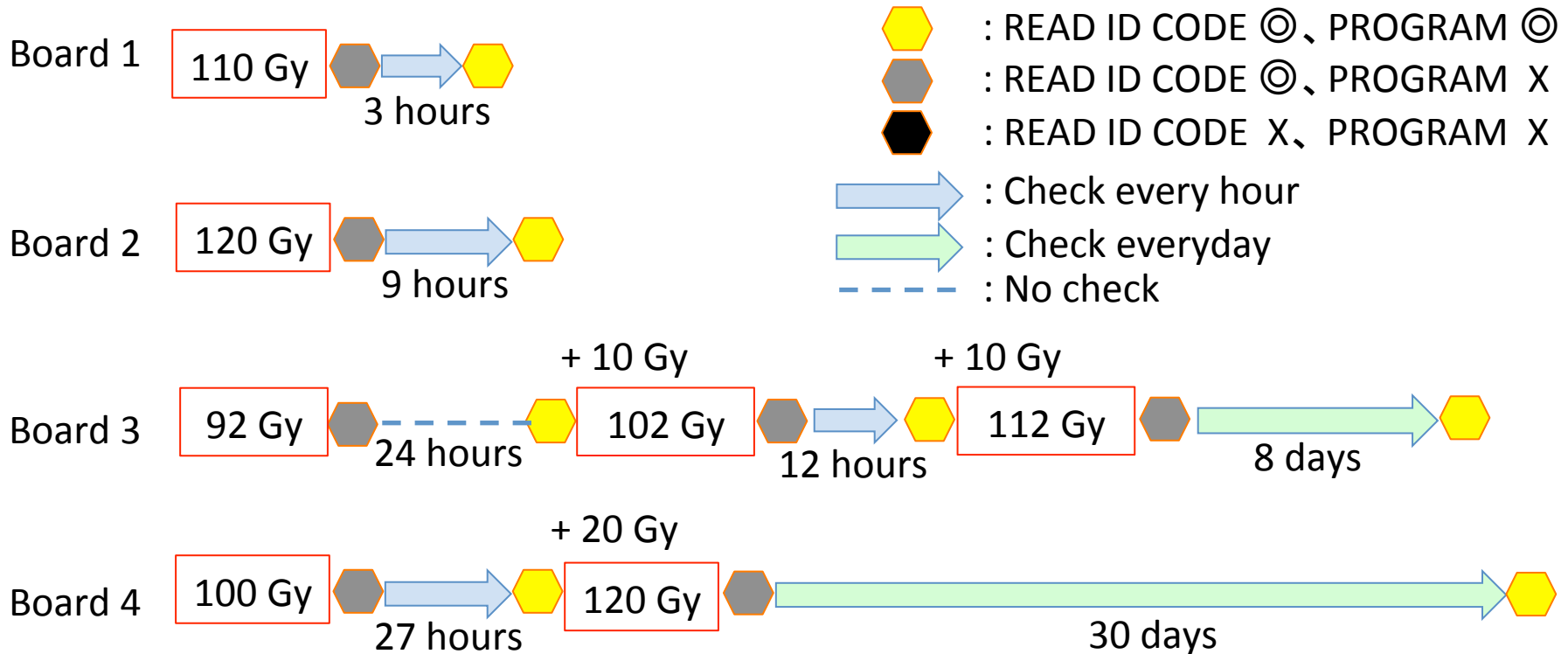


Recovery of the functions

- 8 boards were irradiated. 92-300 Gy depending on the boards.
- Discharge of the insulator layer
 - ⇒ Possibility of the functional recovery.
- Recovery investigated after the irradiation.
 - 4 boards with the error in PROGRAM: in room temperature
 - 4 boards with the error in READ ID CODE
 - 2 boards: room temperature
 - 2 boards: room temperature, 75°C after some weeks

Results of recovery of the functions (1)

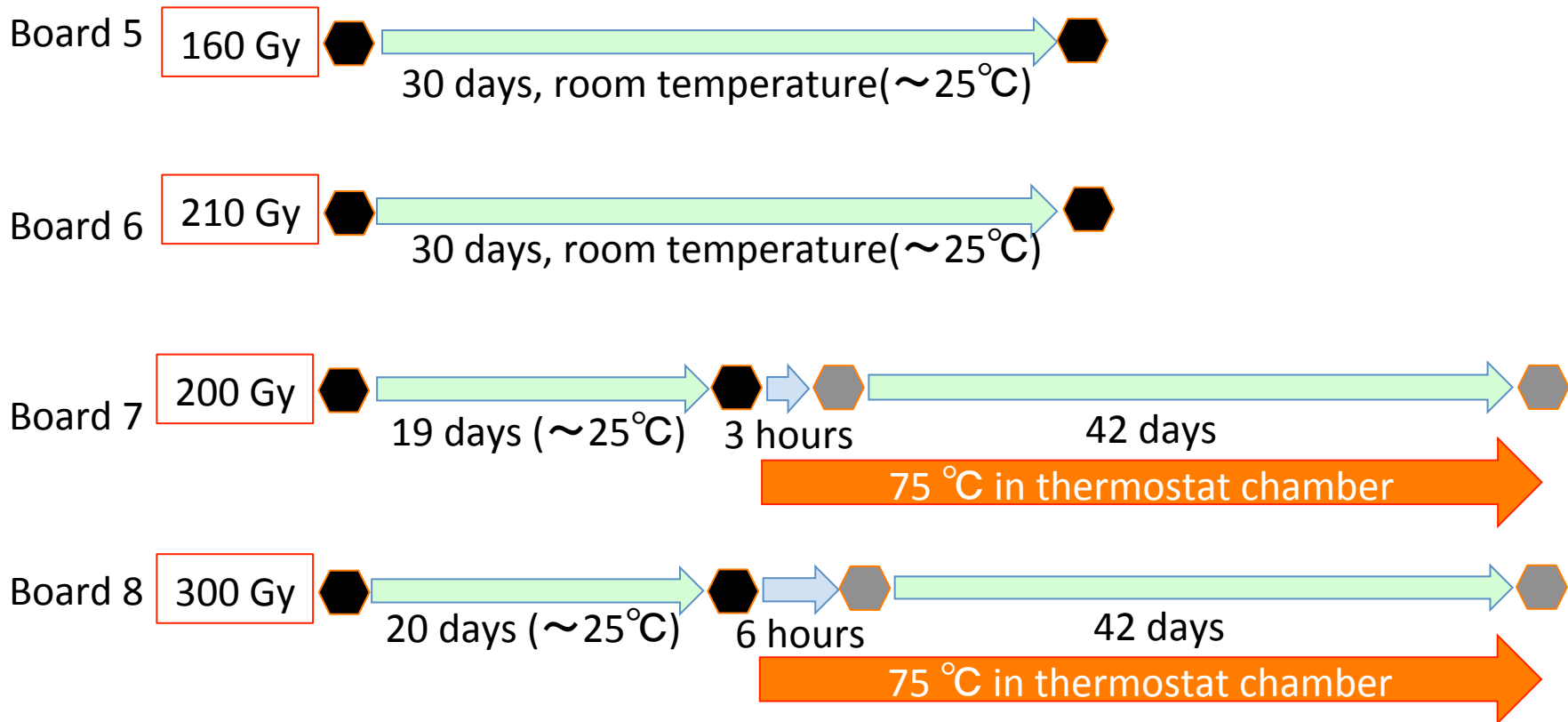
The four boards were kept in room temperature ($\sim 25^{\circ}\text{C}$)



- PROGRAM (firmware download) recovered in a few hours at the irradiation level of about 100 Gy.
- The time needed for the recovery seems to have correlation with the total dose.

Results of recovery of the functions (2)

 : READ ID CODE ©、PROGRAM X
  : READ ID CODE X、PROGRAM X



- READ ID CODE was recovered by “annealing” in the high-temperature environment of 75 °C.
- Implemented firmware, i.e. ring oscillator and SERDES, also recovered.

IGLOO2 TID test summary

Configuration memory

- 80 – 90 Gy : Error in VERIFY
- 110 – 120 Gy : Error in PROGRAM
- 160 – 210 Gy : Error in READ ID CODE

Ring oscillator and SERDES

- Firmware not functional after the irradiation around 200 Gy.

TID effects on the configuration memory could be larger than the ones on ring oscillator and SERDES due to thicker insulator layers.

Recovery

- Recovery of the ring oscillator and SERDES with the temperature of 75°C observed.

Summary

- FPGA is widely used in high energy physics experiments.
- In this report, flash-based IGLOO2 FPGA is focused on.
- Performance of TDC (0.78 ns bin, 24 channels) evaluated.
 - Differential non linearity ≤ 0.4 LSB
 - Integral non linearity is consistent with zero in the full dynamic range
 - Time resolution: measured to be about 0.25 ns
- TID effect evaluated with gamma ray irradiation.
 - Firmware download got impossible at around 100 Gy.
 - SERDES and NAND ring oscillator seem to survive with a higher dose of 100-200 Gy.
 - Function recovery observed. Could be accelerated by higher temperature.

This study provides useful information about the use of IGLOO2 FPGA in high energy physics experiment.