TOTAL IONIZING DOSE EFFECTS ON A 28NM HI-K METAL-GATE CMOS TECHNOLOGY UP TO 1 GRAD

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Outline

- Motivations for 28nm
- Test structure and test setup description
- TID irradiation for nMOSFETs
- TID irradiation for pMOSFETs
- Conclusions

The goal

- The talk will discuss the results of a Total Irradiation Dose (TID) test on a 28nm High-k CMOS technology for applications in instrumentation electronics for particle physics

Why 28nm?

MOTIVATIONS

- Future High Energy Physics Experiments read-out will have to face two key problems
  - Extremely **large radiation total-dose** (Up to 1Grad in 10 years for HL-LHC)
    - Much larger than in any previous situation
    - Present (250nm, 130nm) or under-development (65nm) electronics could fail
  - Extremely **large number of channels** (Increasing power consumption)
- New electronics to be designed
  - rad-hard performance
  - low-power consumption
- Open question: which is the best tech-node for future implementations in terms of
  - Radiation hardness to 1Grad
  - Low-power consumption
  - Technology access (availability, cost, etc..)

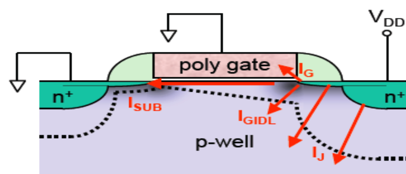
NEW TECHNOLOGIES

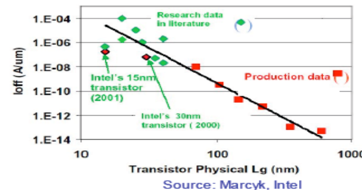
- New technologies offer options in terms of
  - Minimum gate size (65nm, 45nm, 32nm, 28nm, or below)
  - Technology features (CMOS-bulk, CMOS-FinFET, CMOS-SOI, etc)
  - Technology access and cost (not only for prototyping but also for the final production)

- There is a general trend to move ASICs to scaled technologies
  - **Higher digital circuits density** to include more digital funtionalities
  - **Higher speed** to achieve improved performance in terms of larger bandwith
  - **Lower power consumption**

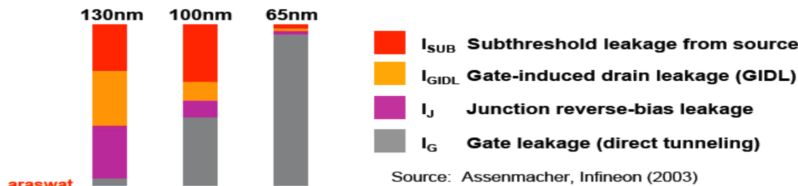
- The cost of 65nm, 45nm, 28nm will become comparable
  - The cost is not anymore a selection reason.
  - The technology can then be chosen in term of performance quality

HIGH-K GATE DIELECTRICS





Relative contributions of OFF-state leakage (but magnitude of total leakage getting exponentially worse for deeper submicron nodes)



Year of Production *DRAM ½ Pitch*	*2004* *90 nm*	*2005* *80 nm*	*2006* *70 nm*	*2007* *65 nm*	*2010* *45 nm*
Physical Gate Length MPU/ASIC (nm)	37	32	28	25	18
Equivalent physical oxide thickness for MPU/ASIC Tox (nm)	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8
Gate dielectric leakage at 100°C (mA/µm) High-performance	0.1	0.3	0.7	1.0	3.0
Equivalent physical oxide thickness for low standby power Tox (nm)	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	0.9-1.3
Gate Dielectric Leakage (pA/µm) LSTP	1.0	1.0	1.0	1.0	3.0
Thickness control EOT (% 3s)	<± 4	<± 4	<± 4	<± 4	<± 4

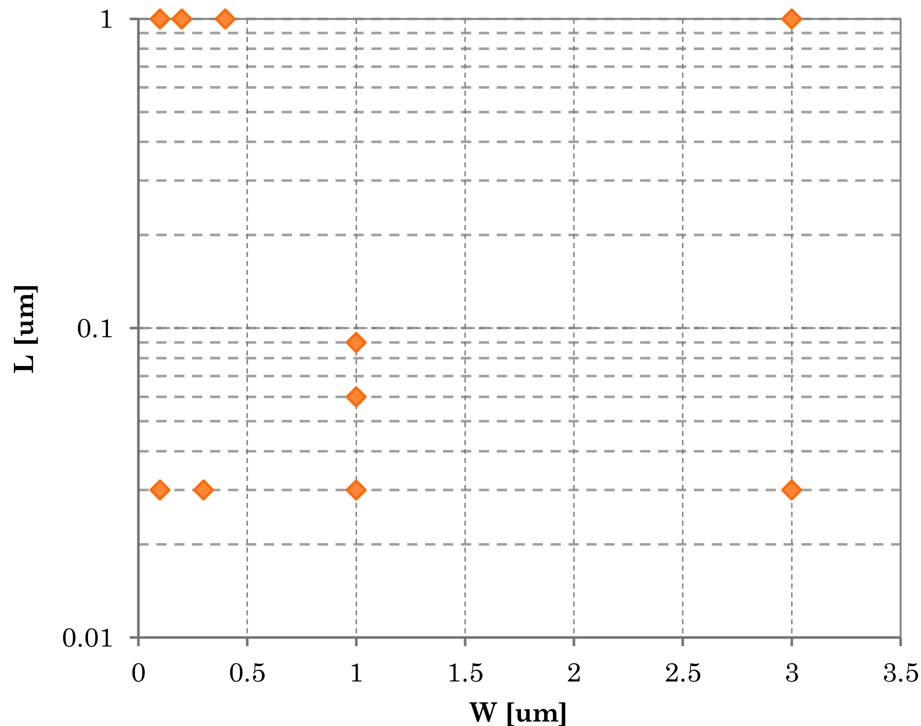
- As devices approach the sub-45 nm scale, the effective oxide thickness (EOT) of the traditional silicon dioxide dielectrics are required to be smaller than 1 nm (about 3 monolayers and close to the physical limit) → high gate leakage currents due to the quantum tunneling effect at this scale.

- To continue the downward scaling, dielectrics with a higher dielectric constant (high-k) are being suggested as a solution to achieve the same transistor performance while maintaining a relatively thick physical thickness

SCALTECH28 PROJECT

- Scaltech28 collaboration: INFN (Milano-Bicocca, Pavia, Padova) + CERN + EPFL-Neuchatel; started in 2014
- Goal: to investigate a 28nm high-k commercial bulk CMOS technology for pixel readout circuits for HL-LHC
- Analog front-end *(see F. Resta's talk on Tuesday 27th at this workshop)*, mixed analog digital circuits, radiation damage analysis and modeling
- Spring 2015: first tapeout submission including some test structures for TID tests
- Chips of the 1st submission delivered in October 2015

Test structure description

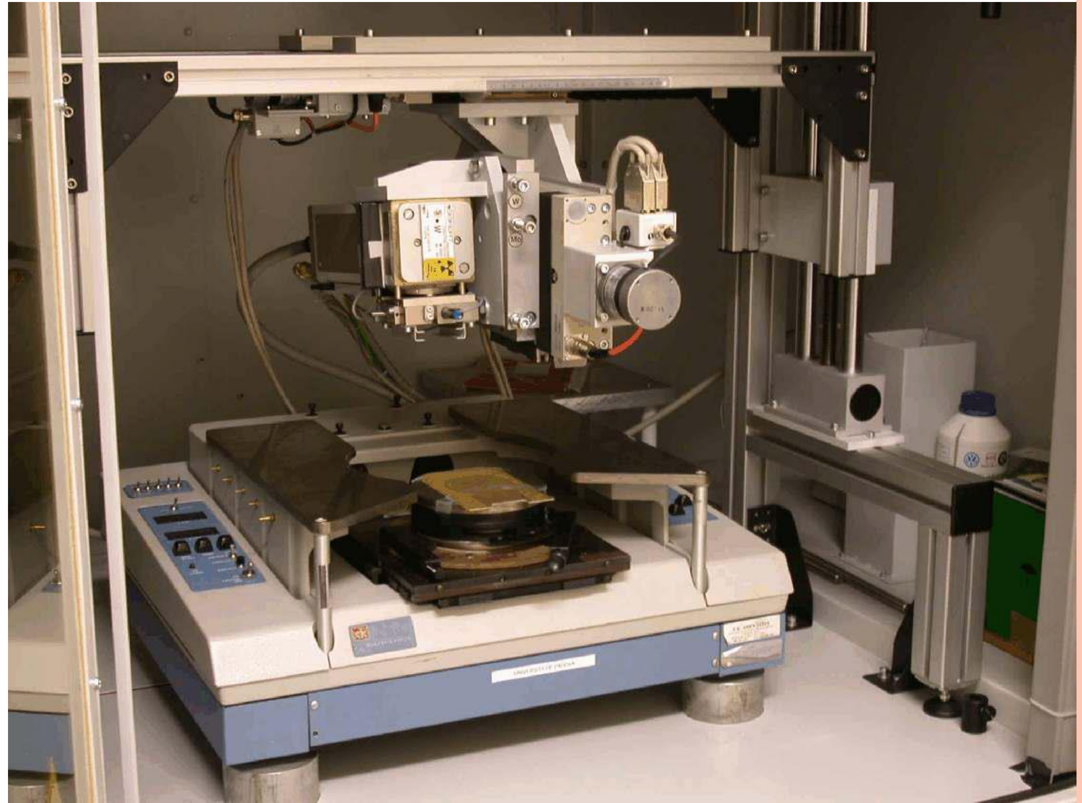


W	L
3u	1u
3u	30n
100n	1u
1u	30n
1u	60n
1u	90n
400n	1u
200n	1u
300n	30n
100n	30n

- Replicated for nMOSFET and pMOSFET
- Standard V_{th} and High V_{th}
- Only linear layout

IRRADIATION AND TEST SETUP DESCRIPTION

- Irradiation at the X-ray facility in Padova (Italy)
- Irradiations at room temperature
- Setup modified to increase the dose rate up to 8Mrad/h (5 days only for irradiation)
- Chip on a semi-automatic probe station
- Contacted with a probe card with 32 probes
- Switching matrix connecting to the Semiconductor Parameter Analyzer and bias



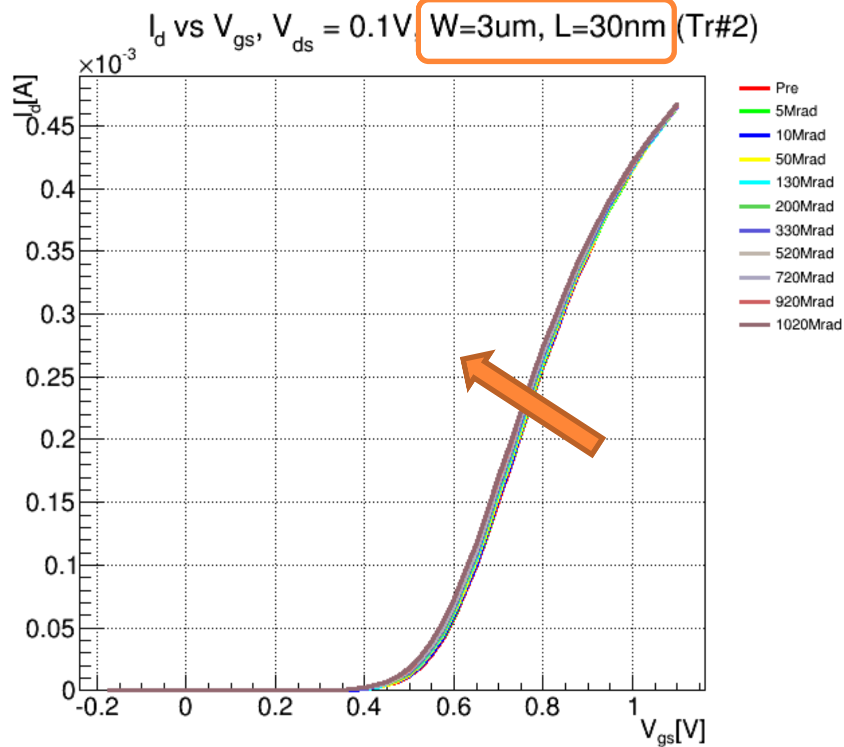
nMOSFET irradiations

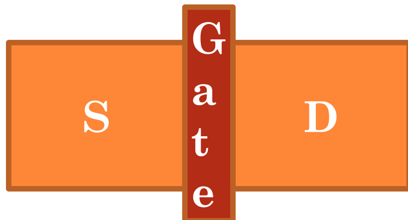
- Irradiations performed at Room Temperature
- Dose rate: 8.3 Mrad/h
- nMOSFET Standard V_{th}
- Bias during irradiation: $V_{gs}=V_{ds}=1.1V$
- Extracted parameters: I_{off}, I_{on}, V_{th}, g_m, Subthreshold Slope
- No annealing

W	L	
3u	1u	
3u	30n	W/L max
100n	1u	W/L min
1u	30n	
1u	60n	
~~1u~~	~~90n~~	
400n	1u	
200n	1u	
300n	30n	
100n	30n	

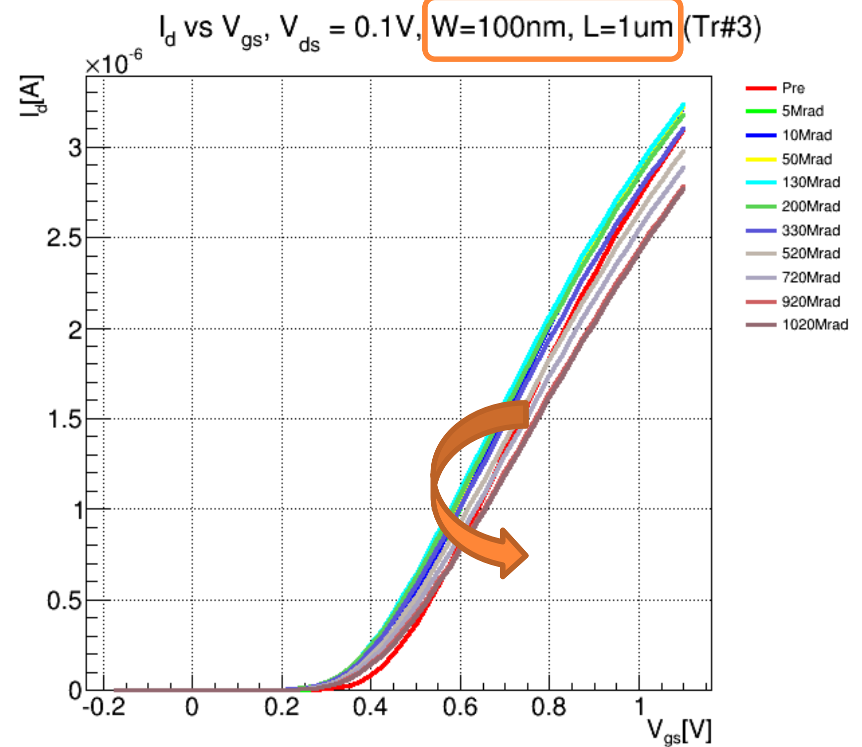
nMOSFET I_{DS}-V_{GS}

Max W/L

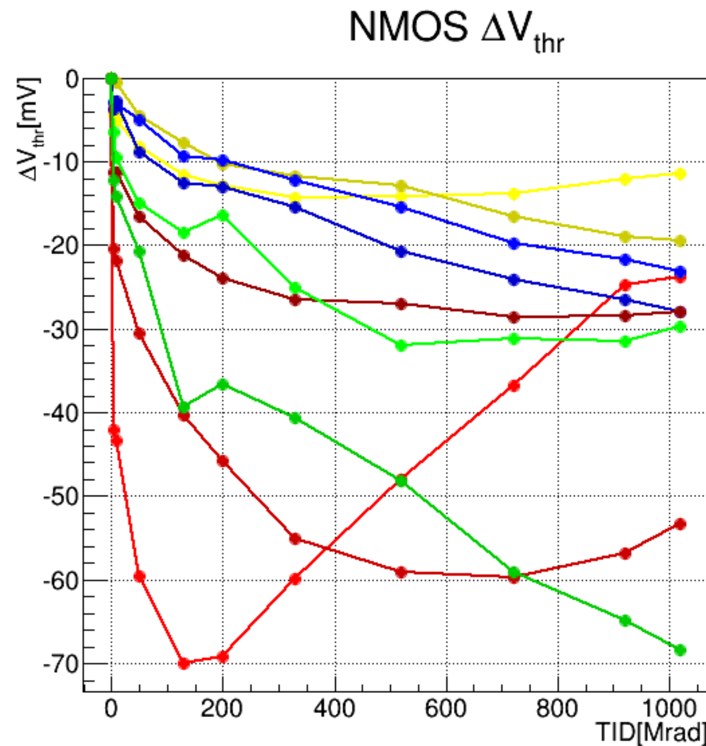


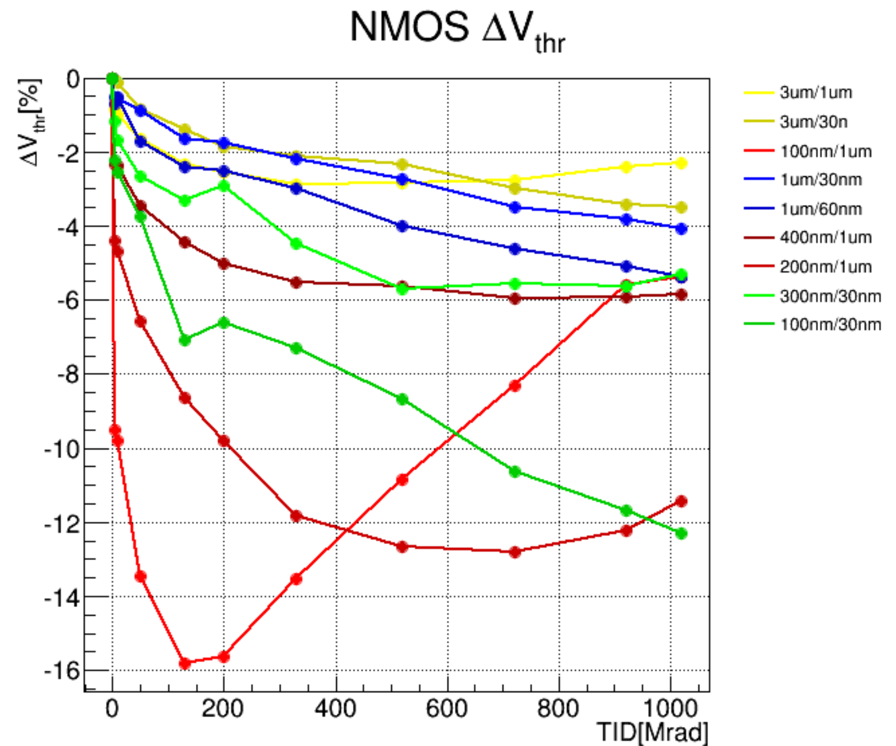


Min W/L



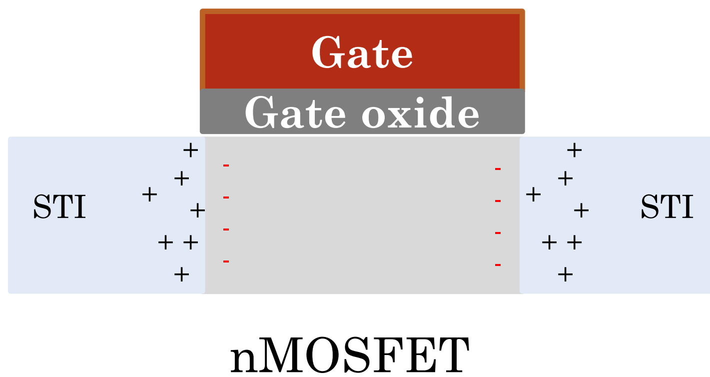
nMOSFET V_{TH} variation



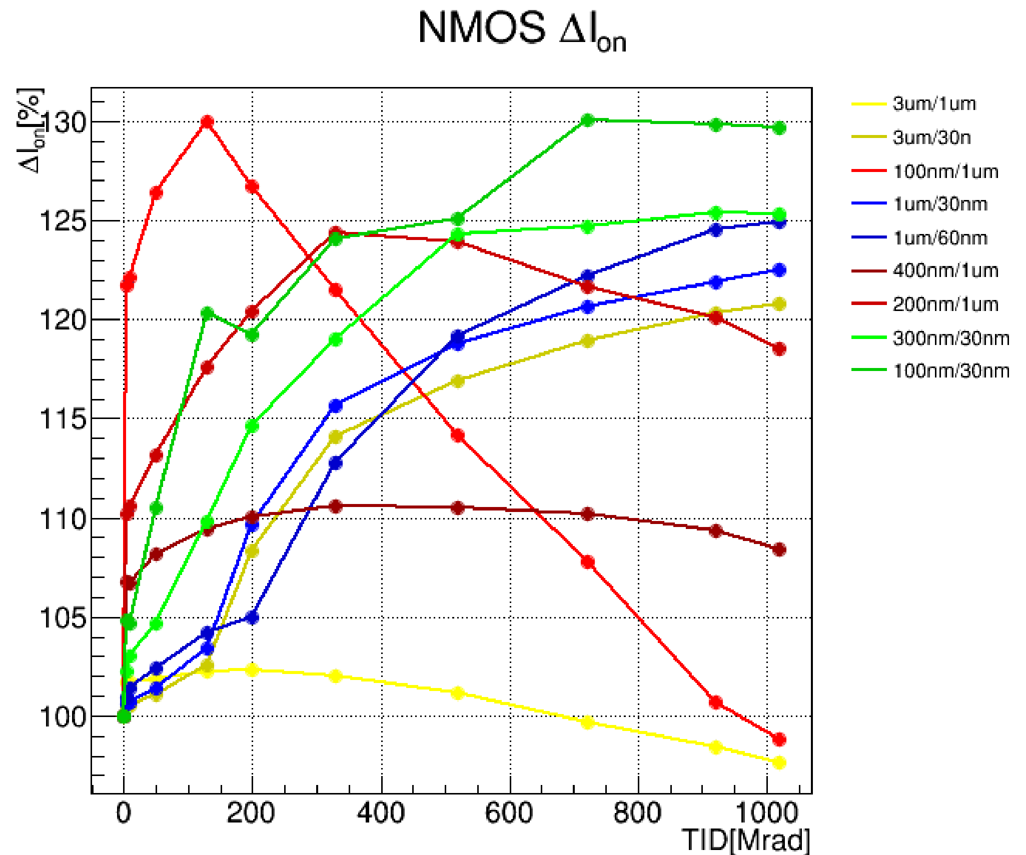


- Threshold voltage variation limited to few tens of mV (-12% in the worst case), within variability

nMOSFET I_{ON} VARIATION

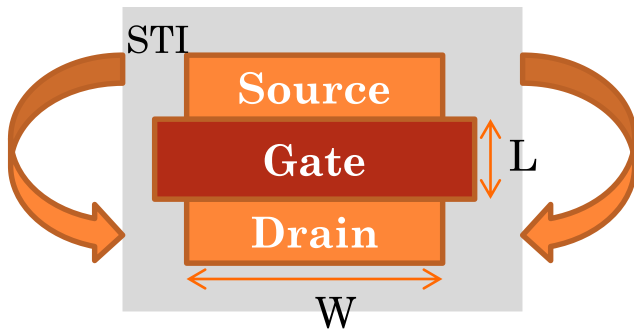


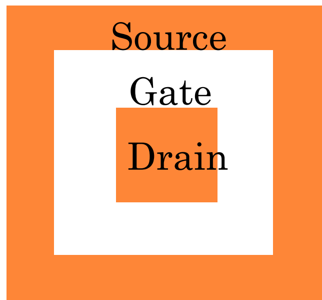
nMOSFET

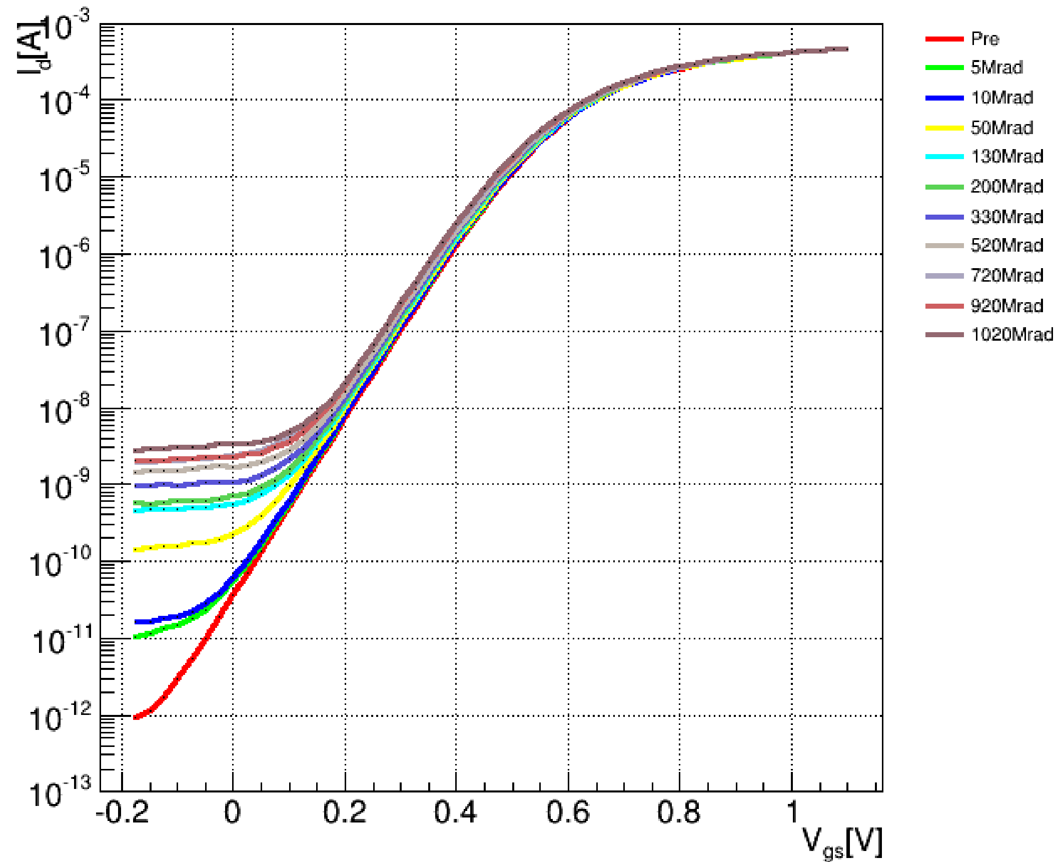


nMOSFET I_{LEAK}

- Leakage current (I_d @ V_{gs} =0) increases more than 3 orders of magnitude!

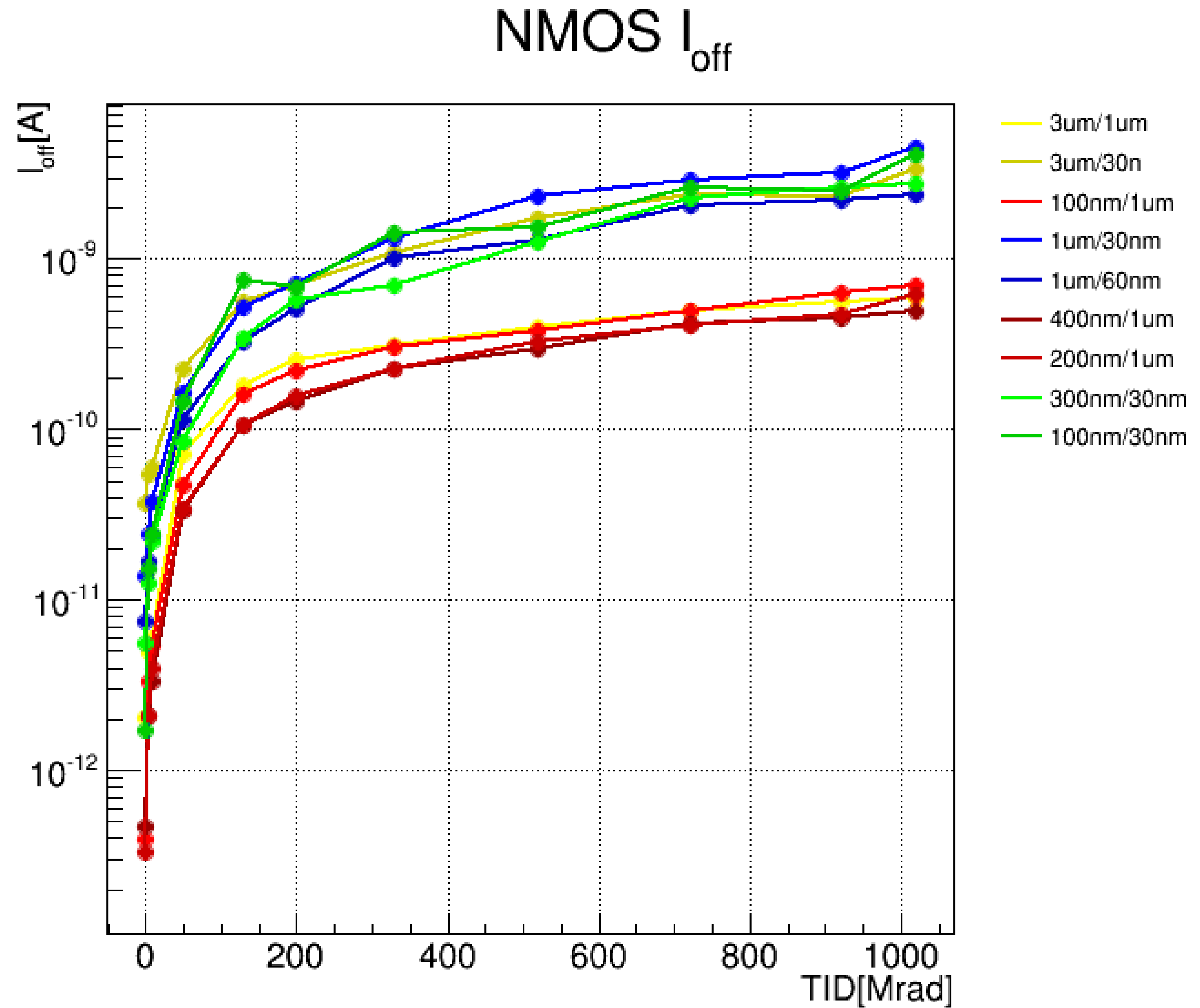






nMOSFET I_{LEAK} VARIATION

Leakage current increases between 2 and 3 orders of magnitude



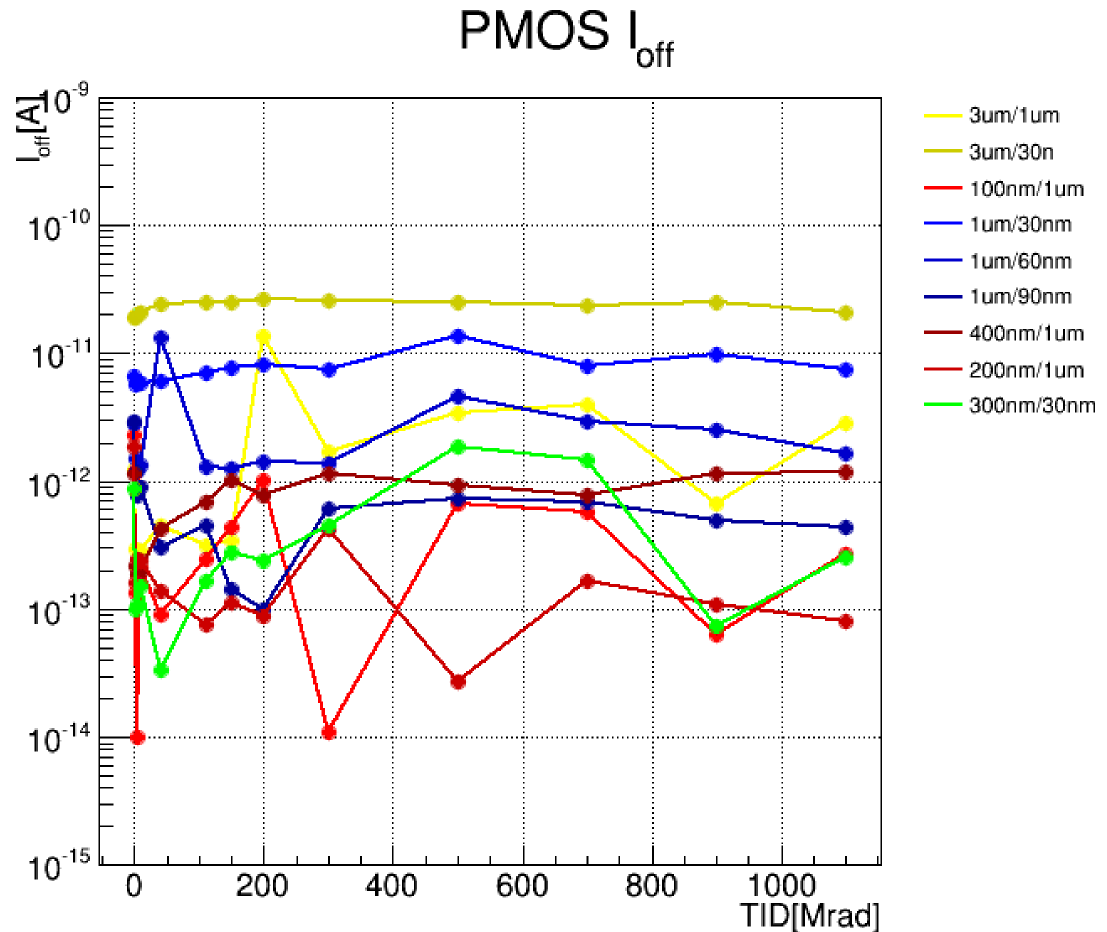
pMOSFET IRRADIATIONS

- Irradiations performed at Room Temperature
- Dose rate: 8.3 Mrad/h
- pMOSFET Standard V_{th}
- Bias during irradiation: $V_{gs}=V_{ds}=-1.1V$
- Extracted parameters: I_{off}, I_{on}, V_{th}, Subthreshold Slope
- No annealing

W	L	
3u	1u	
3u	30n	W/L max
100n	1u	W/L min
1u	30n	
1u	60n	
1u	90n	
400n	1u	
200n	1u	
300n	30n	
100n	30n	

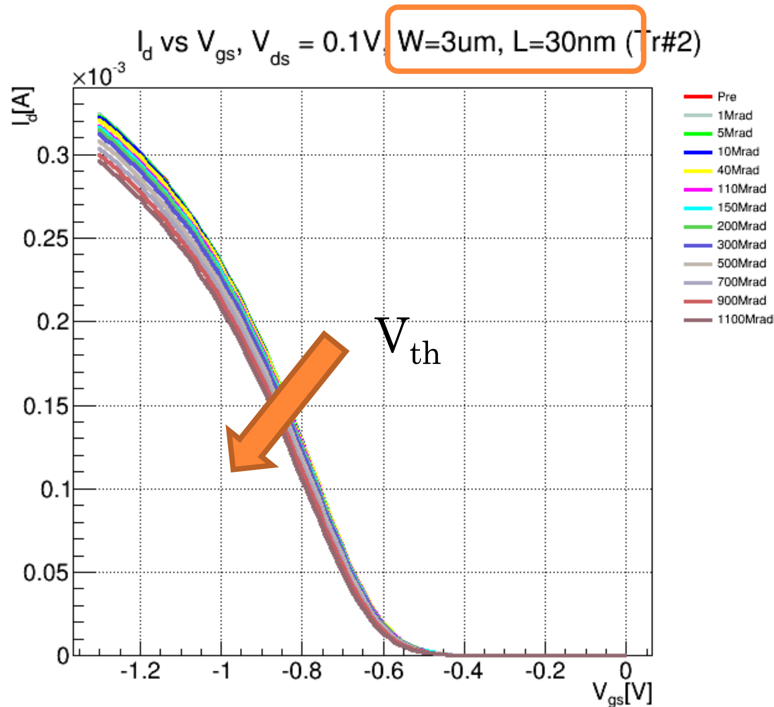
pMOSFET I_{LEAK}

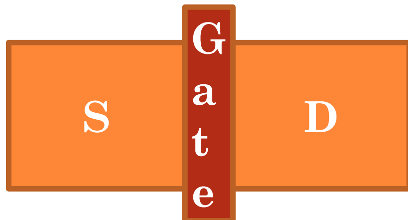
- No increase in leakage current (pMOSFETs are not subject to sidewall leakage current)



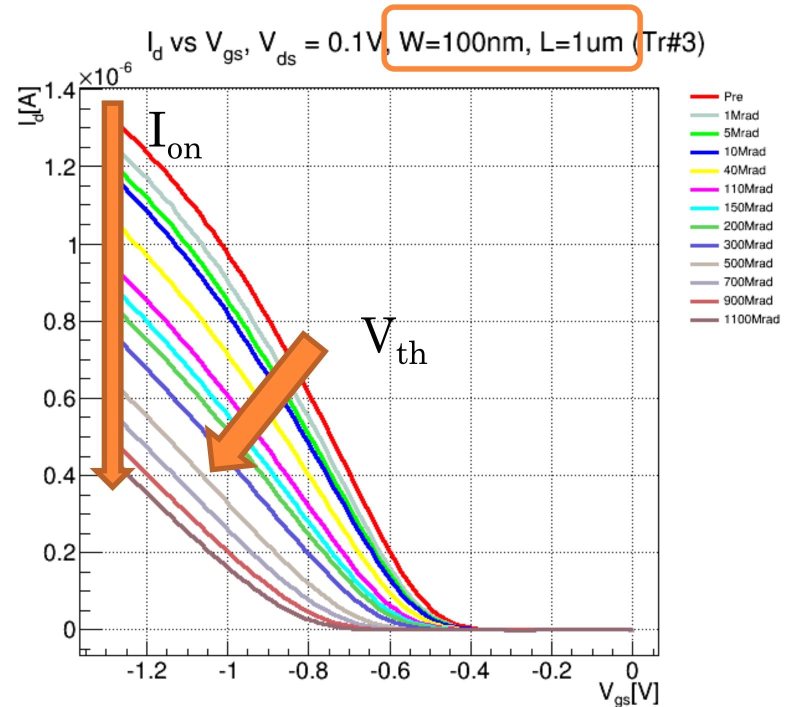
PMOSFET I_{DS}-V_{GS}

Max W/L

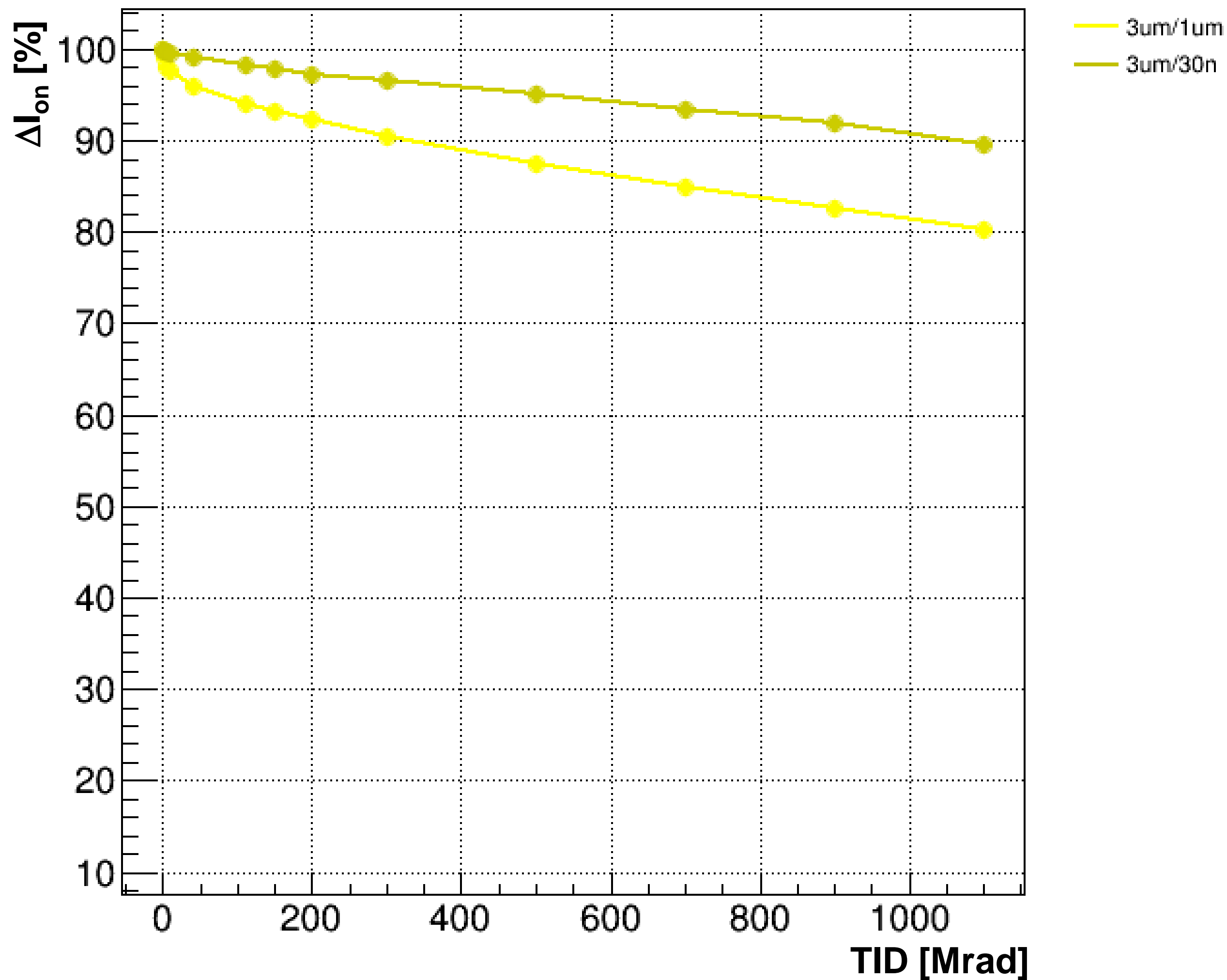




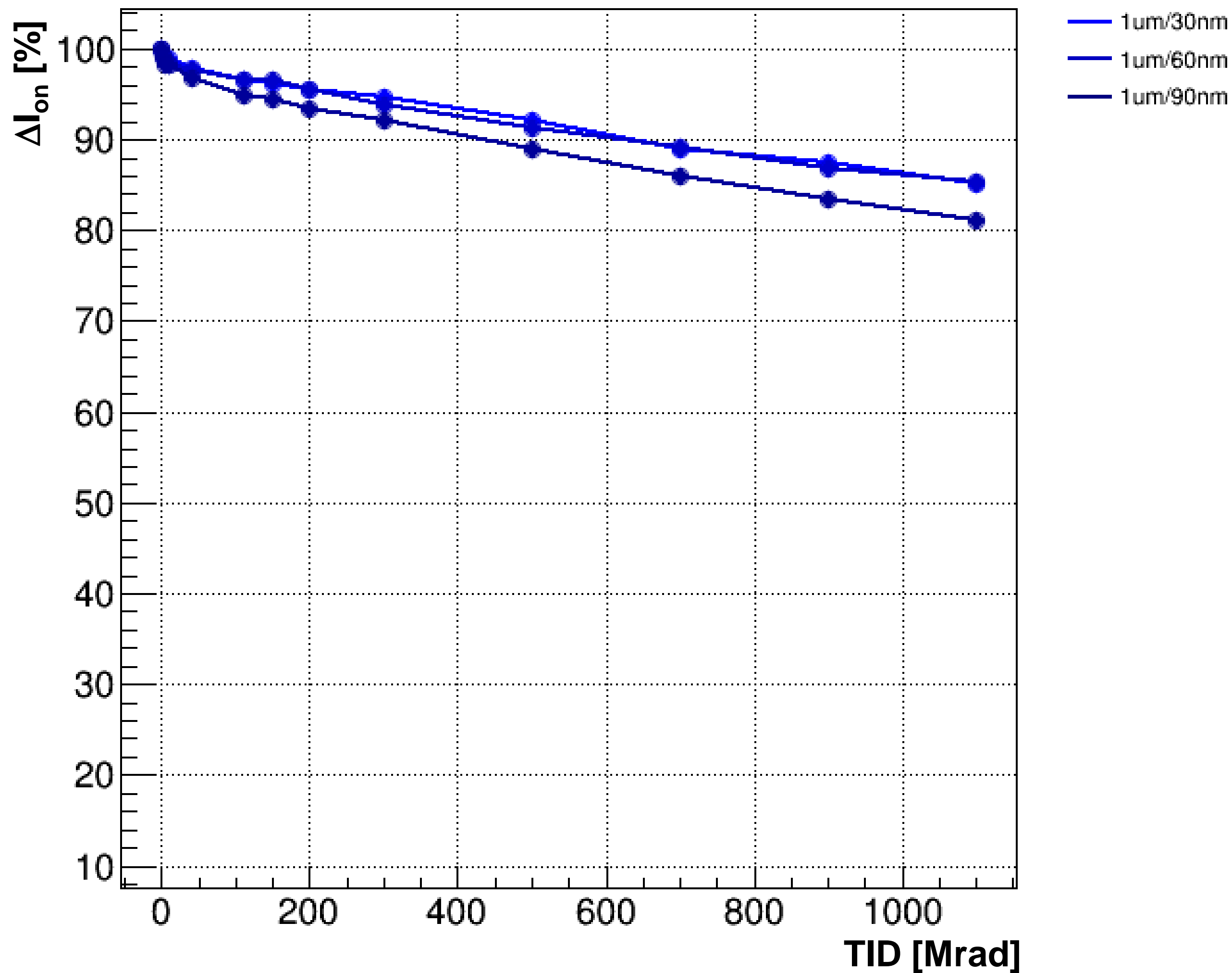
Min W/L



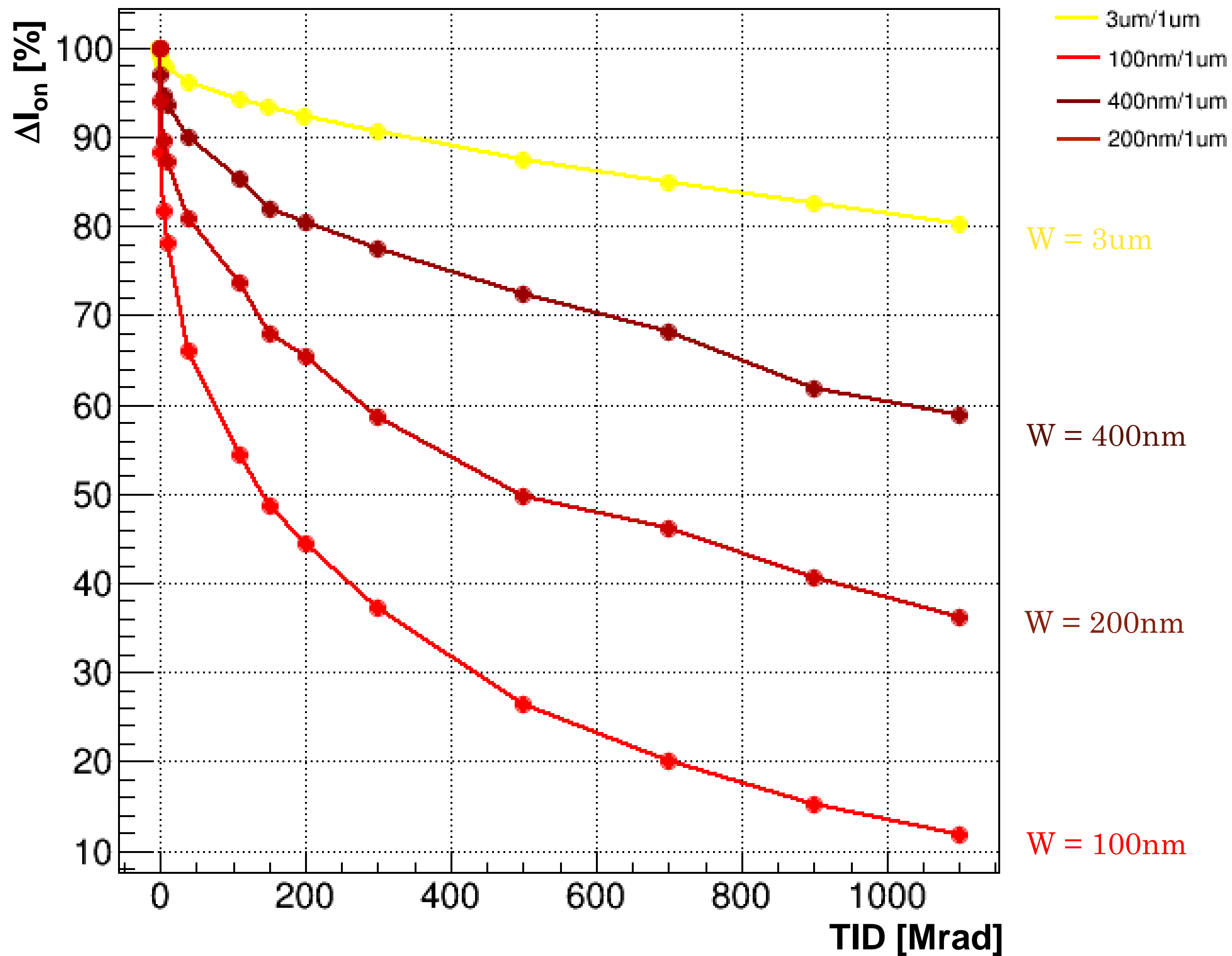
PMOSFET I_{ON} VARIATION



pMOSFET I_{ON} variation

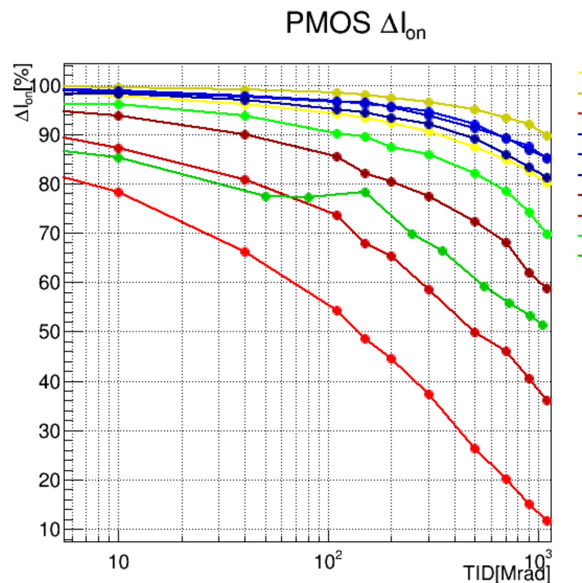


pMOSFET I_{ON} VARIATION



PMOSFET I_{ON} VARIATION

- Dramatic decrease of I_{on} more pronounced for narrow transistors
- No clear dependance on transistor length



PMOS ΔI_{on}

ΔI_{on}[%]

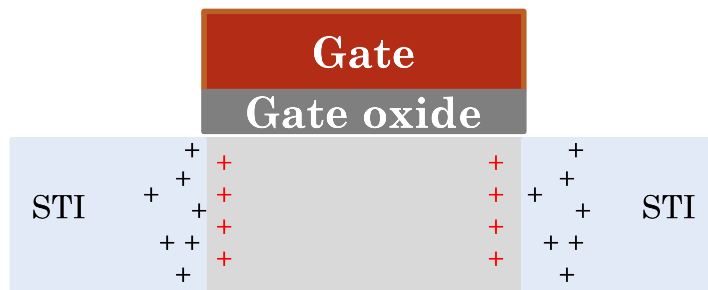
100
90
80
70
60
50
40
30
20
10

0
200
400
600
800
1000
TID[Mrad]

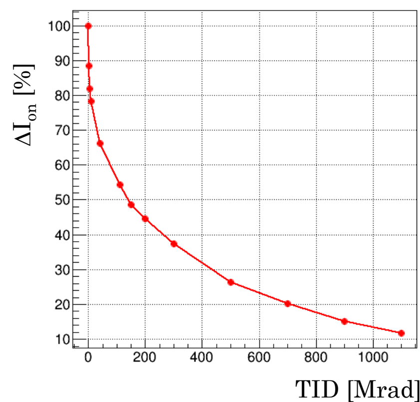
3um/1um
3um/30n
100nm/1um
1um/30nm
1um/60nm
1um/90nm
400nm/1um
200nm/1um
300nm/30nm
100nm/30nm

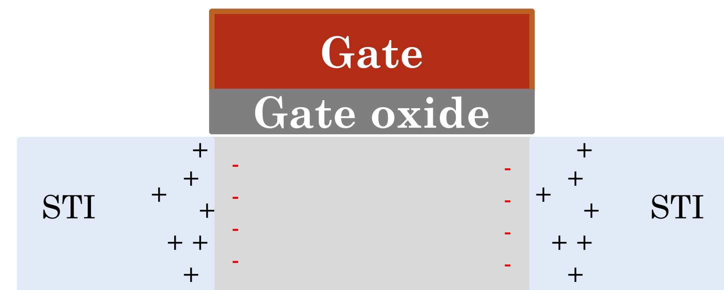
RINCE (1)

- Radiation Induced Narrow Channel Effect is related to charge trapping in the STI oxides

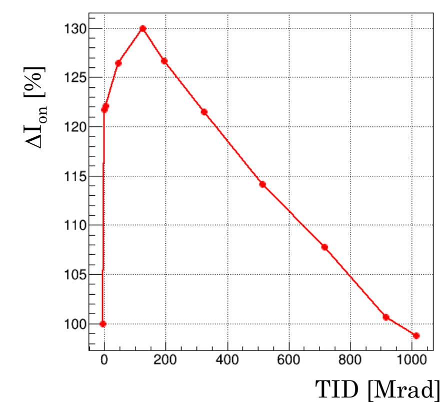


pMOSFET





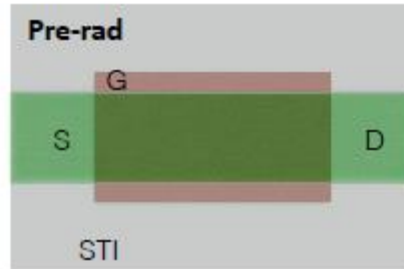
nMOSFET

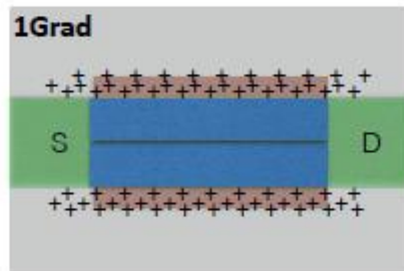


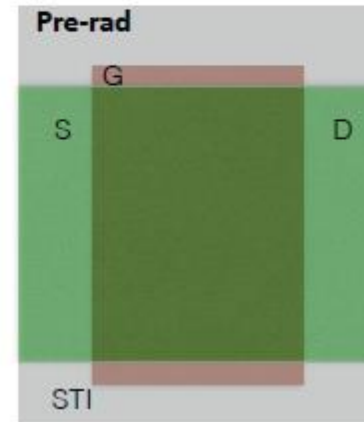
RINCE (2)

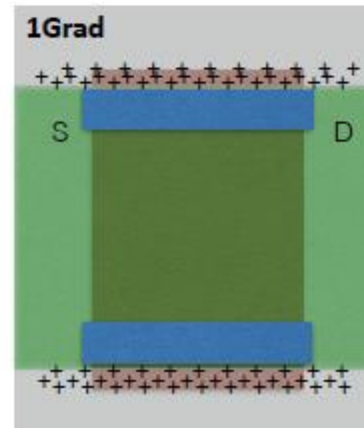
W=min size

W=moderate size





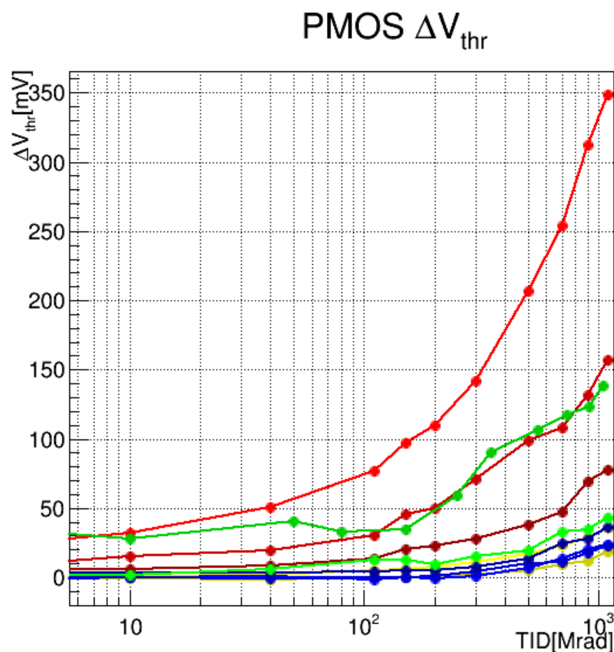


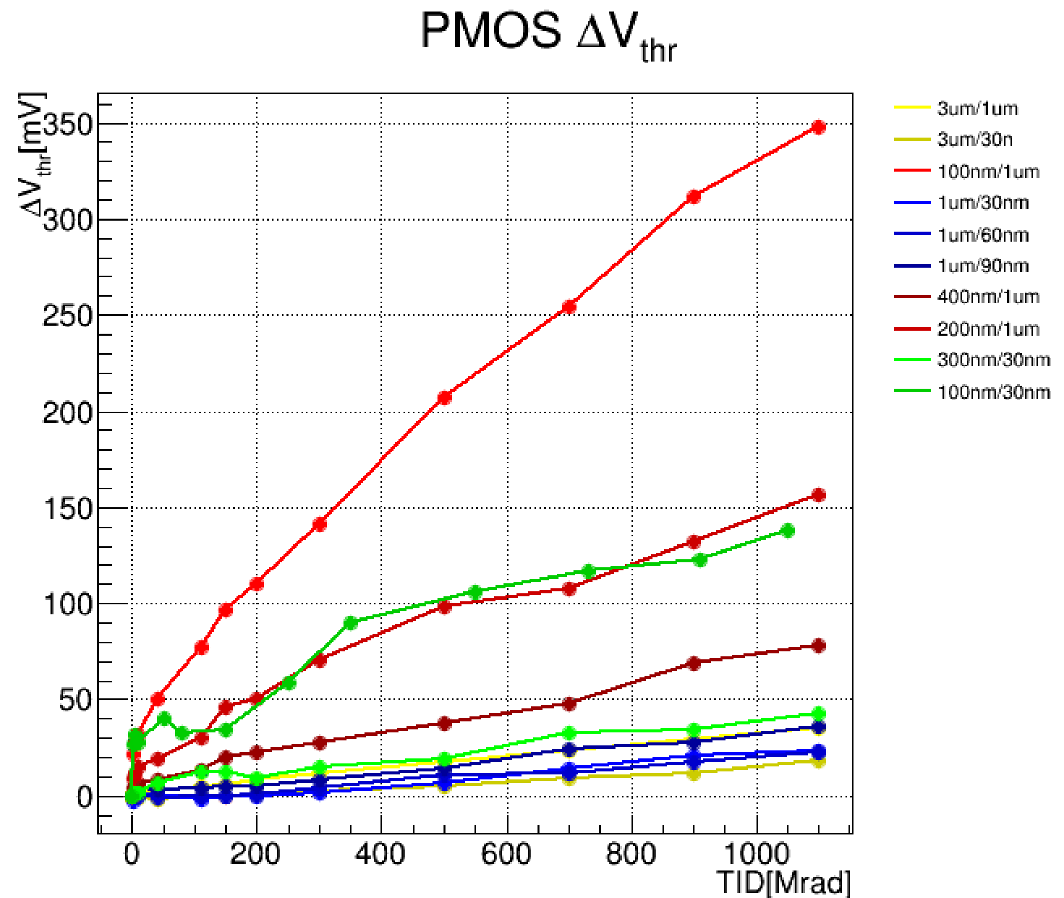


F. Faccio's talk at TWEPP 2015

PMOSFET V_{TH}

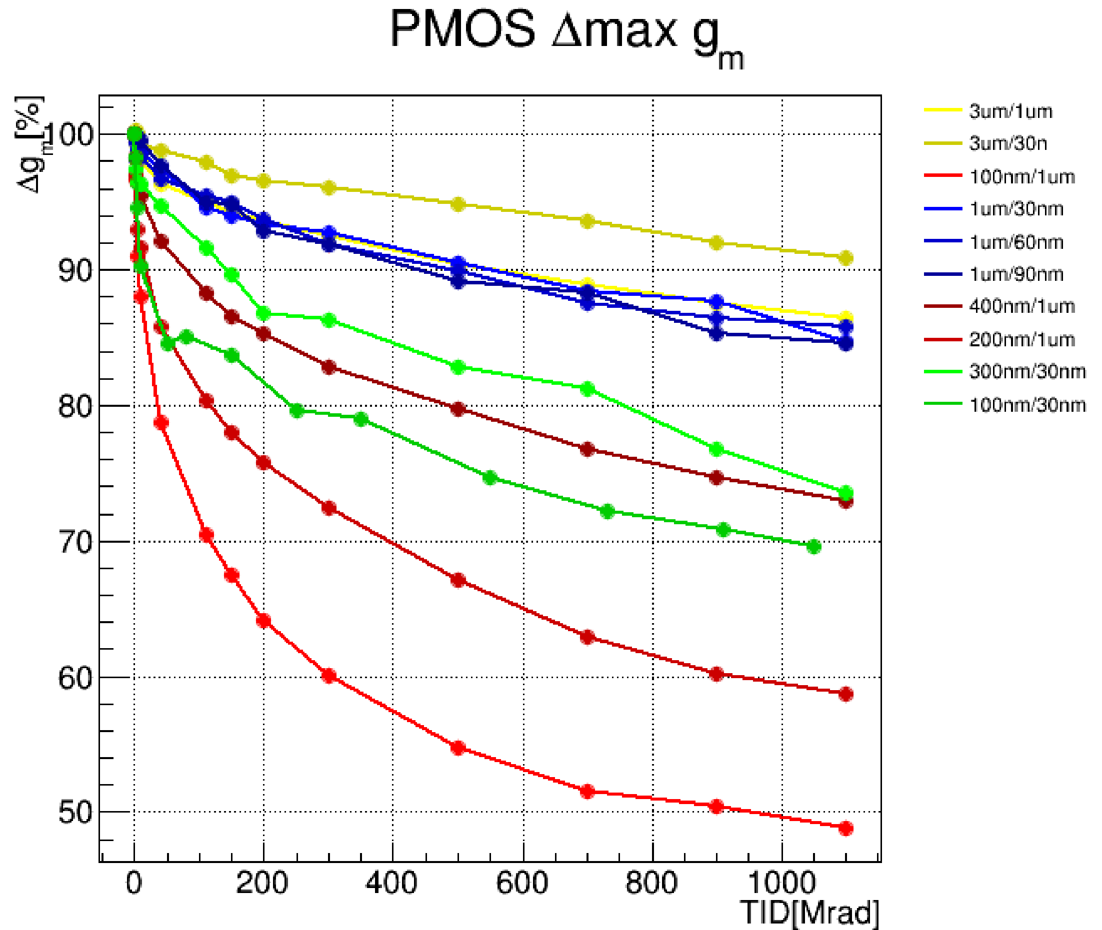
- V_{th} shows a substantial increase (>80mV) for narrow transistors
- For wider devices, the variation is < 50mV





TRANSCONDUCTANCE

- g_m decrease is 50% for the narrowest transistor (mobility degradation)



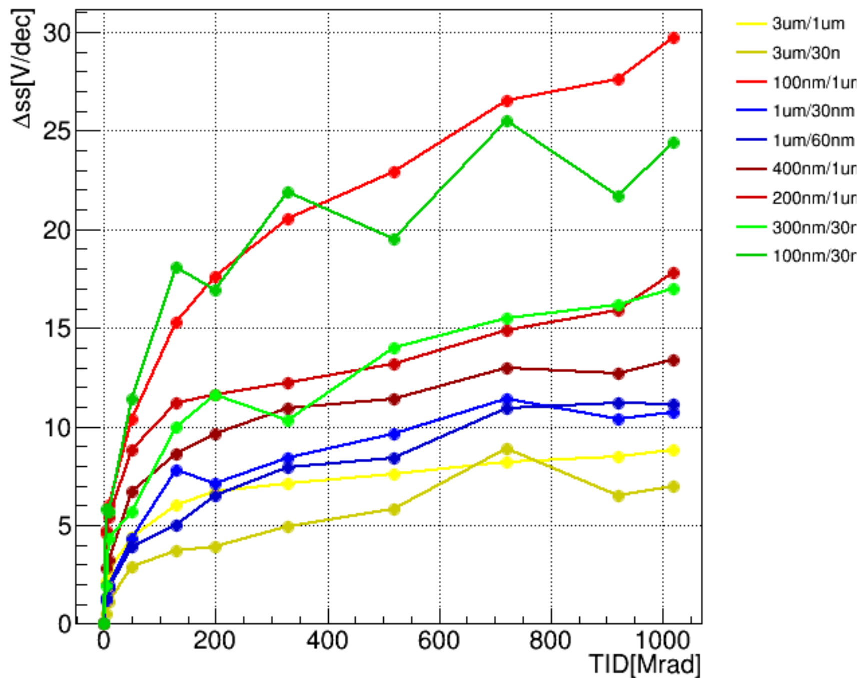
CONCLUSIONS

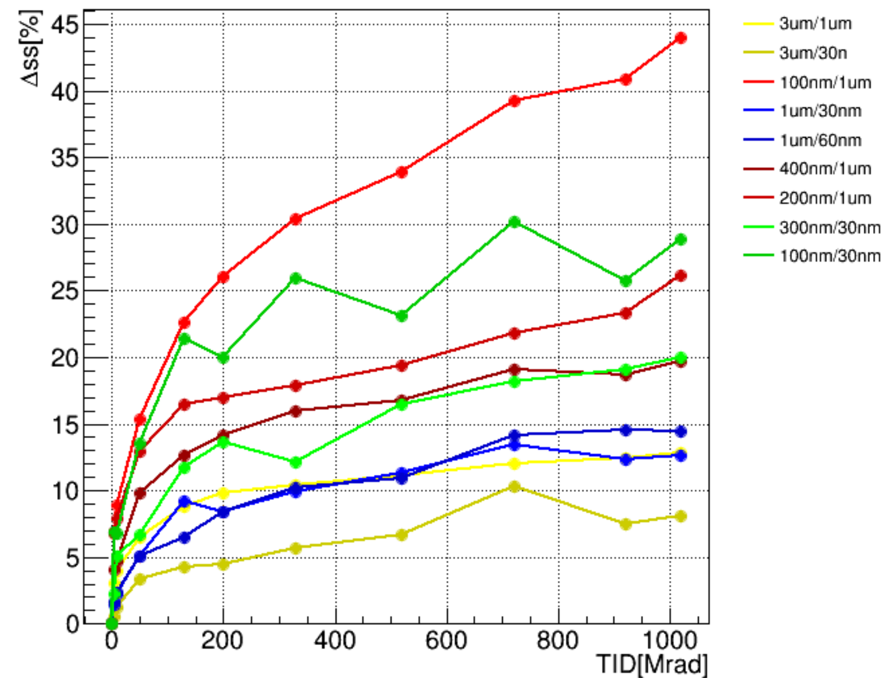
- No unexpected behavior due to the use of high-k oxides
- nMOSFET transistors have a limited damage due to TID (significant increase of leakage current)
- pMOSFET are much more affected by TID due to charce trapping in the STI oxides (dramatic loss of I_{on})

- No possibility to irradiate at low Temperature
- No Enclosed Layout Transistors

BACKUP

nMOSFET Subthreshold slope

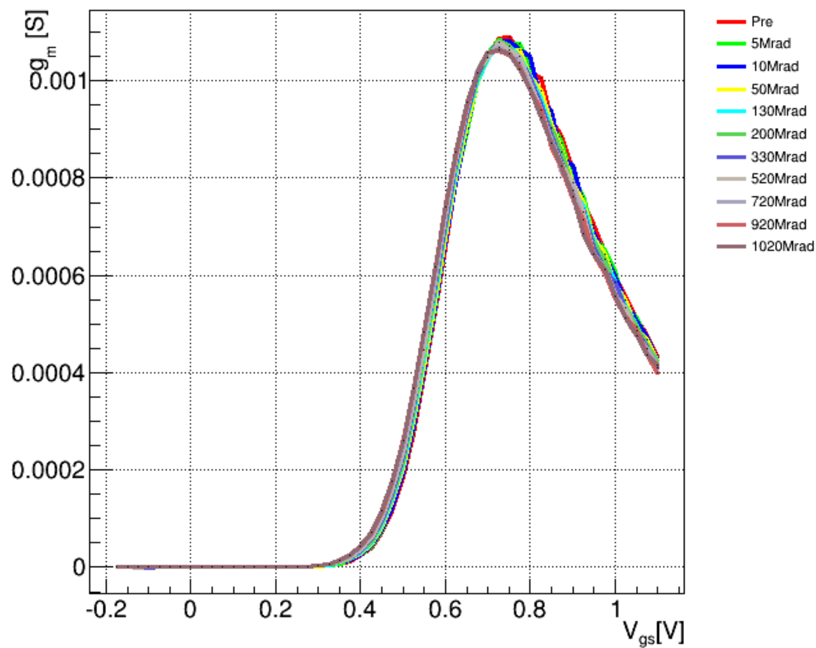




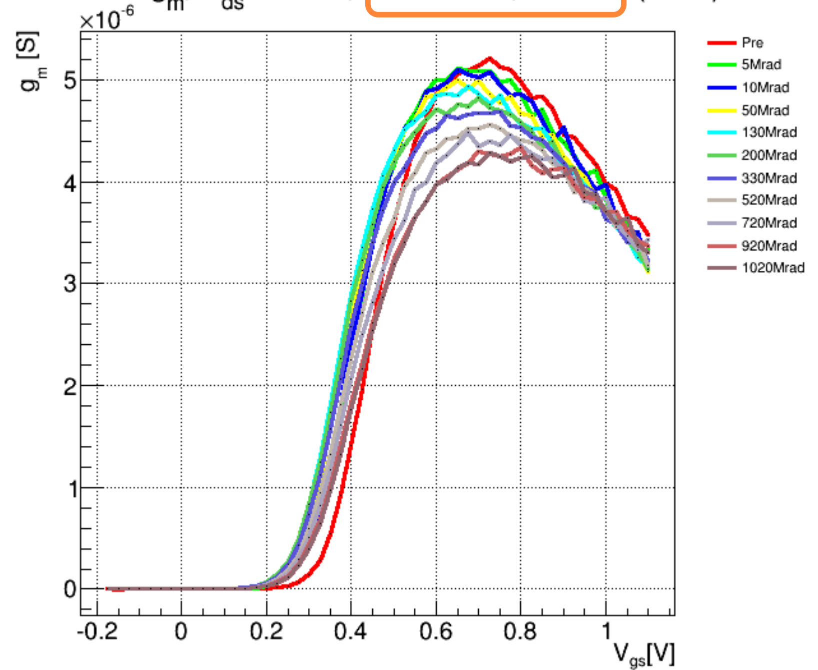
- Moderate ss variation (except for the minimum W/L transistor)

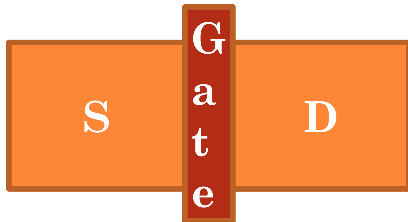
nMOSFET: TRANSCONDUCTANCE

Max W/L

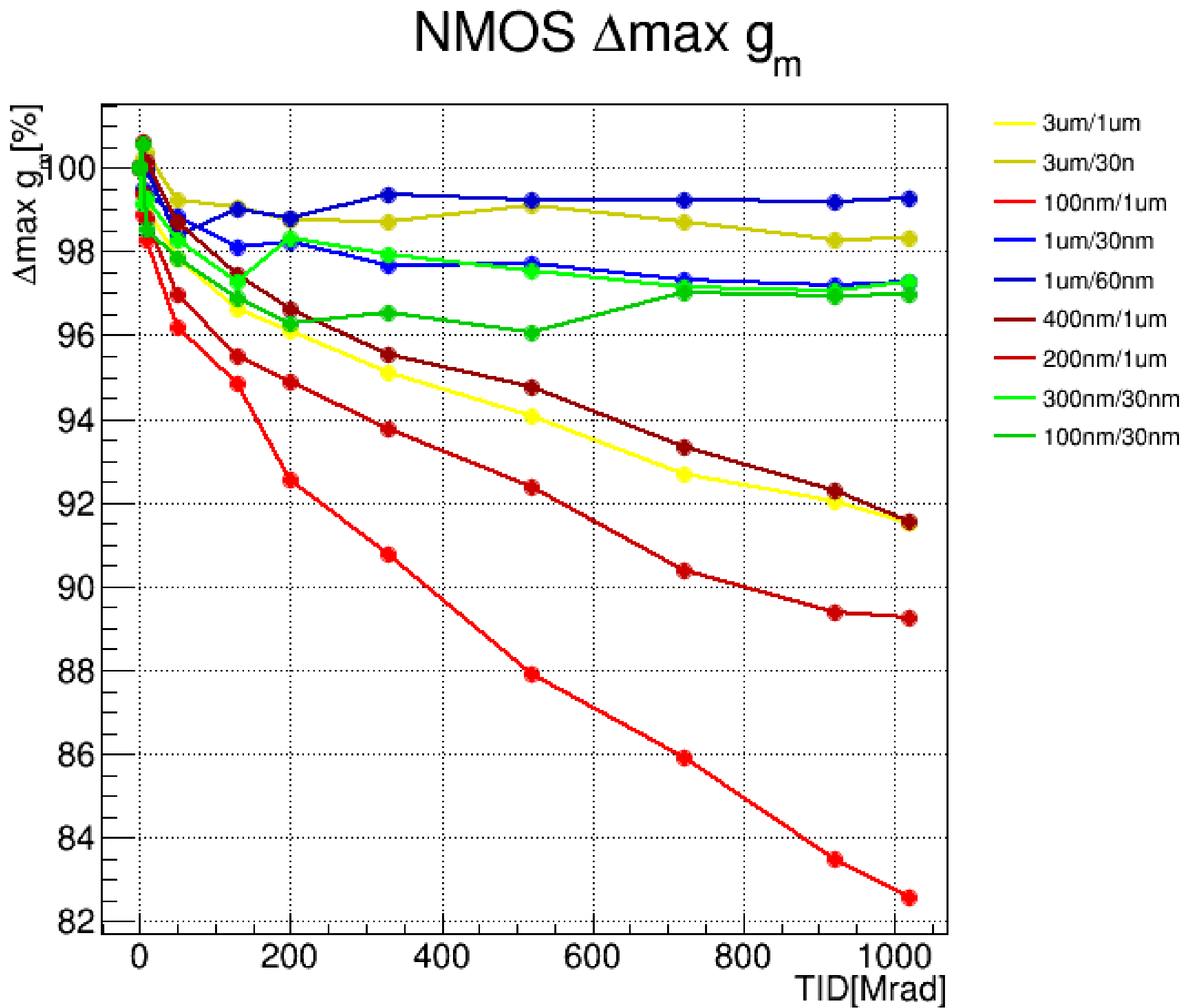


Min W/L



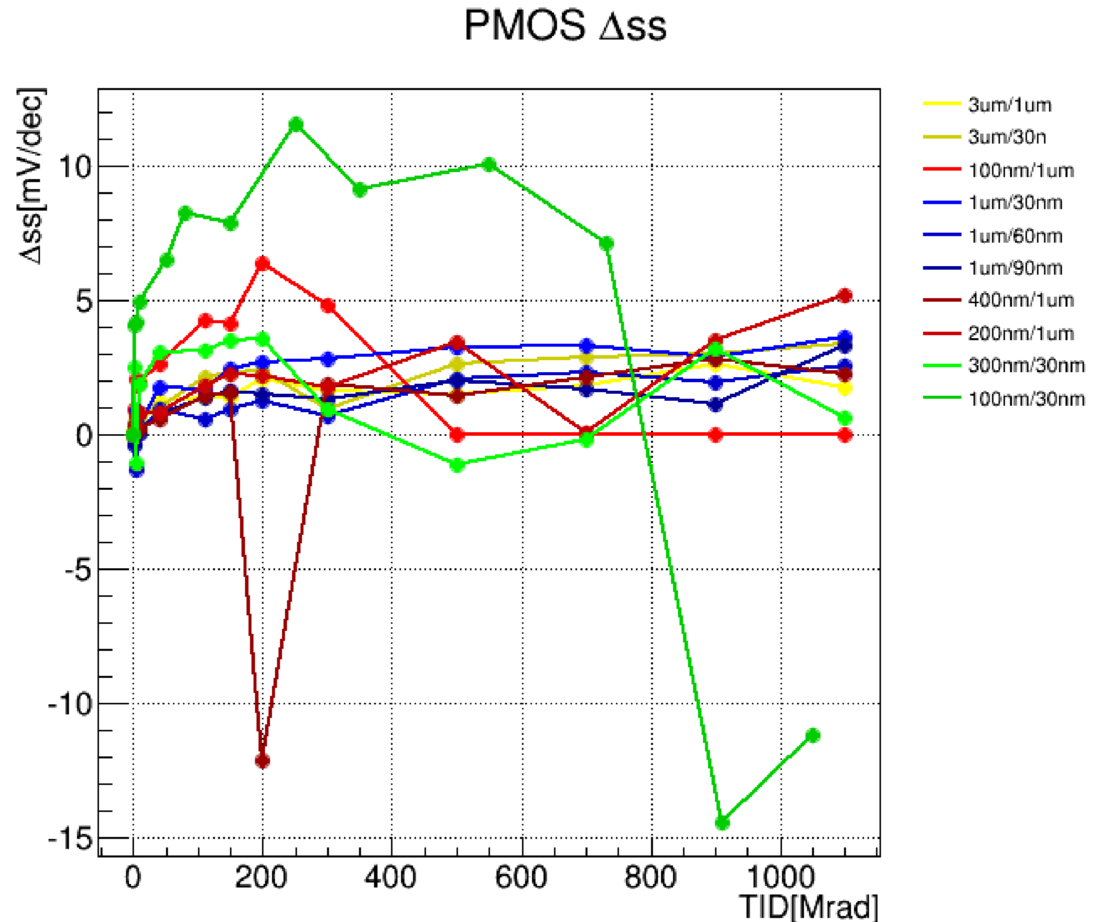


nMOSFET: TRANSCONDUCTANCE LOSS



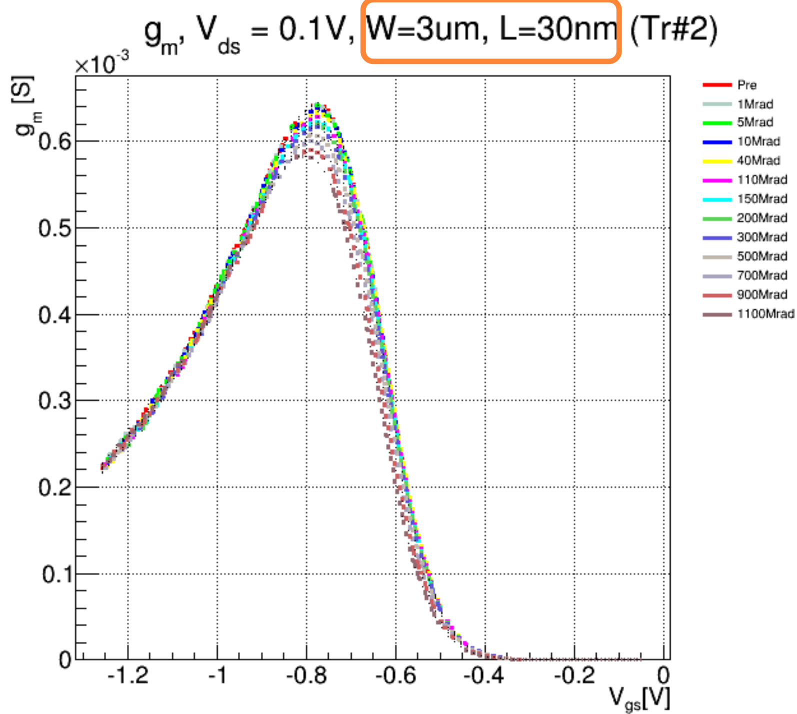
pMOSFET Subthreshold slope

- No significant change in ss (for W/L minimum, ss extraction is difficult for TID > 500 Mrad): limited contribution coming from Q_{it}

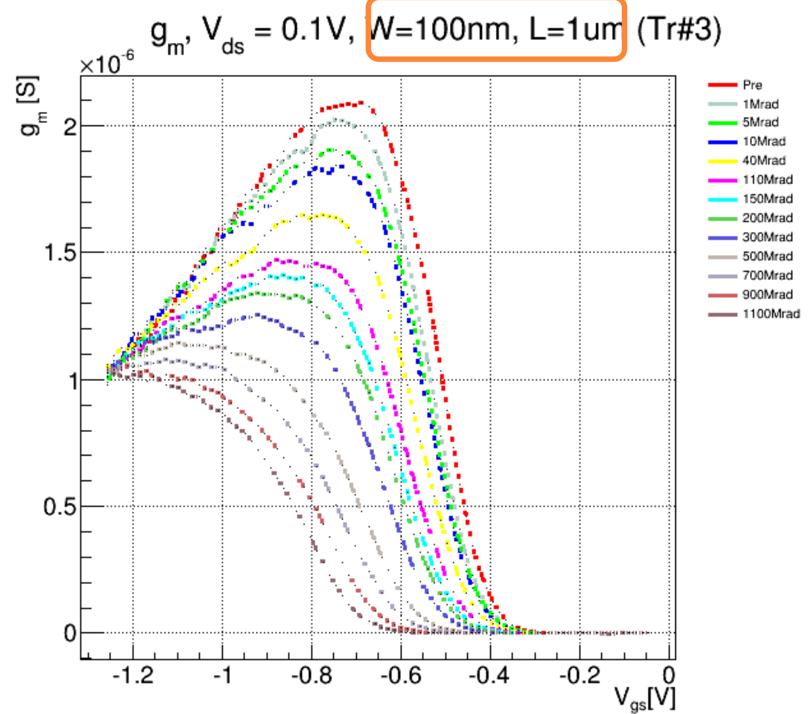


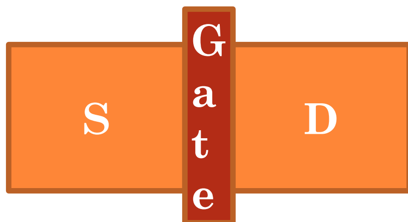
pMOSFET transconductance

Max W/L



Min W/L





pMOSFET transconductance