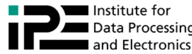

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Total Ionizing Dose effects on a 28nm Hi-K metal-gate CMOS technology up to 1 Grad

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This paper presents the results of an irradiation campaign up to 1 Grad on single transistors manufactured in a 28nm commercial CMOS technology. This technology is of interest for future upgrades for HL-LHC. NMOS transistors have been irradiated and electrical parameters have been measured. Moderate threshold voltage shift and sub-threshold slope degradation have been observed, while leakage current shows an increase of 3-4 orders of magnitude. These measurements are significant as this is the first technology evaluated for HEP applications using a High-K dielectric material for the transistor gate

Summary

During the next decade, the Large Hadron Collider at CERN will bring a factor ˜10 increase in collision rate. Silicon Vertex Trackers will require to read out large area sensor matrices of highly pixellated detectors with low power consumption and high level of processing. In addition, exceptional levels of Total Ionizing Dose (TID), up to 1 Grad, and NIEL up to 10^{16}neq are foreseen. In order to comply with such challenging requirements, designers are considering to move to higher density CMOS technology nodes for the pixel readout channels.

In this paper we present the results of an irradiation campaign at the transistor level for a 28nm commercial bulk CMOS technology. A test chip containing standard and high threshold voltage (Vth) nMOSFETs and pMOSFETs and with several channel widths (W) and lengths (L) was fabricated for this purpose.

The irradiations were performed on standard Vth nMOSFETs, performed at the Physics and Astronomy Department of the University of Padova (Italy) with an X-ray source. The dose rate in SiO2 was about 8.3 Mrad/h. During irradiation, the NMOS devices were kept under standard 'maximum-stress'conditions (Vgs = Vds = 0.9V) and at room temperature. The chip was mounted on a semi-automatic probe station and contacted with a custom probe card with 32 probes. A Keithley 707 switching matrix connected the semiconductor device analyzer (HP4156) and the bias supply.

Standard Id vs Vgs and Id vs Vds characteristic curves were measured in steps up to a total dose of 1.05 Grad; electrical parameters like threshold voltage shift, sub-threshold slope, leakage current and saturation current were extracted.

The threshold voltage was extracted with the maximum transconductance method in linear region (Vds = 0.1V). The Vth shift trend depends on the transistor geometry and was found to be limited for wide transistors (monotonic decrease up to ΔVth = -40mV in the worst case) and more pronounced for narrow transistors. For the narrowest channel transistor (W=100nm, L=1μm), Vth shows a monotonic decrease up to ΔVth = -95mV at 250 Mrad, and then started to increase again up to 1 Grad. The calculated sub-threshold slope shows a similar trend: a limited increase, more pronounced for the narrow transistors (Δss = +16mV/dec in linear region and Δss = +22mV/dec in saturation).

No decrease in the saturation current is observed; instead a very pronounced increase of the leakage current has been measured for all transistors (up to 3-4 orders of magnitude). The observed leakage current is independent on W, as expected, since it comes from lateral parasitic transistors.

These results show that a state of the art High-K metal gate technology does not introduce unexpected bad behaviors when irradiated to HL-LHC levels and that therefore HEP designers may be able to use the use it

and profit from the intrinsic low-power advantages which are accompanying this technology.
An irradiation campaign on pMOSFETs is currently undergoing and results will be reported later

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