Contribution ID: **17** Type: **Oral**

Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Tuesday 27 September 2016 15:15 (25 minutes)

The high-luminosity phase of the Large Hadron Collider will provide 5-7 times greater luminosities than assumed in the original detector design. An improved trigger system requires an upgrade of the readout electronics of the ATLAS Liquid Argon Calorimeter. Concepts for the future readout of the 182,500 calorimeter channels at 40-80 MHz and 16bit dynamic range, and the development of low-noise, low-power and high-bandwidth electronic components will be presentet, including ASIC developments towards radiation-tolerant low-noise pre-amplifiers, up to 14bit ADCs and low-power optical links with up to 10GB/s.

Summary

The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities of up to $7x10^{34}cm^{-2}s^{-1}$ corresponding to a signal pile-up from up to 200 events per proton bunch-crossing, with the goal of accumulating a total integrated luminosity of $3000fb^{-1}$. To be able to retain interesting physics events even at rather low transverse energy scales, increased trigger rates are foreseen for the ATLAS detector. At the hardware selection stage acceptance rates of 1MHz are planned, combined with longer latencies up to 60 $/mus$ in order to read out the necessary data from all detector channels. Under these conditions, the current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. Furthermore, the expected total radiation doses of $10^{13}neq/cm^2$ (NIEL) and 0.3kGy (TID) are beyond the qualification range of the current front-end electronics.
For these reasons a replacement of the LAr front-end and back-end readout system is foreseen for all 182,500 readout channels, with the exception of the cold pre-amplifier and summing devices of the hadronic LAr Calorimeter. The new low-power electronics must be able to capture the triangular detector pulses of about 400-600ns length with signal currents up to 10mA and a dynamic range of 16bit.
In 180nm SiGe technology (IBM 7WL) and choosing unipolar shaping, two gain stages can cover the desired dynamic range. An ADC matching this pre-amplifier and shaper will need to provide 14bit digitization range. Such a design is shown to meet the noise requirements and achieve an integral non-linearity below 0.1%. Moreover, in simulations of the complete readout chain using the unipolar shaping approach signal pile-up is introducing a controllable baseline shift, and an additional digital CR shaping stage does not introduce a degradation of the energy resolution.
Alternatively, a development of pre-amplifier and shaper as well as SAR ADCs is performed in 65nm CMOS technology. Due to the lower voltage range, 2-gain and 4-gain designs of the analog part are studied with programmable peaking time to optimize the noise level in presence of signal pile-up. The 65nm ADC uses a SAR architecture and an active SEE detection mechanism by feeding the signals into two ADCs in parallel and comparing their output. In this way, the signal-to-noise ration can be further improved in presence of radiation. Results for an 80MHz 12bit prototype design show ENOB values above 10.8bits after 10kGy irradiation, and similar performance is reached for a 14bit layout.
Furthermore, results for a newly designed VCSEL array driver show that the required 10Gb/s transfer rate at 20-35mW per channel is achieved, suitable for integration into a low-power optical link package.

Results from performance-simulation of the calorimeter readout system for the different options and results from design studies and first tests of the ASIC components will be presented.

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Session Classification: Systems, Planning, installation, commissioning and running experience

Track Classification: Systems