



Contribution ID: 25

Type: Oral

The ATLAS Level-1 Topological Trigger Design and Operation in Run-2

Thursday 29 September 2016 09:50 (25 minutes)

The ATLAS Level-1 Trigger system performs event selection using data from calorimeters and the muon spectrometer to reduce the LHC collision event rate down to about 100 kHz. Trigger decisions from the different systems are combined in the Central Trigger Processor for the final Level-1 decision. A new FPGAs-based AdvancedTCA sub-system was introduced to calculate in real time complex kinematic observables: the Topological Processor System. It was installed during the shutdown and commissioning started in 2015 and continued during 2016. The design and operation of the Level-1 Topological Trigger in Run-2 will be illustrated.

Summary

Due to the increase of the LHC instantaneous luminosity and collision energy, the ATLAS trigger system in Run-2 needs to cope with five times higher event rates than in Run-1. Several upgrades were performed during the Long Shutdown 1 to improve the ATLAS trigger capability. In particular, a new Level-1 Topological (L1Topo) trigger system was designed and installed. It selects events based on topological event kinematics calculations like invariant masses between objects, minimum distance between objects, etc.

The L1Topo trigger system is a single processor shelf equipped with two processor modules and is part of the ATLAS Level-1 (L1) trigger system. The processor modules are identical copies with firmware adapted to run different topological algorithms. These modules are designed in AdvancedTCA form factor.

The L1Topo system receives optically and through the backplane real-time data from the L1 calorimeter and L1 muon systems. The optical signals are converted to electrical signals in 12-fibre receivers. Due to its big density Avago miniPOD receivers are used. The electrical high-speed signals are routed into two FPGAs, equipped with on-chip Multi-Gigabit Transceivers (MGT). The data is de-serialized in the MGT receivers and parallel data enters the FPGA fabric. No data duplication is implemented at the PCB level. The two processors can communicate via their fabric interface to get access to data that cannot be received directly via the MGT links. Even though higher data rates are technically possible, a maximum bit rate for the inter-FPGA link of 1Gb/s per differential pair is anticipated. This limits parallel connectivity to 238 Gb/s of aggregate bandwidth. The L1Topo input data consist of Trigger Objects (TOB) corresponding to jets, electromagnetic clusters, taus or muons. The TOBs information include the position of the object along with some qualifying information like its energy. Thanks to the large amount of logic resources in the FPGAs, more than 100 algorithms are executed using real-time data. The results of the algorithms are sent on both optical fibres and electrical cables to the Central Trigger processor (CTP), which is responsible of the final ATLAS L1 decision. The output to the CTP consists of individual bits indicating the decision of each of the topological algorithms. In addition, L1Topo provides through the data path the TOBs input received in addition to the decision per algorithm.

The commissioning of the L1Topo system started in 2015 and continues in 2016. Data triggered or rejected by the L1Topo system is analysed comparing the hardware decisions with the simulated ones using the appropriate L1 trigger objects that are saved in the data along with the trigger decisions and the rest of the event. An initial set of data triggered by the L1Topo system and used for the commissioning was taken during the heavy-ion run in 2015. The commissioning continues in 2016 during cosmics and proton-proton collisions data-taking. This talk gives an overview of the design, operation and commissioning status results.

Presenter: IGONKINA, Olga (Nikhef National institute for subatomic physics (NL))

Session Classification: Systems, Planning, installation, commissioning and running experience

Track Classification: Systems