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On-detector electronics for the LHCb VELO upgrade

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the VeloPix ASIC with on-chip zero-suppression. This paper will present the systems overview and design of the VELO on-detector electronics, including the front-end hybrid, the opto-conversion and power distribution boards. Results will be shown from the evaluation of these prototypes of these boards.

Summary

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The event selection will be performed by high-level software algorithms implemented in a CPU farm. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC, which is part of the Medipix/Timepix family. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the whole VELO.

This paper will present the architecture and the design of the VELO on-detector electronics, and describe how it interfaces to the front-end ASIC and the LHCb readout system. Its two main components are the opto- and power board (OPB) and the front-end hybrid. The OPB is situated immediately outside the VELO vacuum tank and performs the opto-electrical conversion of control signals going to the front-end and of serial data going off-detector. Moreover, it performs the DC/DC conversion of supply voltages and provides the local control of the front-end. The board is designed around the Versatile Link components developed for high-luminosity LHC applications. The front-end hybrid hosts the VeloPix ASIC and also a GBTx ASIC that provides the control signals for the VeloPix. The hybrid and OPB are linked by 60 cm long electrical data and control links running at 5 Gbit/s.

This system is an example of a full implementation of a front-end readout and control system for an LHC detector, based on the radiation tolerant opto-modules, DC/DC converters and the GBT chipset developed for the LHC upgrades. Prototypes for all components of the system have been produced and tested, the results from these tests and the experience gained from designing and operating the system will be presented.

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