Contribution ID: **95** Type: **Oral**

Data Acquisition System for the CALICE AHCAL Calorimeter

Wednesday 28 September 2016 10:15 (25 minutes)

The data acquisition system (DAQ) for a highly granular analogue hadron calorimeter (AHCAL) for the future International Linear Collider (ILC) will be presented. The developed DAQ chain has several stages of aggregation and scales up to 8 million channels foreseen for the AHCAL detector design. The largest aggregation device, LDA (Link data aggregator), has 96 HDMI connectors, four Kintex7 FPGAs and a central Zynq SoC (System-On-Chip). Architecture and performance results will be shown in detail. Experience from CERN testbeams with a small detector prototype consisting of 15 detector layers will be reported.

Summary

The CALICE (CALorimeter for Linear Collider Experiment) collaboration is developing highly granular calorimeters, which are needed for particle flow reconstruction. AHCAL (Analog Hadron CALorimeter) group is developing a steel sandwich calorimeter option, which uses individually read out 3x3x0.3 cm3 scintillator tiles with SiPMs (Silicon PhotoMultipliers). This corresponds to 4 millions channels just in the HCAL barrel. The front-end electronics is embedded in the detector layers in between the absorber plates without active cooling. Given the ILC (International Linear Collider) beam structure (<1 ms of collisions followed by 199 ms readout), the electronics use a power pulsing scheme which cuts the power consumption down to <2%.

The DAQ was developed from scratch to adopt the ILC timing. It is organized in a cascade of components: 1) the SPIROC ASIC, which reads out 36 channels, stores up to 16 events in analog memory cells and digitizes the stored information; 2) the DIF (Detector InterFace), which reads out 72 ASICs from one detector layer; 3) the LDA (Link Data Aggregator), which reads out up to 96 DIFs and sends the data out over Gigabit Ethernet; 4) the CCC (Clock and Control Card), which controls all 16 LDAs in the barrel. Given the ILC scenario duty cycle, the bandwidth of the LDA does not exceed 85 MB/s, even with 100% hit occupancy. Taking into account the auto-trigger nature of the ASIC, which records and sends data only from actual physics hits, the data rate during physics data taking is expected to be lower.

The recently developed aggregation device, the Wing-LDA, contains 4 Kintex7 Xilinx FPGAs and a Zynq SoC (System-on-Chip). The processor part is running Linux and the data is transferred using a DMA (Direct Memory Access) between FPGA and Linux memory, from where it is streamed to Gigabit Ethernet using the TCP protocol. The link between the LDA and individual detector layers is based on HDMI physical connectors and cables with 10MBit/s serial protocol. The links between FPGAs are based on dual 400 Mbit/s serial lines implemented in user logic, encoded in 8b10b and secured by a CRC16 packet checksum with retransmission in case of an error.

The DAQ was tested in beam for the first time in the configuration which is foreseen for the ILC in terms of DAQ hierarchy. It has been tested several times with up to 15 detector layers instrumented with up to about 4000 channels in total. Main tests were done in 2014 and 2015 in test beams at CERN and DESY, where it was operated in a sparse continuous beam (in contrast to the ILC beam structure). The continuous beam then requires to read out and restart as fast as possible. The DAQ finally achieved ˜17 readout cycles per second in the beam tests. When recent speed improvements are taken into account, the extrapolated DAQ performance already fulfills the requirements of the fully instrumented AHCAL barrel operated in the ILC mode, even with 100% hit occupancy.

Author: KVASNICKA, Jiri (Acad. of Sciences of the Czech Rep. (CZ))

Presenter: KVASNICKA, Jiri (Acad. of Sciences of the Czech Rep. (CZ))

Session Classification: Systems, Planning, installation, commissioning and running experience

Track Classification: Systems