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GBT based readout in the CBM experiment

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The CBM experiment at FAIR will use GBTX and Versatile link based readout systems for several subdetectors.

Particularly challenging is the readout of the silicon tracking system (STS) which requires features like a minimal number of frontend connections, AC coupling and time deterministic messages.

The paper gives a detailed description of the readout concept for the STS, emphasizing the common features with the GBT based readout in other CBM detectors.
A CBM common readout board with 3 GBTX is presented which provides the full GBT functionality for all systems and can be interfaced to various prototype readout chains.

Summary

The CBM experiment at FAIR is a fixed target heavy ion experiment planned to operate at high interaction rates up to 1e7/s and using self-triggering frontend electronics. The silicon tracking system (STS) is the main tracking detector in CBM, consisting of 8 stations of silicon strip sensors located inside a 1T dipole magnet.

The GBTX transceiver ASIC and VersatileLink optical modules were chosen to implement a data aggregation stage between the STS-XYTER frontend ASICs connected to the strip sensors via low mass cables and the data processing boards (DPBs), a common FPGA-based layer. Readout boards (ROB) with the GBT and Versatile Link devices are located inside the magnet close to the active sensor area.

Based on the specific conditions in the STS setup and the GBTX features, the readout concept for the STS was developed:
The frontend board (FEB) carries 8 STS-XYTER2 ASICs which implement an E-Link interface.
Up to 5 FEBs connect to one of the ROBs, which are stacked in the limited space at the sides of the STS box. Each FEB operates at the bias potential of the connected sensor. Consequently the E-Link interfaces are AC coupled.

A single GBT clock and a single downlink per FEB are used for ASIC configuration, control and time synchronization. A configurable number of 1 to 5 uplinks per STS-XYTER depending on the local data rate is used for data readout and for control responses.

The ROB for STS will implement 3 GBTX together with 1 VTRx and 1 VTTx module.
The resulting 42 readout E-Links at 320 Mbps in widebus mode can be matched efficiently with 8,16 or 40 readout links per FEB. The backend interface of the GBTX communication is implemented in the DPB layer which resides outside the experimental cavern. The DPB also includes the backend of the specifically developed STS-XYTER readout protocol and the interfaces to data acquisition, detector control and the timing system.

Similar readout concepts were devised for other CBM detectors with frontend systems based on custom ASICs, namely the muon detector (MUCH) which uses the same XYTER as frontend ASIC, the TRD and the TOF detectors. This will allow for shared developments and partial reuse of hardware, firmware and protocols.

A common CBM readout board (C-ROB) is being developed that implements the full GBT and Versatile Link functionality needed by all systems. The C-ROB serves to setup prototype readout chains and provides sufficient data aggregation to readout moderately sized detector assemblies in laboratory and beam tests. The required subset of E-Links, clocks and SCA functionality is connected to 2 FMC connectors. Prototype readout chains of the various frontend systems can be interfaced via individual mezzanine cards.

For the final CBM readout chains, systems will adapt the C-ROB in order to fulfill specific needs such as smaller ROB dimensions and efficient cooling for the STS, a single GBTX ROB for TOF, or duplicated GBTX/VTTX blocks for the TRD readout.

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