
BROOKHAVEN NATIONAL LABORATORY

# The Trigger Readout Electronics for the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeters

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**Brookhaven National Laboratory**

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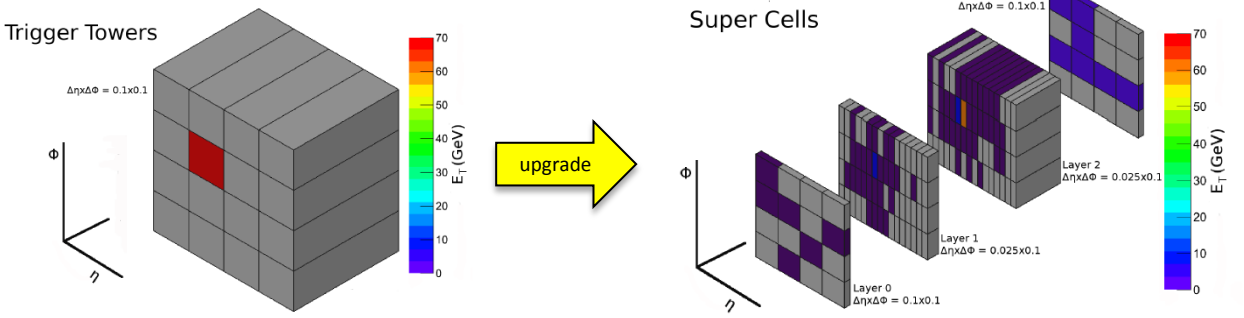
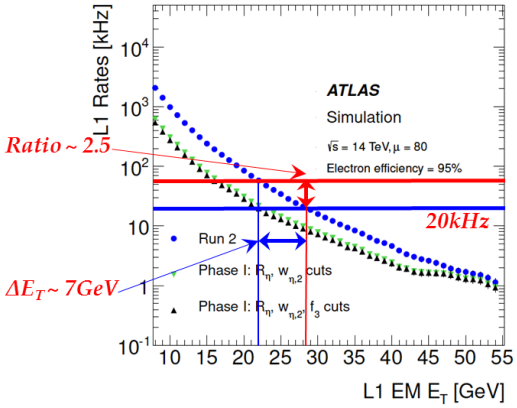
# Outline

- Introduction to LAr Phase-I Upgrade
- The LAr Phase-I Demonstrator
- Phase-I Front-End Electronics
- Phase-I Back-End Electronics
- Summary

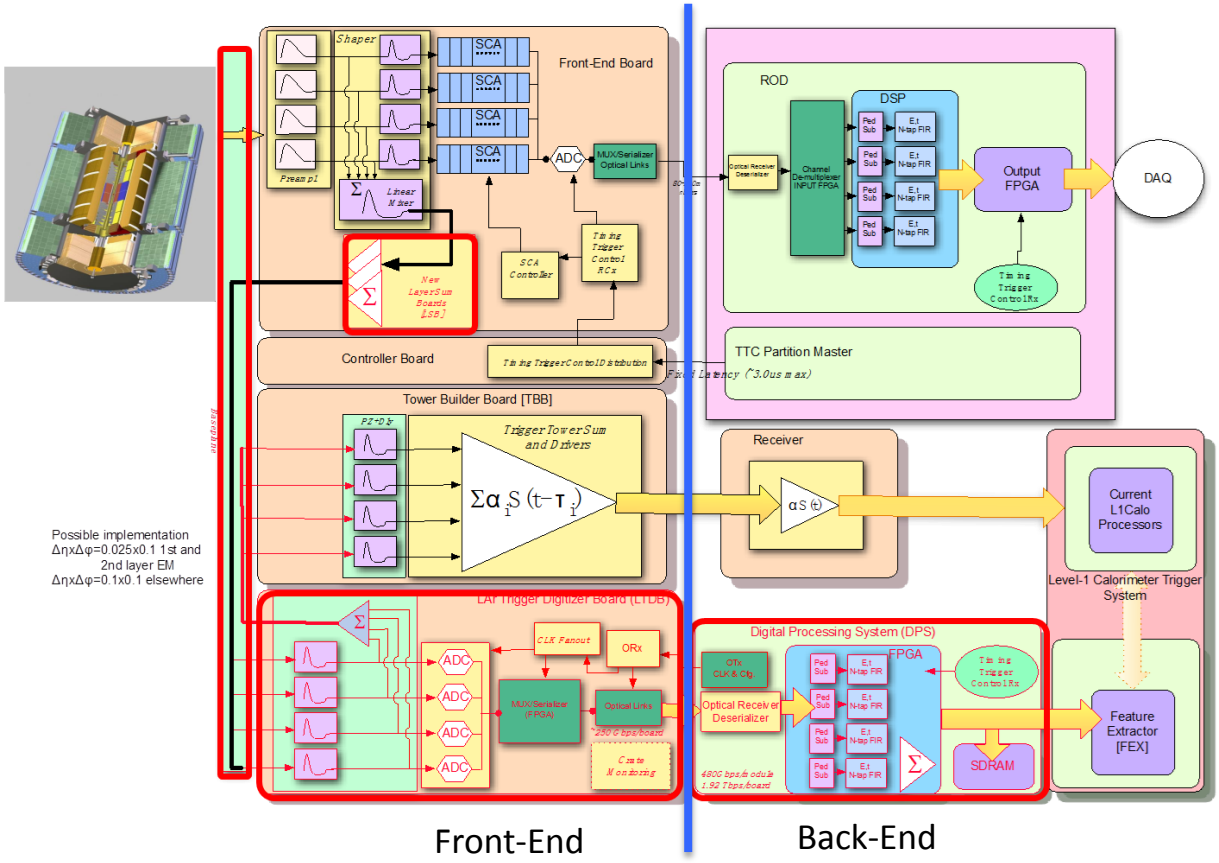
# Introduction



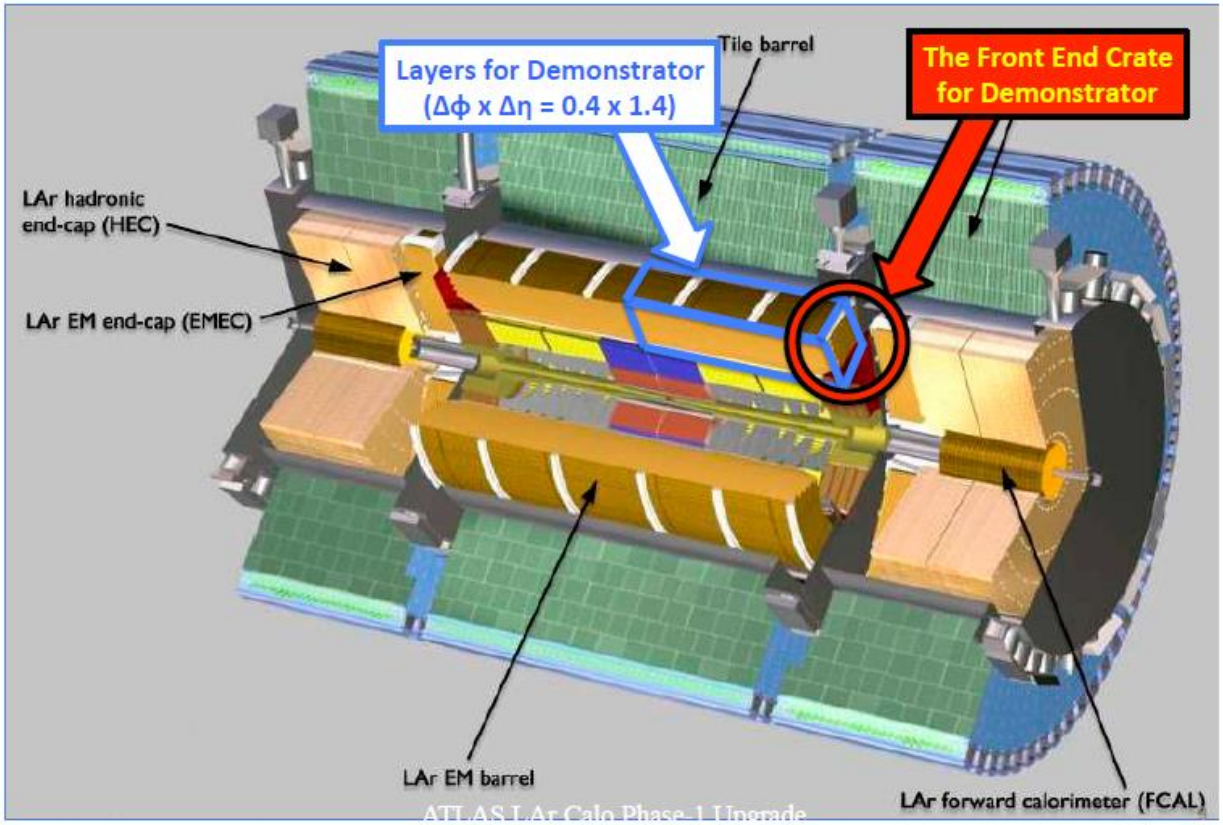

- As LAr Phase-I upgrade, new calorimeter trigger electronic with finer granularity and improved precision will be introduced for Level-1 trigger.
  - Trigger Towers are replaced by Super Cells, thereby increasing the granularity by a factor of 10 at the trigger processor inputs.
  - Signal processing and energy reconstruction algorithms
  - Offline identification algorithms in Level-1 hardware (FPGA based)

# The LAr Phase-I Upgrade: 2018.12-2021.2




- New elements are highlighted in RED boxes
- The legacy analog trigger readout path will be kept

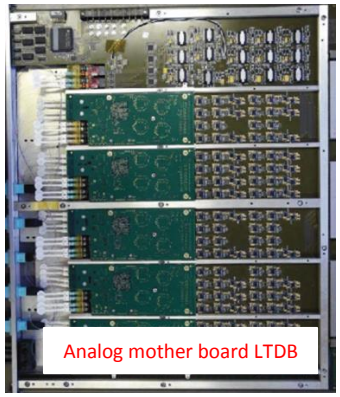
# The LAr Phase-I Demonstrator




- The demonstrator system, in which about 1/60 of the full new trigger readout is realized, was installed on the ATLAS detector in summer 2014.
  - part of the calorimeter covered: $1.767 < \varphi < 2.160$, $0 < \eta < 1.4$

# LAr Demonstrator FE

- New Baseplane has been tested at CERN
- Two LTDB versions have been developed with the digital part or analog part on the mother boards.
- Similar total noise levels for trigger, and comparable cross-talk across trigger towers. No impact on analog trigger and standard readout





**Baseplane**

**installation of front end electronics**

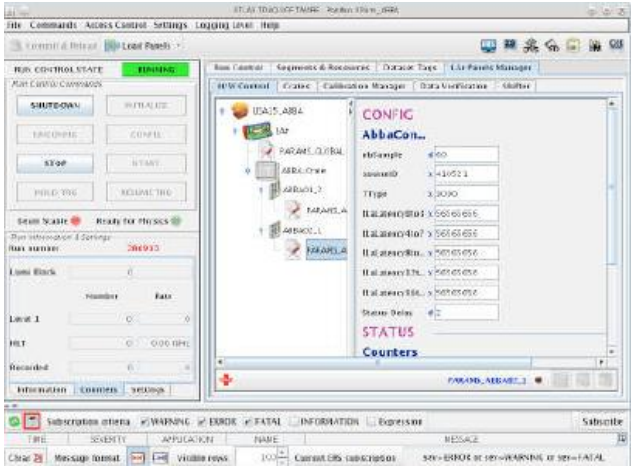
# LAr Demonstrator BE

## ABBA: ATCA test Boards for Baseline Acquisition

- Prototype of LAr Digital Processing System.
- ATCA with 10GbE switch
- 3 Altera Stratix IV FPGAs
- 40 Fibers runs at 5.12Gbps, total 208.4Gbps per board
- Readout path with IPbus:
  - ABBA->ATCA backplane (Zone-2) -> Switch blade -> PC

ABBA

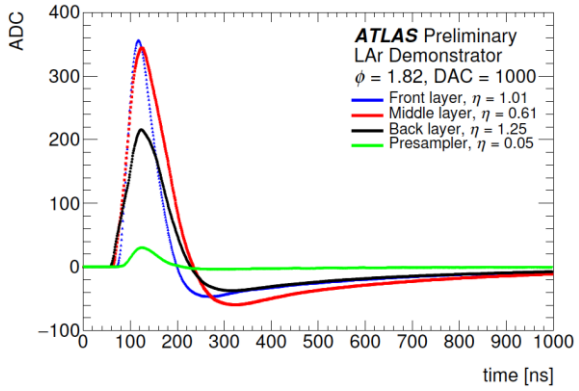
Back-end electronics Crate



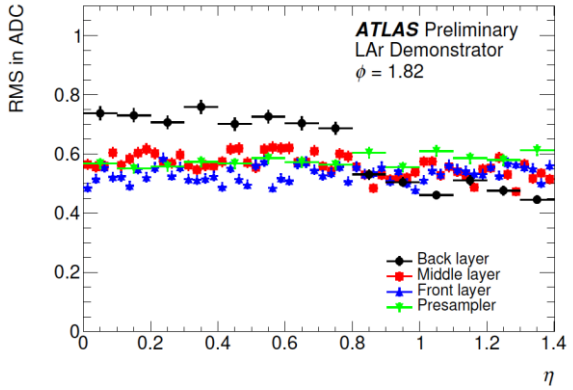

ABBA software GUI

# First Results from LAr Demonstrator

- Successful data taking in 2015 pp and HI runs.
- Restarted collecting pp data with start of LHC on May 19th, 2016.
- These data are used to understand effect of pileups and to develop new filtering algorithm.




**Super Cell pulse shapes for each layer**



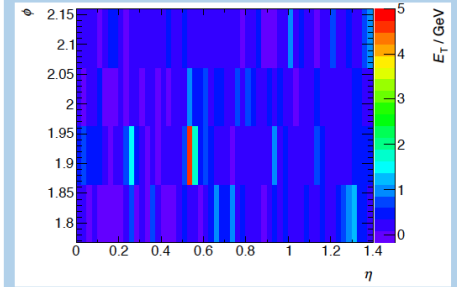

**Noise level of Super Cells in ADC counts**

## Energy distribution in middle layer in ABBA run 287232

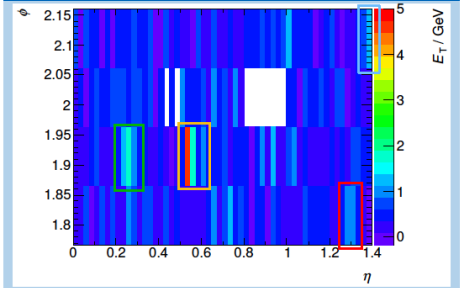
- Reconstructed objects in demonstrator region in corresponding ATLAS event:

| type | $p_T$/GeV | $\eta$ | $\phi$ |
|---|---|---|---|
| $e^-$ | 11.0 | 0.55 | 1.95 |
| $e^-$ | 5.6 | 1.39 | 2.14 |
| $e^+$ | 6.7 | 1.32 | 1.82 |
| $e^-$ | 3.2 | 0.68 | 1.79 |
| $\gamma$ | 6.3 | 0.27 | 1.89 |
| $\gamma$ | 4.8 | 1.32 | 1.82 |

ATLAS main readout (run 287224)




ABBA readout (run 287232)

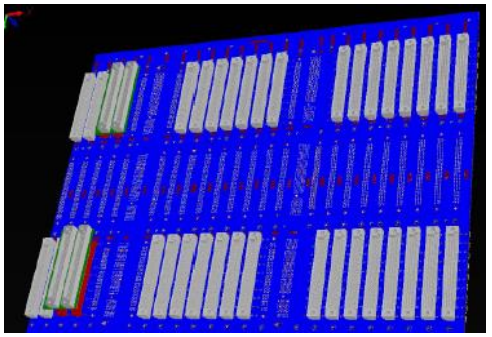



$\Rightarrow$ good agreement for ATLAS main and ABBA readout

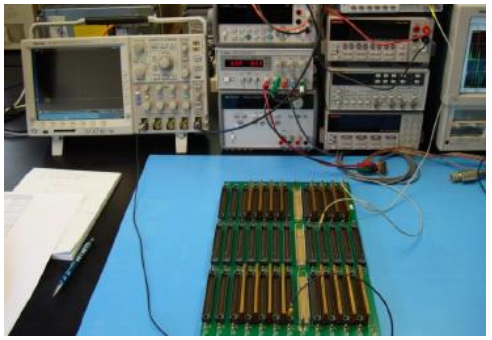
LAr Demonstrator data taking during heavy ion collisions with trigger type 0x90 in 2015 (Robert Wolff, 19/4/2016) 6

# Phase-I: Front-End Electronics

- Key components of FEE
  - New Layer Sum Boards (LSB)
  - New Baseplanes
  - LAr Trigger Digitizer Boards (LTDB)
    - Radiation-tolerant custom ASICs are designed for the Phase-I upgrade
    - Nevis ADC
    - LOCx2
    - LOCld



EMEC special baseplane

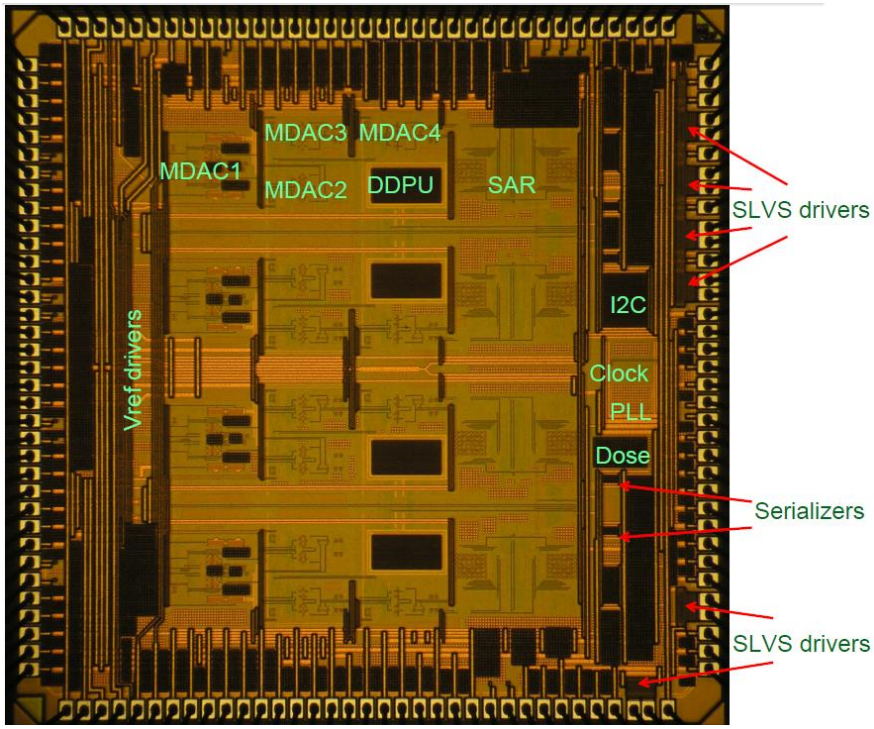


HEC baseplane test stand

# FE LTDB ASIC –ADC

## Quad 12-bit hybrid pipeline SAR ADC

- Sampling information derived from the rising edge of differential input SLVS 40MHz clock
- Data sent out serially using 320MHz DDR SLVS clock signaling
- I2C interface (1.2V signaling) allows to control all internal functions of the chip
- Power dissipation of ~43mW/channel
- Radiation tolerant
- Die:
  - 3.6mm x 3.6mm
  - 72 pin QFN
- Final prototype produced and tested on 64-ch LTDB prototype

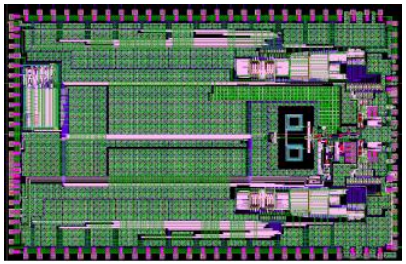



Layout of ADC

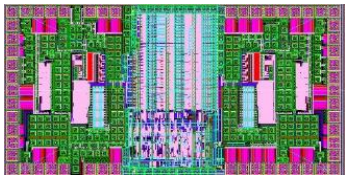
# FE LTDB ASIC – LOCx2

On LTDB, the optical link on the transmitter side consists of a transmitter ASIC LOCx2 and a custom optical transmitter module MTx.

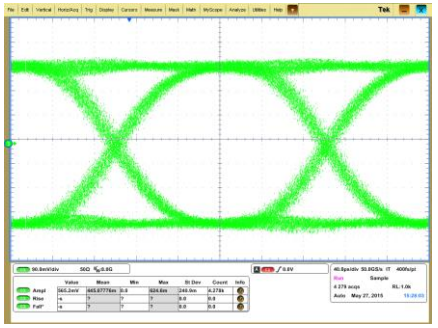
- LOCx2
  - Dual 8*14 bits channel 5.12Gbps serializer
  - Nevis ADC compatible
  - Radiation tolerant
  - Die:
    - 6.036mm x 3.68mm
    - 100pin QFN
- LOCld
  - Dual channel VCSEL driver
  - Radiation tolerant
  - Die:
    - 2.114mm x 1.090mm
    - 40pin QFN
- Early prototype has been tested on 64-ch LTDB prototype, final prototype is being tested.



Layout of the LOCx2 ASIC



Layout of the LOCld



The eye diagram of
LOCx2 output at 5.12Gbps

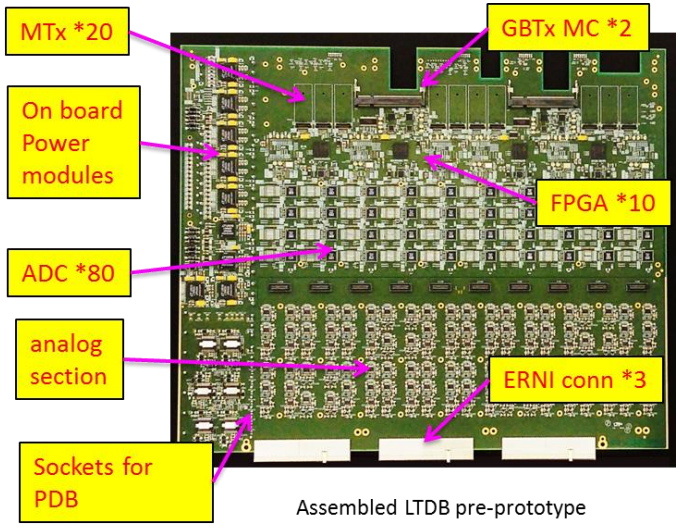
# FE LTDB Development

The final board design has to be developed while finalizing ASICs. Therefore, we're developing following three boards:

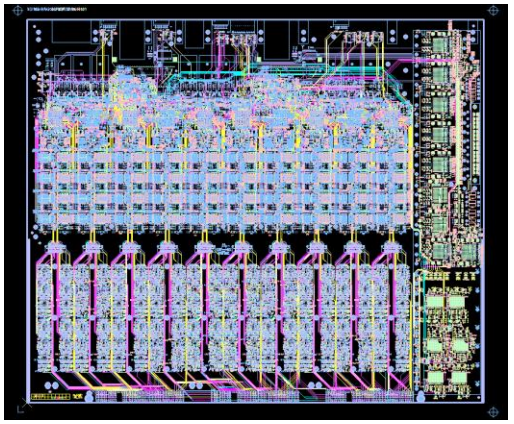
- **LTDB pre-prototype**
  - Commercial FPGAs, radiation-tolerant custom ASIC: Nevis ADCs, optical transmitter MTx and GBTx
- **64-ch LTDB prototype**
  - Radiation-tolerant custom ASICs: Nevis ADCs, MTRx, MTx, GBTx and GBT-SCA.
- **Full LTDB prototype**
  - Radiation-tolerant custom ASICs: Nevis ADCs, MTRx, MTx, GBTx and GBT-SCA.

# FE LTDB Pre-Prototype

- Understand integration and large board manufacturing : GBTx, Nevis ADC, LOCld, MTx, Serialization on FPGA
- Pre-selection irradiation testing for the analog COTS components has been done
- 10 Artix-7 FPGAs, 80 custom 12-bit ADCs, 20 custom MTx devices for data processing, and 2 GBTx for clock distribution, control and monitoring
- Analog and digital part are designed by different institutes and merged Gerber together.

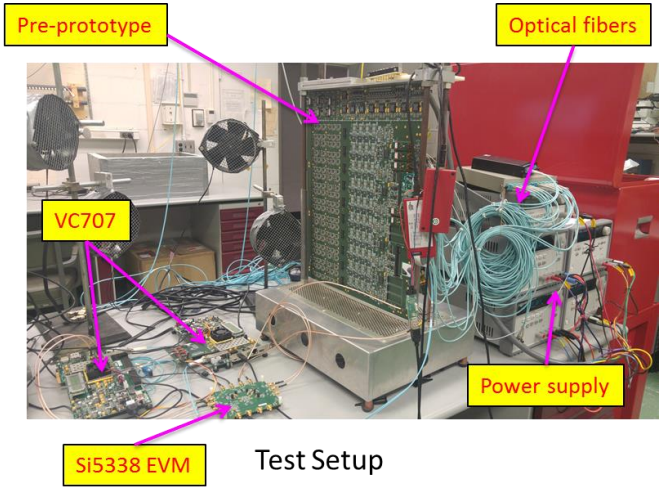


Assembled LTDB pre-prototype

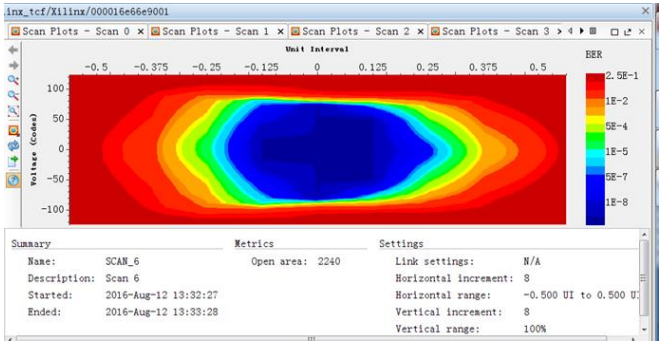

Layout of LTDB pre-prototype

# FE LTDB Pre-Prototype Tests

- Evaluation tests of digital section have been done and results show the digital section and on board power supply work properly
- Clock distribution and Slow control link over GBTx-MC work properly
- Link speed test
  - IBERT with MTx : good eye opening and BER (< $10^{-15}$) at 4.8 Gbps have been achieved on all link speed tests



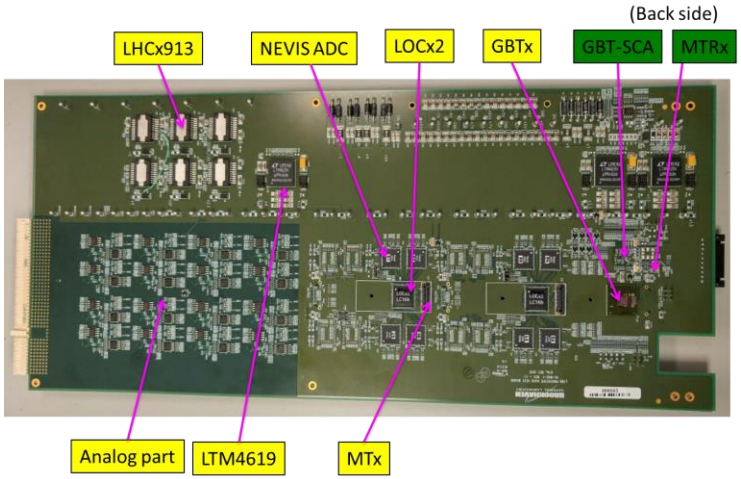

Test Setup




Link BER test

# FE 64-ch LTDB Prototype

- A 64-ch LTDB prototype test board has been developed.
  - Similar to LTDB prototype, but less channels.
- The digital section is 1/5 LTDB prototype digital section.
  - It's the first integration test of final components currently planned to be used on LTDB prototype design
  - It serves as the LOCx2 and Nevis ADC integration test platform before the final design review
- The analog circuit uses modified circuit on LTDB demonstrator.

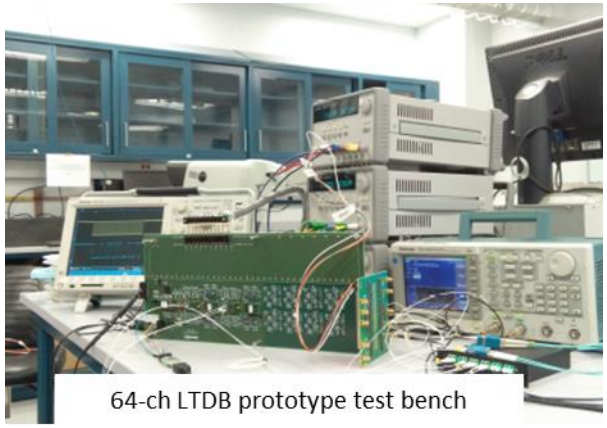



Assembled 64-ch LTDB prototype

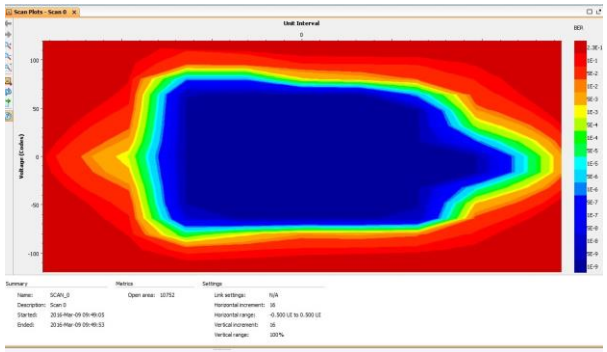
Layout of 64-ch LTDB prototype

# FE 64-ch LTDB Prototype Tests

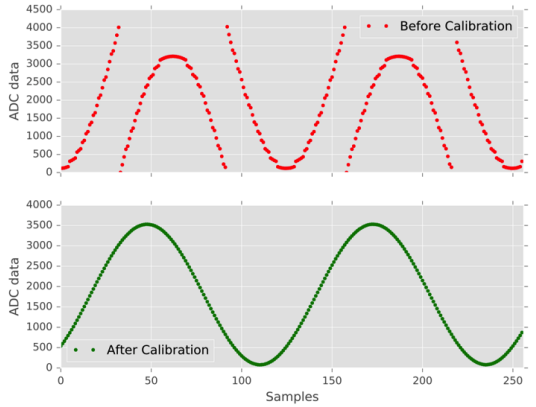
- Tests have been done in Lab
- Link speed tests
  - Good eye opening and BER (< $10^{-14}$) at 5.12Gbps have been achieved on all link speed tests
- Pedestal/noise measurement: RMS < 1 ADC count
- All 48 channels have been tested with pulse injection
- Crosstalk measurement: xtalk < 0.1%
- Non-linearity ~ 0.12%



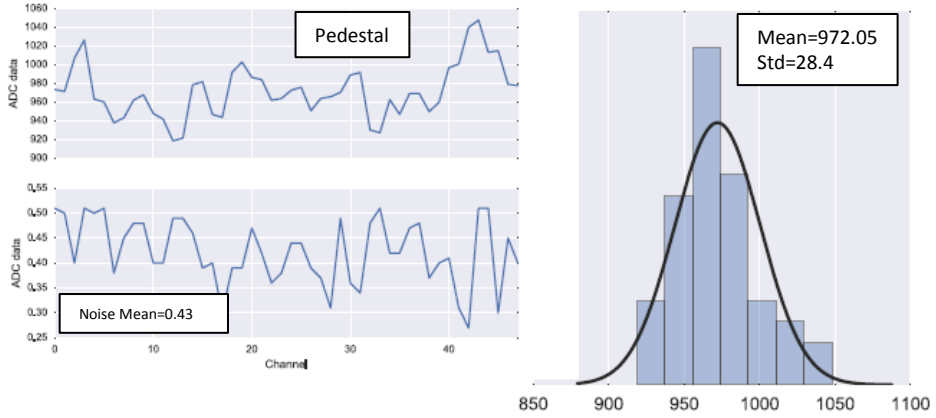
64-ch LTDB prototype test bench



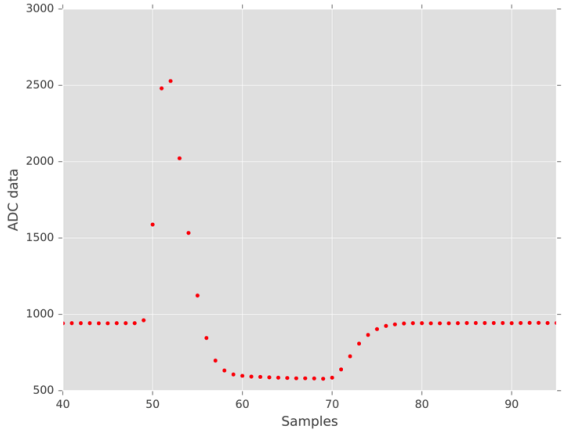
# ADC Calibration/PED/Saturation



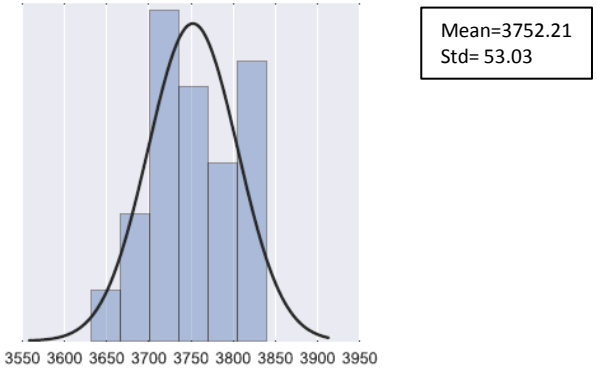

Calibration test with sine waveform




Pedestal and noise of 48 Nevis15 ADC channels

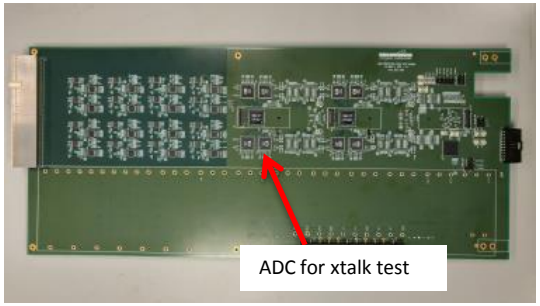


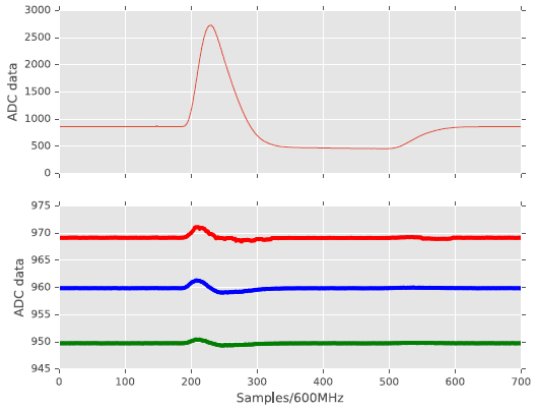

Calibration test with LAr pulse

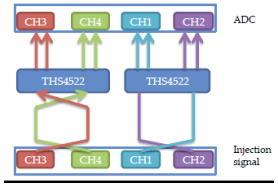



48 channels of Nevis15 ADC have been tested, saturation values are from 3632 to 3689

# Crosstalk and Non-Linearity



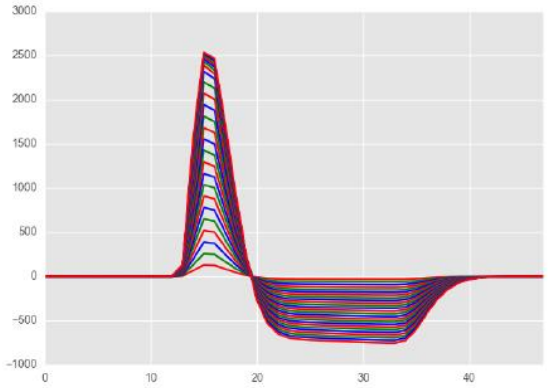



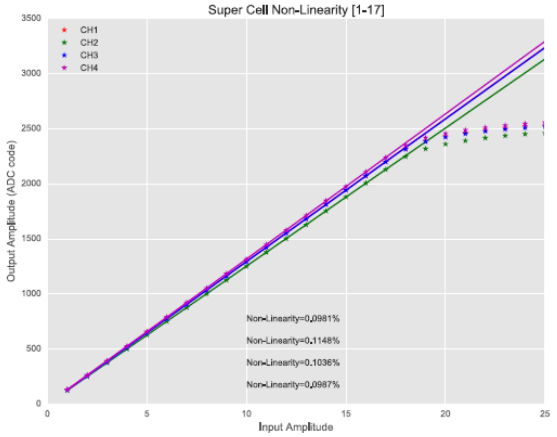




Signal path

| CH1 | CH2 | CH3 | CH4 |
|---|---|---|---|
| - | 0.113% | 0.041% | 0.080% |
| 0.117% | - | 0.041% | 0.042% |
| 0.045% | 0.046% | - | 0.095% |
| 0.092% | 0.045% | 0.095% | - |

Each row is the result when injecting signal to one ADC channel

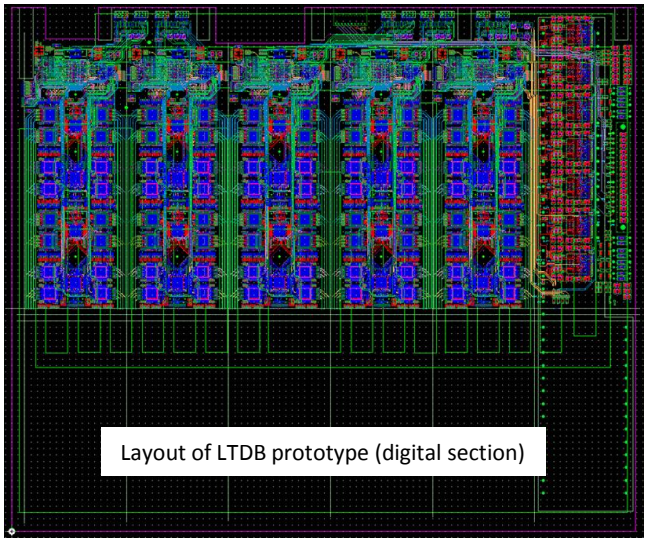




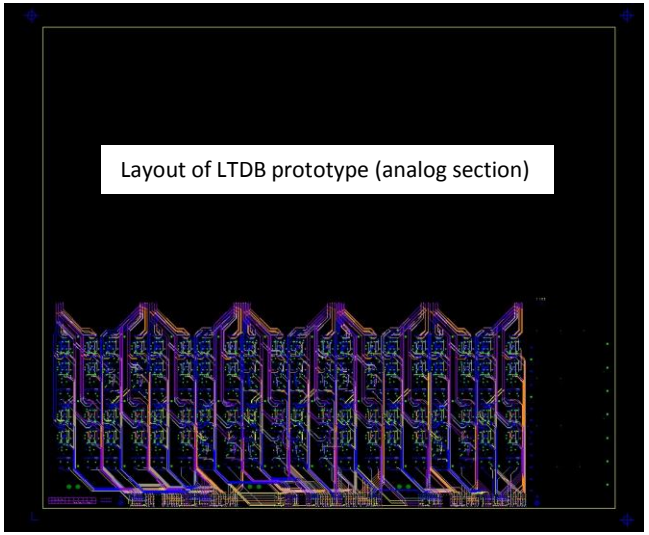

Non-linearity is better than 0.12%, for a range of around 2200 ADC count
Gain difference for these 4 channels: ~5%
For large input signal, the injection board output is already saturated, obvious distortion is seen.

# FE LTDB Prototype

- 20 LOCx2 + 80 Nevis ADCs + 20 MTx for 320 Super Cell signals processing
- 5 GBTx/GBT-SCA/MTRx for timing and slow control
- Reuse 64-ch LTDB prototype digital design, plus analog design on LTDB pre-prototype
- A power distribution board PDB-LTM will supply power. It is realized on a mezzanine
- Analog section and digital section are designed by different institutes, and Gerber merged for fabrication
- Expected December of 2016



Layout of LTDB prototype (digital section)



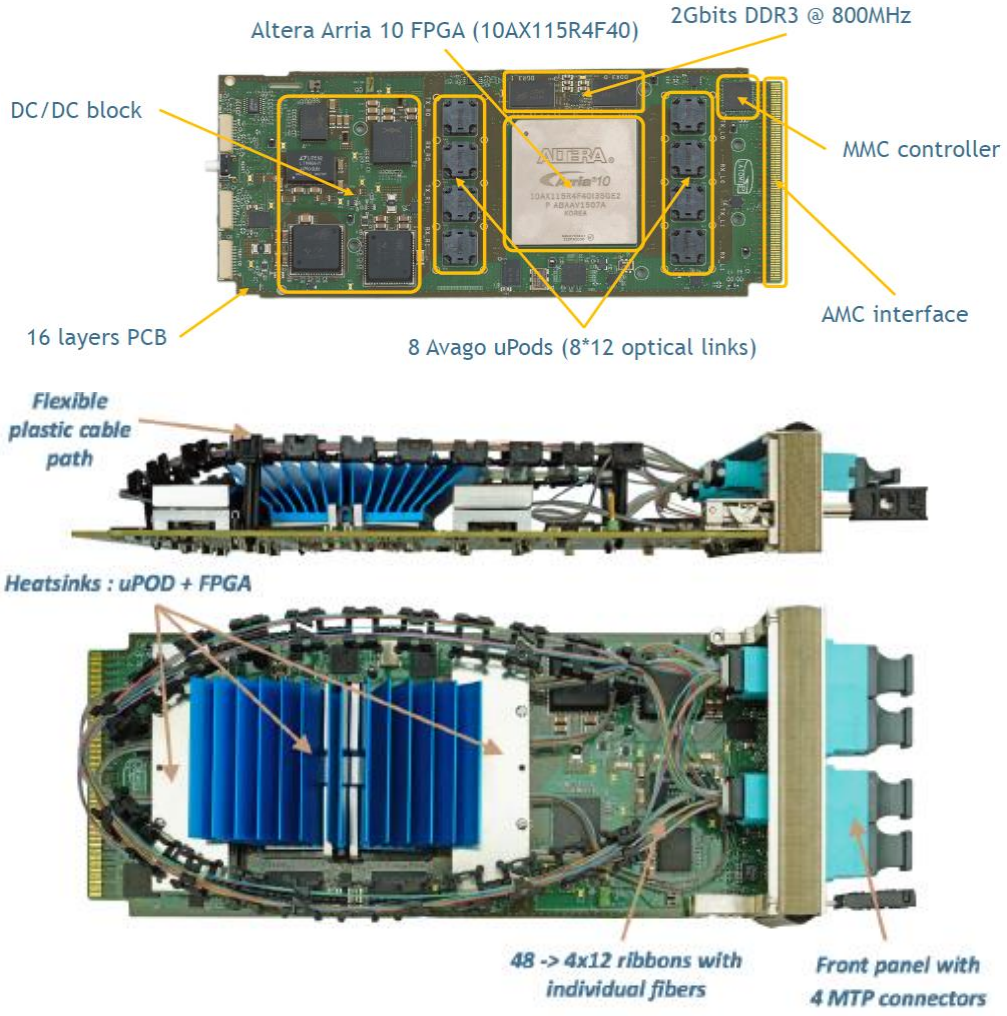
Layout of LTDB prototype (analog section)

# Phase-I BE: LDPS

LDPS (LAr Digital Processing System) receives 12 bits ADC data from the LTDBs @ 5.12 Gbps/fiber, extract the transverse energy for each Super Cell every 25 ns, and transmit these data to the Level-1 calorimeter trigger system (L1Calo) @ 9.6/11.2/12.8 Gbps

LATOME: LAr Trigger prOcessing MEzzanine

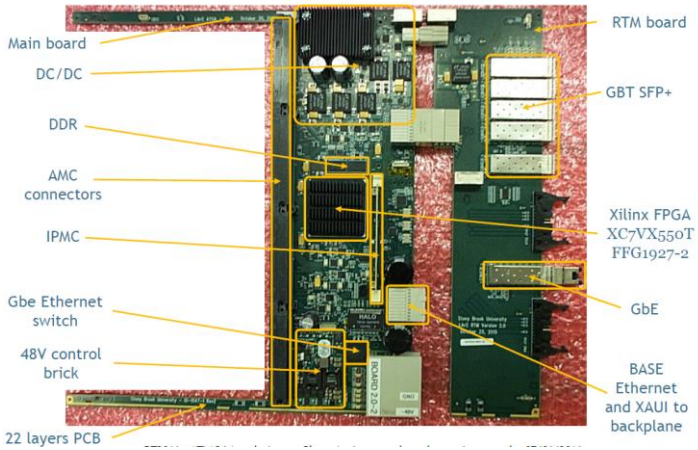
- AMC mezzanine card with ARRIA-10 FPGA
- 3 pre-prototype boards have been produced
- Fully tests have been carried out and working as expected
  - Power, GbE, XAUI, GBT, TTC, 10GbE, JTAG, flash, DDR3, I2C, MMC etc.
- Various optical link speeds (6.4, 9.6, 11.2, 12.5 and 12.8 Gbps)

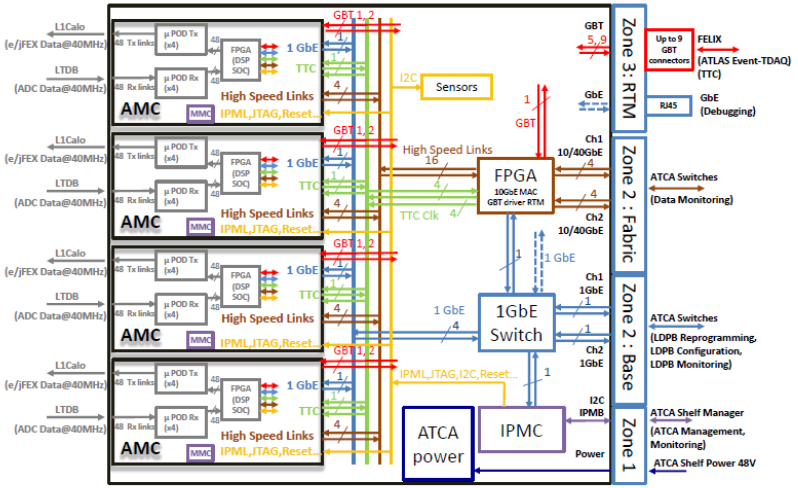


# Phase-I BE : LDPS

LArC: LAr Carrier

- Each carrier board holds four AMCs, a RTM and provides a variety of different communication functionalities as shown in the schematic diagram.
- Achieving a reliable high rate of transmission for clock distribution and data rates at 10/40 GbE is a challenge on large ATCA boards
- Integration tests with LATOME have been successfully done
- LArC V2 tested and working well

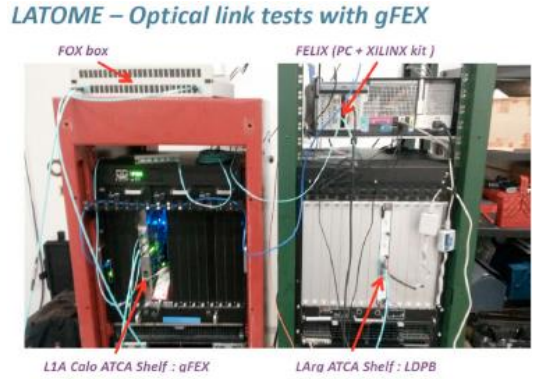


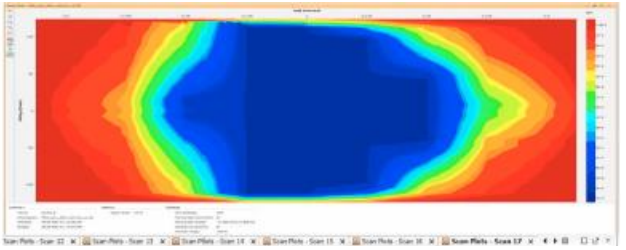



# BE Link Speed Test

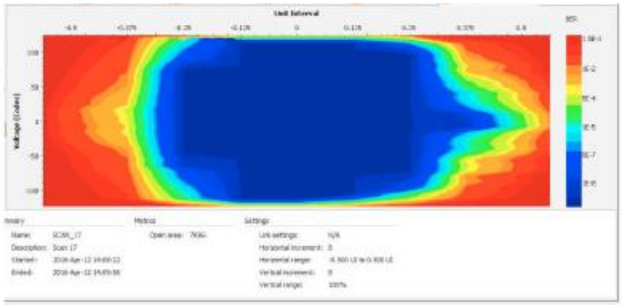
Link speed test between LATOME and LAr-L1Calo has been done

- Test 48 optical links from LATOME to e/gFEX, use test data as basis to set baseline link speed @6.4 Gbps
- Exercise different clock architectures, and setups for optical fiber splitters
- Good eye opening and BER (< 10-14) @11.2 Gbps have been achieved on both link speed tests
- Baseline link speed of 11.2 Gbps has been agreed upon



To gFEX



To eFEX

# Summary

- A new trigger readout system is being developed
- LAr Phase-I demonstrator
  - Successful data taking in 2015 runs
  - 2016 ATLAS data taking is ongoing
- Front-End electronics
  - Radiation-tolerant ASICs are being evaluated
  - Prototypes are being developed and tested
- Back-End LDPS
  - Prototypes development are processing well
  - Successful link speed tests with L1Calo have been done
  - Baseline link speed of 11.2Gbps has been agreed
- Full FE-BE Integration test will take place in early 2017 at CERN