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The Trigger Readout Electronics for the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeters

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LHC is planned to run at high luminosity during Run 3 from 2021 through 2023. In order to improve the identification performance for electrons, photons, taus, jets, missing energy at high background rejection rates, a new trigger readout system is being designed to process the signals with higher spatial granularity. The LAr Trigger Digitizer Board (LTDB) that will process 320 Super Cells signals is being developed. In this paper, results of the 64-channel LTDB and LTDB pre-prototype will be presented. Progress of development of the LTDB prototype for the final trigger readout system will be discussed as well.

Summary

The planned upgrade of the LHC will increase the instantaneous luminosity to $2-3\times10^{34}cm^{-2}s^{-1}$. The trigger readout electronics for the Phase-I upgrade of the ATLAS Liquid Argon (LAr) Calorimeters will be installed on the ATLAS detector during the second long shutdown of LHC in 2019/2020. The upgrade will improve the trigger energy resolution and efficiency for selecting electrons, photons, tau leptons, jets, and missing transverse momentum, while enhancing discrimination against pile-up. The readout of the trigger signals will process 34,000 so-called Super Cells at every LHC bunch-crossing at 12-bit precision and a frequency of 40 MHz.

The LTDB is the key electronics board for the upgrade. It will digitize the Super Cells signals and send processed data to the back-end electronics, where data are transmitted to the trigger processors. Each LTDB will process up to 320 Super Cells signals. The output data connection of an LTDB consists of up to 40 optical fibers running at 5.12 Gbps through the use of a custom serializer and optical link. With a total of 124 LTDBs in the system, the total rate to the back-end electronics is approximately 25 Tbps.

In order to evaluate performance of the upgraded electronics, understand the integration and manufacturing of large circuit board, an LTDB pre-prototype with the key components that are planned to be used for the LTDB has been developed. The LTDB pre-prototype processes the signals by the analog circuit that will be used on LTDB. It uses 80 custom 12-bit ADCs to digitize the signals, 10 Xilinx Artix-7 FPGAs to process the ADC data, and 20 custom MTx dual channel optical transmitters to send the serialized data to back-end electronics.

An LTDB 64-channel test board has been developed to verify the final design. The board is also an integration test platform for the radiation-tolerant ASICs used on LTDB. There are 16 custom 12-bit ADCs to digitize the Super Cells signals, and 4 custom Link-on-Chip (LOCx2) devices to interface with the ADC, prepare the data and serialize them for the optical transmitter. There are also 4 custom MTx dual channel optical transmitters to transmit the data to the LDPB (Liquid Argon Digital Processing Board), 1 GBTx, 1 GBT-SCA and 1 MTRx to configure on-board devices, control the power supply and monitor the voltage, current and temperatures. The preliminary test results show the radiation-tolerant ASICs work properly.

The final version of the LTDB prototype is being designed. It will implement 80 custom 12-bit ADCs to digitize 320 Super Cells signals, 20 custom LOCx2 devices, 20 custom MTx dual channel optical transmitters, 5 each of the GBTx, GBT-SCA and MTRx modules to implement the timing, slow control and configuration of the on-board devices.

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