



## Design and test performance of the ATLAS Feature Extractor trigger boards for the Phase-I Upgrade

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On behalf of the ATLAS Collaboration



# Outline

- Introduction
- ATLAS Level-1 calorimeter trigger architecture for Phase-I
- Trigger board design
  - Electron Feature Extractor (eFEX)
  - Jet Feature Extractor (jFEX)
- Prototype modules and test performance
- Summary

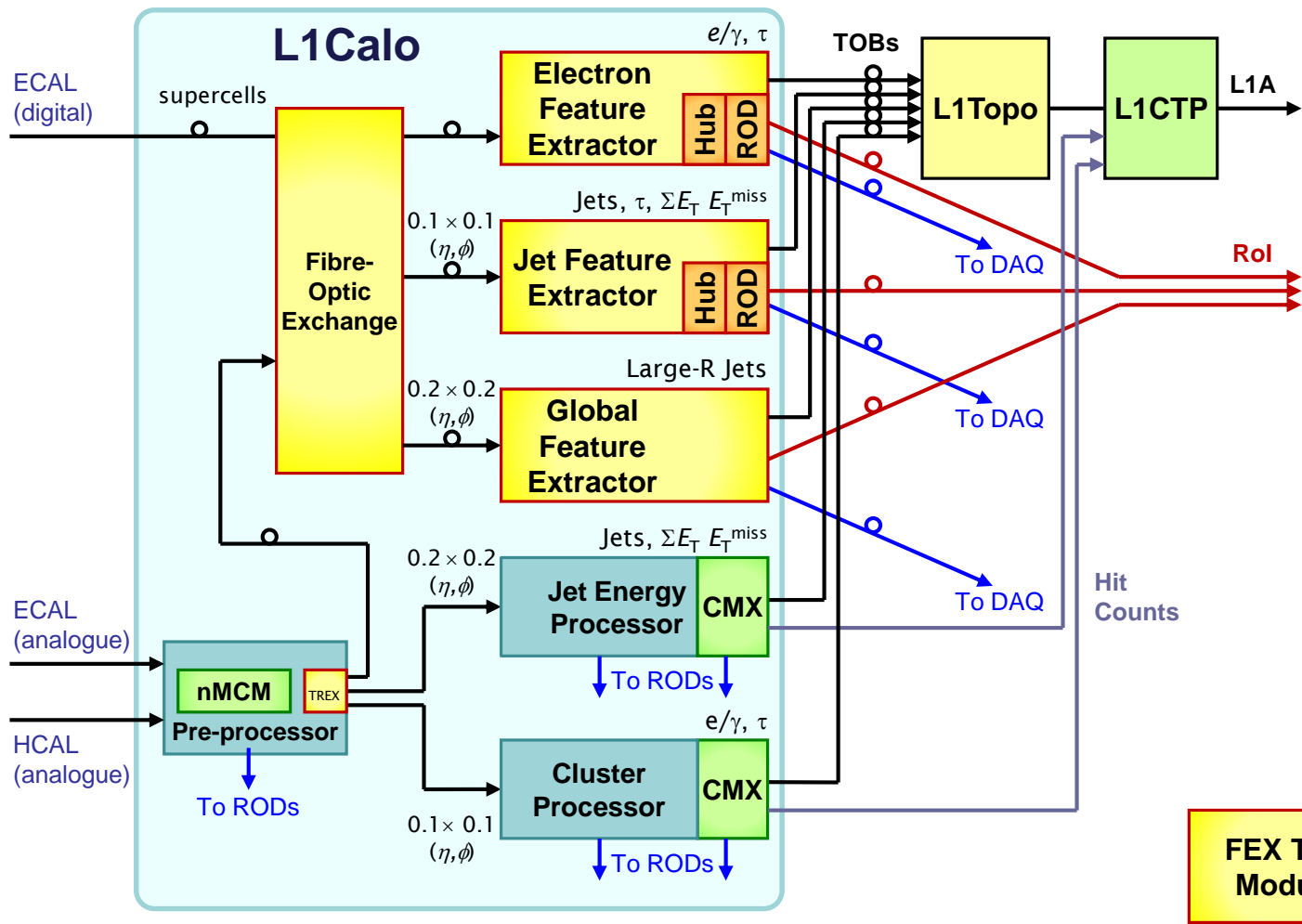


# Introduction

- Phase-I upgrade
  - LHC luminosity will double ( $\sim 2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ )
  - Total Level-1 trigger rate remains  $\leq 100 \text{ kHz}$ 
    - Retain sensitivity to electroweak processes
    - Stay within Level-1 trigger latency envelop of  $2.5 \mu\text{s}$
  - Forward compatibility with Phase-II upgrade
- Strategy
  - Use higher granularity from calorimeter
  - Include shower shape information
  - Improve pileup suppression with event-wide information
  - Identify large-radius jets

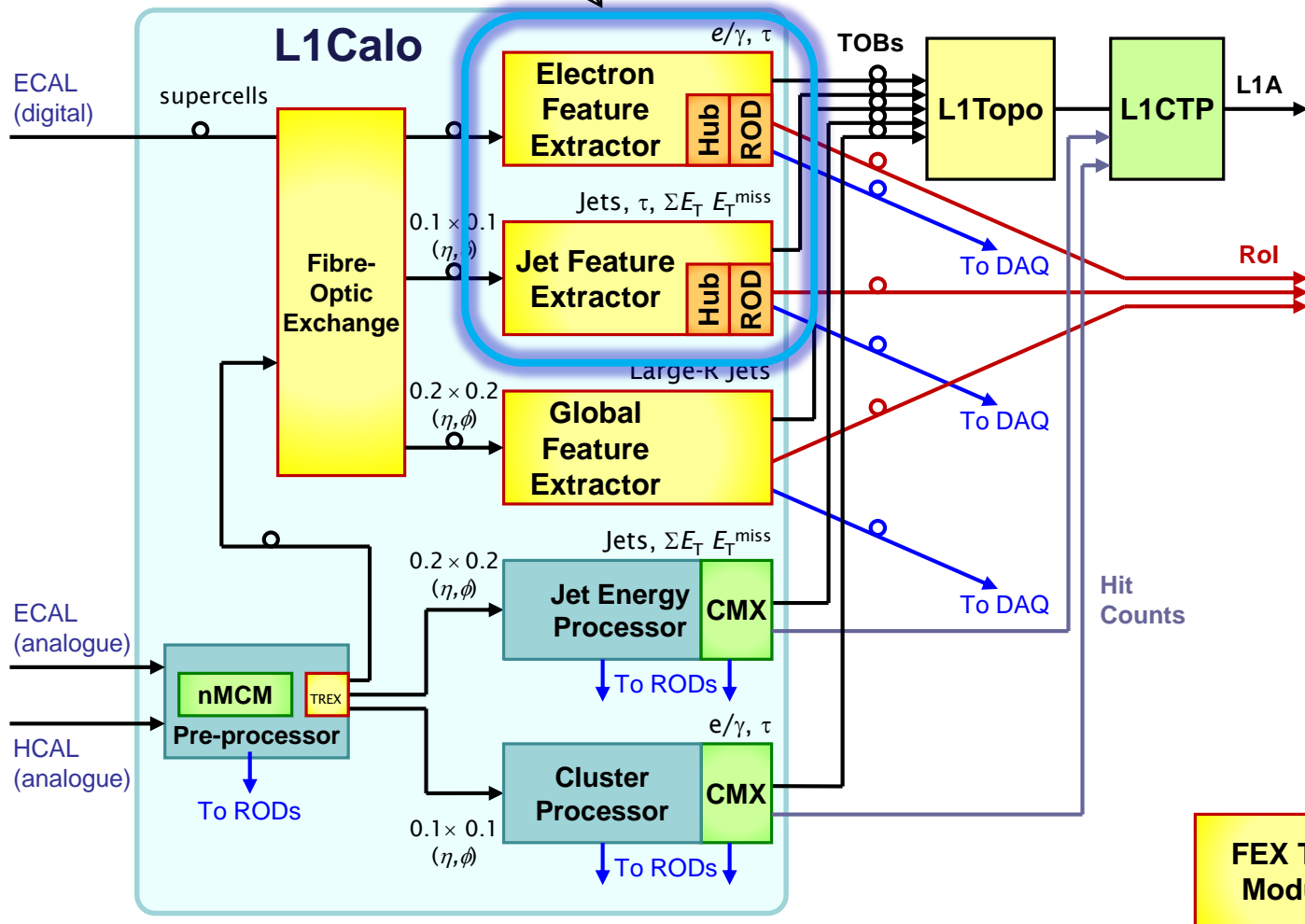


# L1Calo at Phase I





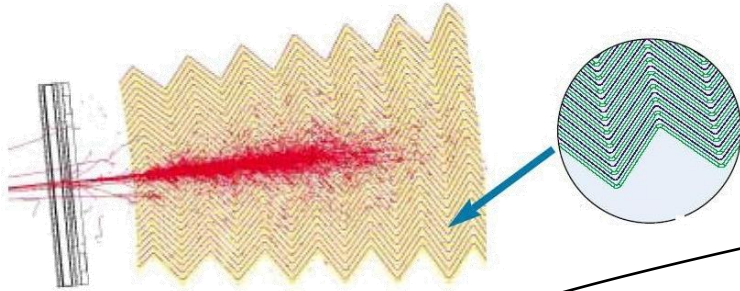
# Focus of this talk



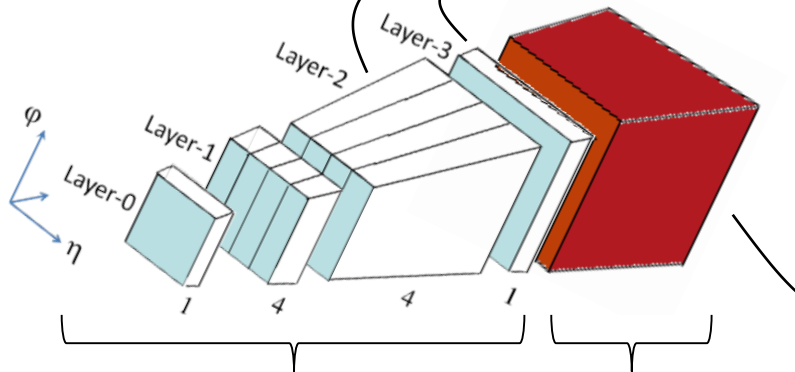


# eFEX Algorithms

➤ Cluster and identify  $e/\gamma$  and  $\tau$



EM shower in LAr



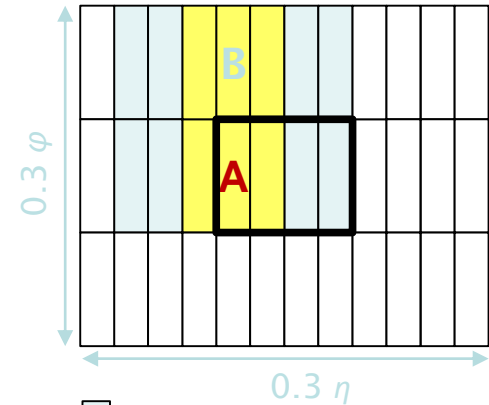
LAr supercell structure in a trigger tower of  $\Delta\eta \times \Delta\phi = .1 \times .1$

Tile trigger tower

$$R_\eta = \frac{E_{3 \times 2}}{E_{7 \times 2}}$$

$$f_3 = \frac{E_{S3}}{E_{Tot.}}$$

$$R_{Had} = \frac{E_{Had}}{E_{Tot.}}$$



Environment area (8 supercells)

Cluster area (6 supercells)

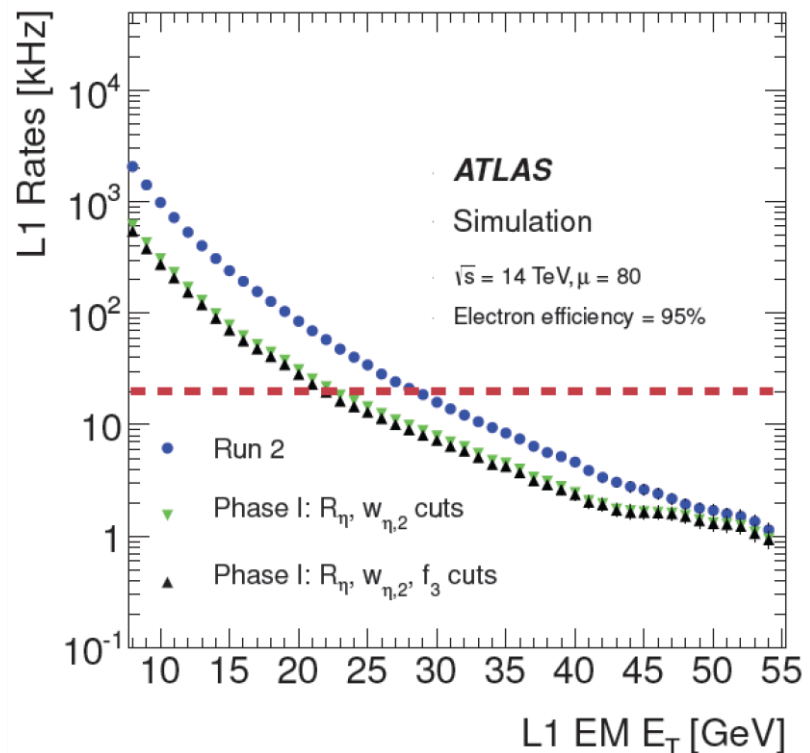
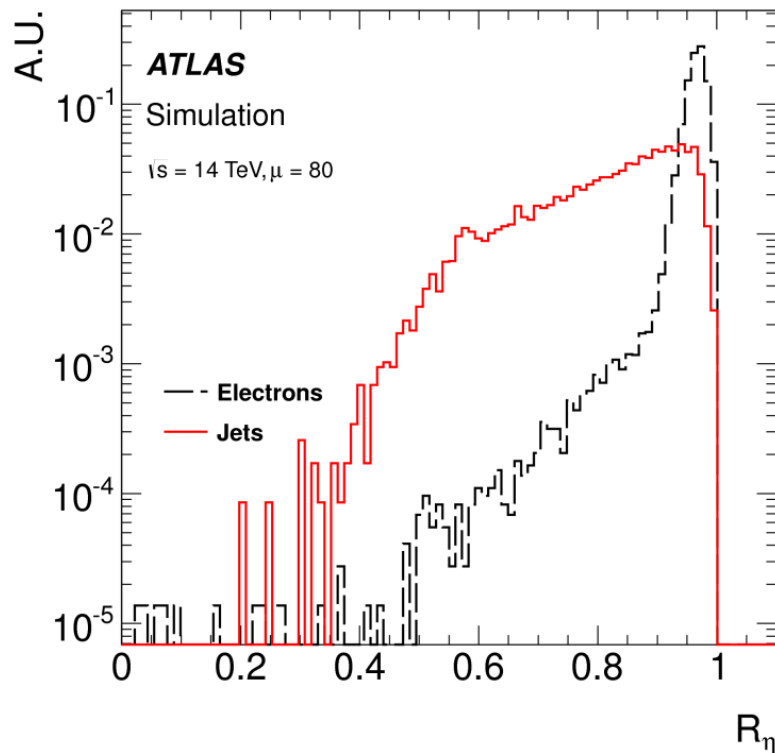
**A** Biggest local maximum in  $\eta$

**B** Biggest neighbour in  $\phi$  of **A**



# eFEX Trigger Performance

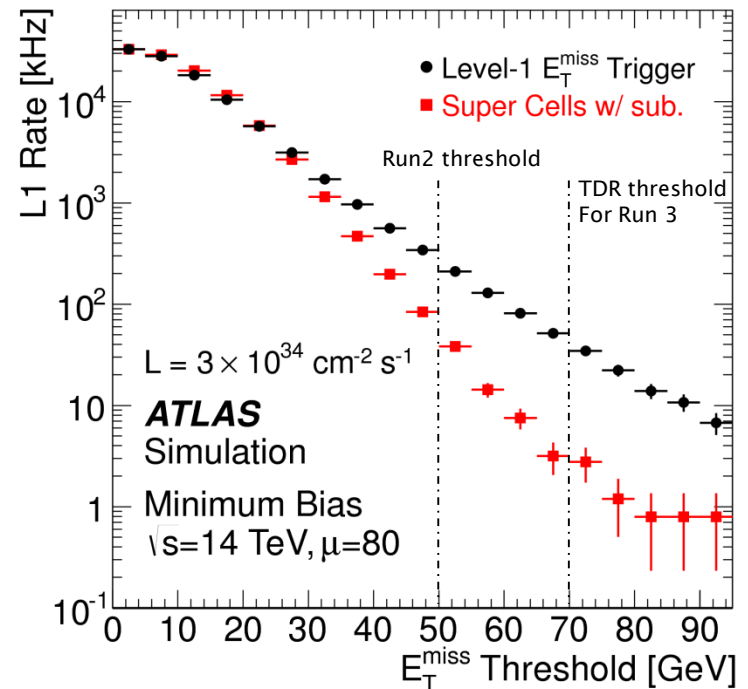
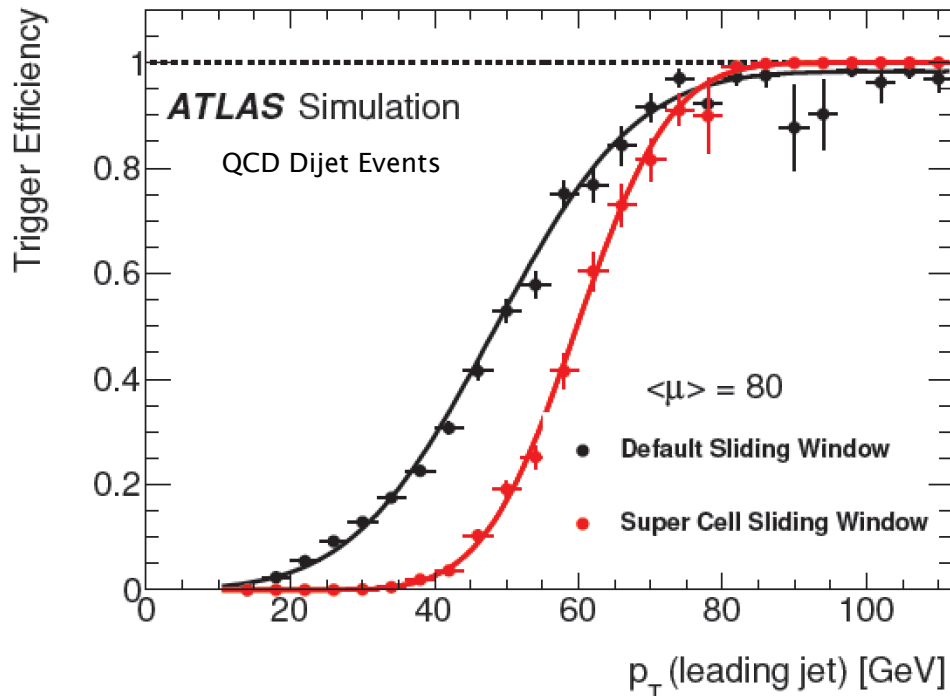
- EM trigger rate reduced by a factor of  $\sim 3$ , or
- The threshold lowered by  $\sim 7\text{GeV}$ 
  - Compared at reference points of 20KHz





# jFEX Trigger Performance

- Cluster and identify jets/fat  $\tau$  and calculate Sum  $E_T$  and missing  $E_T$ 
  - Gaussian weighting filter, larger window, higher granularity
- Enables pile-up suppression using event energy density
- Sharper turn-on for jet trigger and better missing  $E_T$  trigger
- Similar rate reduction as eFEX

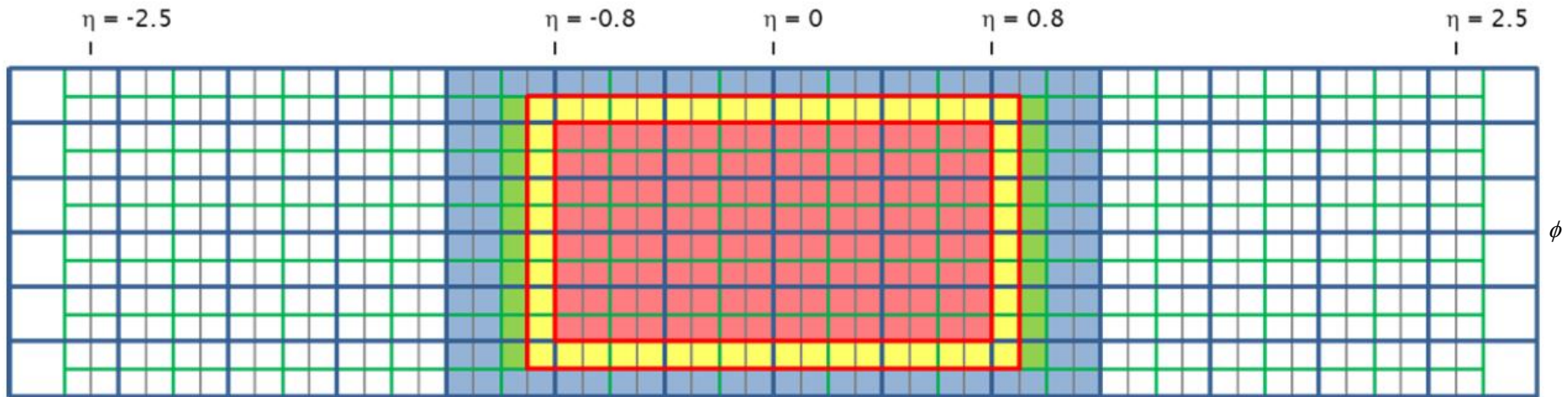






# eFEX partitioning

- 24 eFEX modules in total covering  $|\eta| \leq 2.5$
- Each eFEX module
  - Core area of up to  $1.7(\eta) \times 0.8(\phi)$
  - Environment area of  $1.8 \times 1.0$  (EM) and  $2.4 \times 1.2$  (HAD)

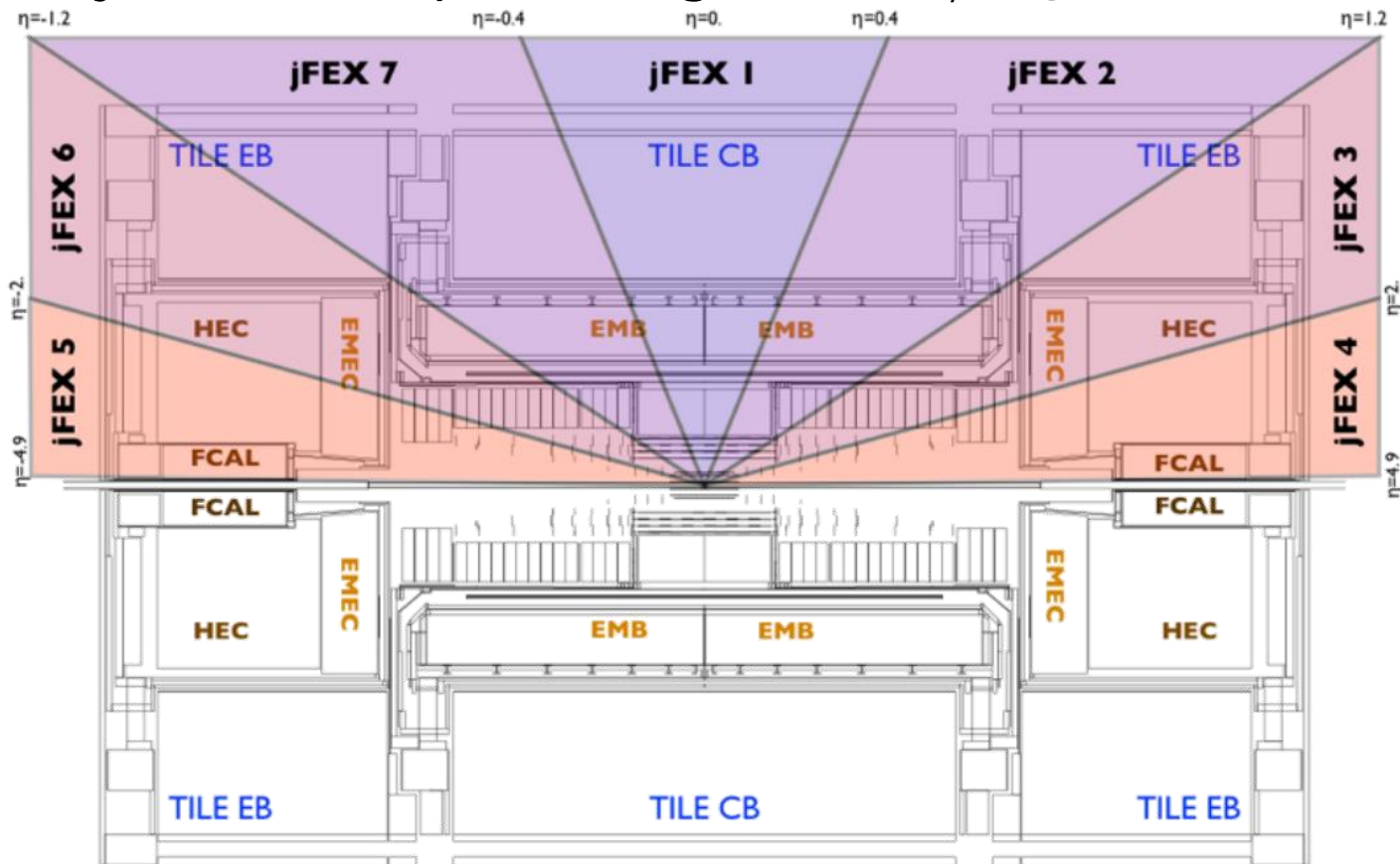


- Core area of algorithms
- Environment area of algorithms
- Extra area in LAr + Tile carried within fibres, but not used by algorithms
- Extra area in Tile carried within fibres, but not used by algorithms



# jFEX partitioning

- 7 jFEX modules in total
- Each jFEX module processing a whole  $\phi$  ring





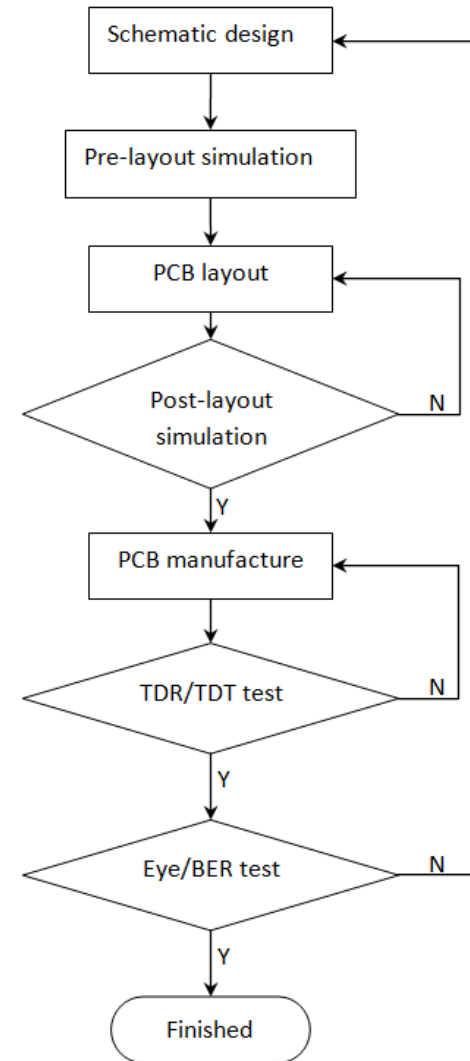
# FEX Module Concept

- ATCA form factor
  - Power estimate ~ 400W per module
- eFEX
  - 144 optical input, 36 optical output
  - 450 differential pairs on-board @10G+
  - 94 fan-out buffers @10G+
  - 17 MiniPODs
  - 4 Xilinx Virtex-7 FPGAs (XC7VX550T) - algorithm
  - 1 Xilinx Virtex-7 FPGA (XC7VX330T) - control + readout
- jFEX
  - 216 optical input, 32 optical output
  - 540 differential pairs on-board @10G+
  - 24 MiniPODs
  - 4 Xilinx Ultra scale FPGAs (XCVU190) - algorithm + readout
  - 1 Mezzanine - control

# Challenges

- Very high density
- Very high-speed
- Very complex signal mapping
- Very long signal tracks
- Very high power consumption
- Cooling

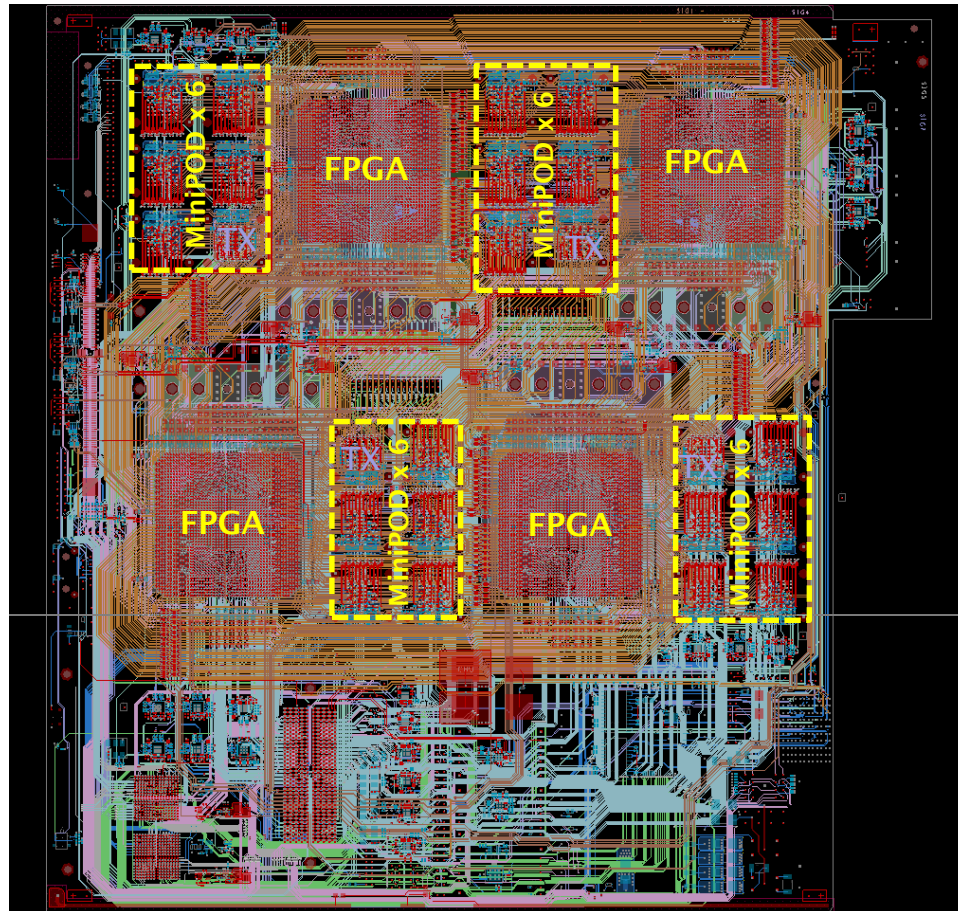
Systematic method for PCB design





# jFEX prototype

- Currently being manufactured (24 layer PCB – Megtron 6)

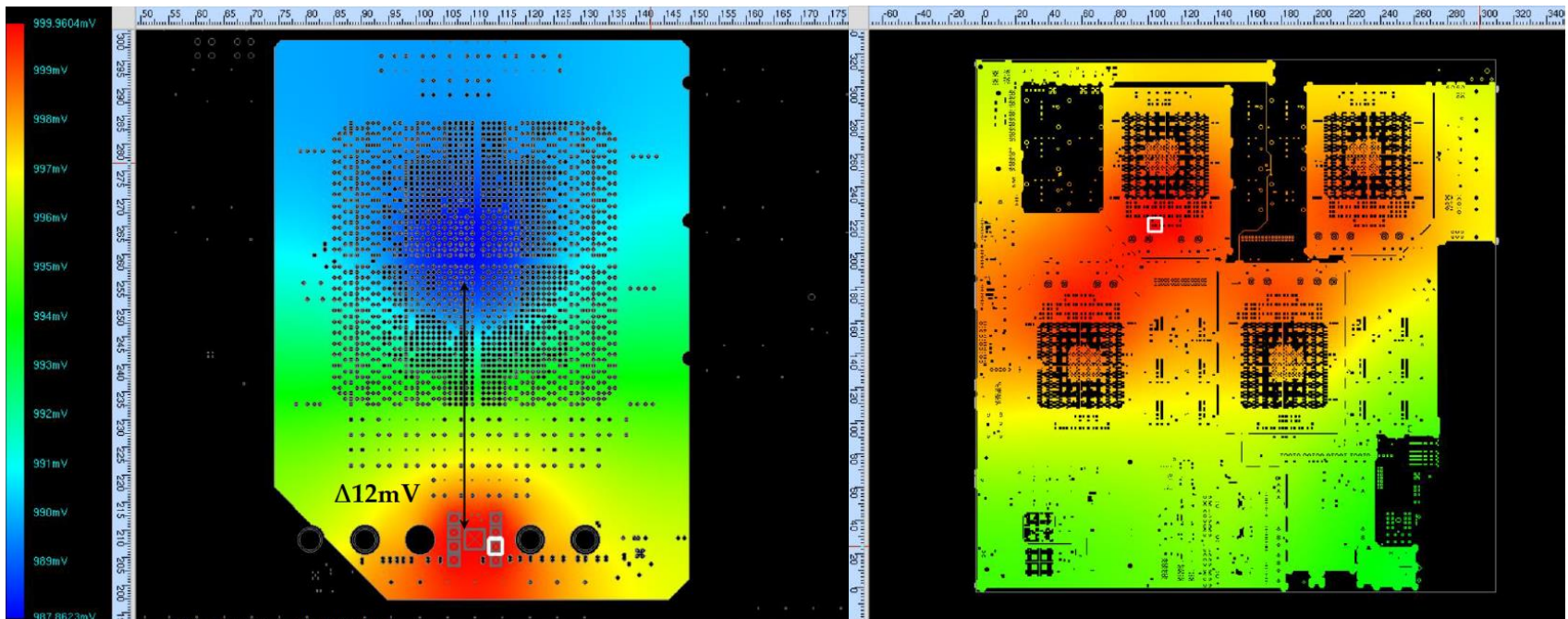




# jFEX power/thermal simulation

VOLTAGE DROP: VCC\_INT (1.0V/60A)

TEMPERATURE: VCC\_INT 1.0V/60A

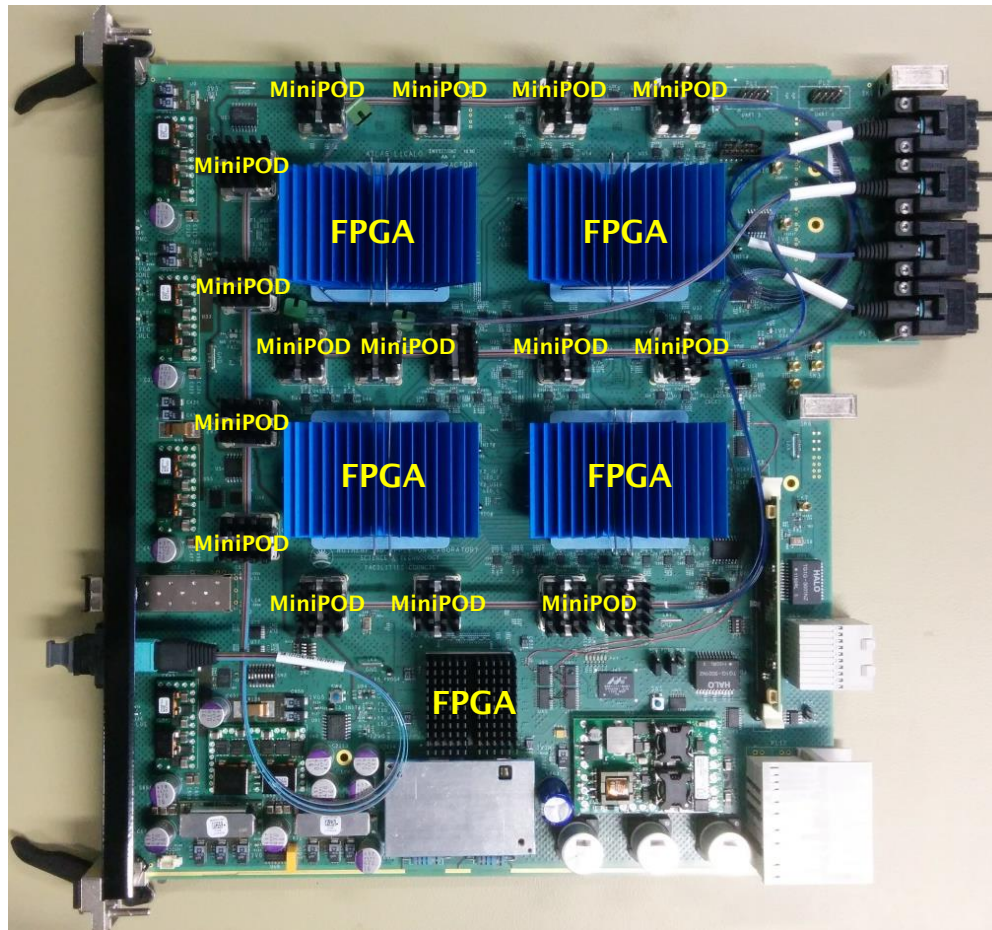


- Simulation optimised power plane design
- Thickness of high current planes:  $105\mu\text{m}$

- Power simulation: Max  $\Delta V \sim 12\text{mV}$
- Thermal simulation: Max  $\Delta T \sim 6.4^\circ$

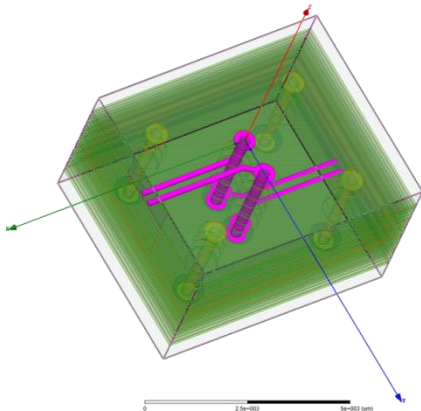
# eFEX prototype

- 1<sup>st</sup> eFEX prototype, Feb 2016
- 22 layer PCB
  - I-Tera





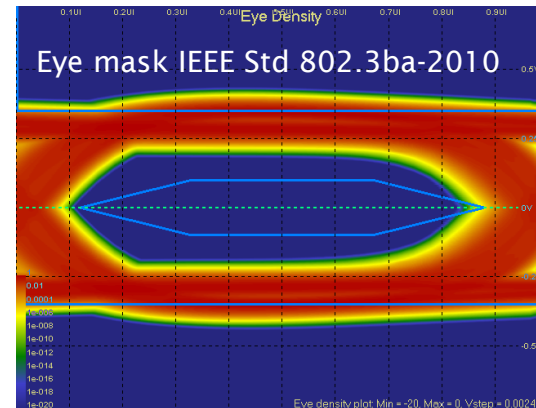
# eFEX SI simulation



3D via modelling

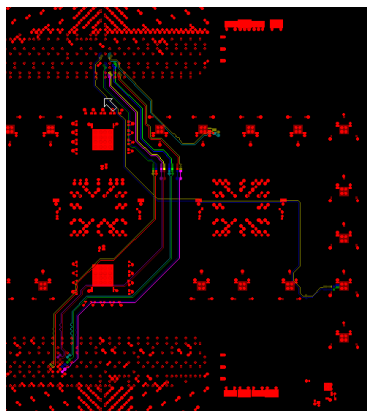


Single channel S-parameter extraction

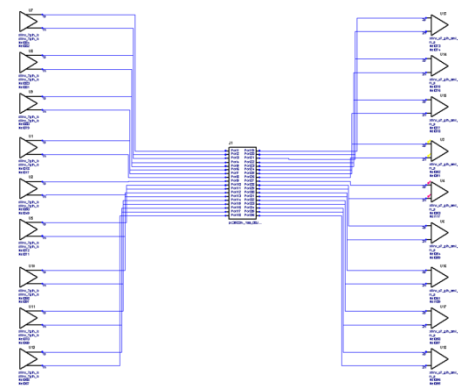


Eye diagram simulation

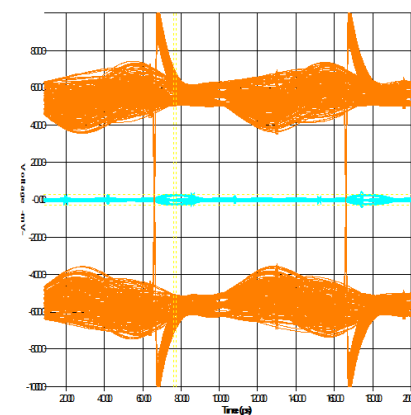
## Single channel simulation and optimization flow for 10G+



Parallel crosstalk channels



Multi channel S-parameter modelling



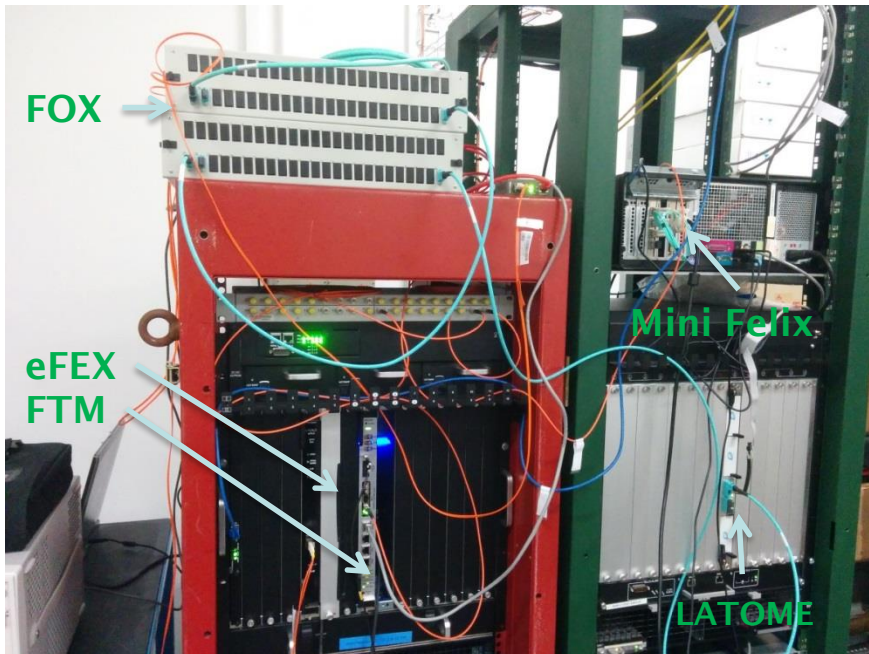
Crosstalk simulation

## Multi-channel crosstalk simulation and optimization flow for 10G+

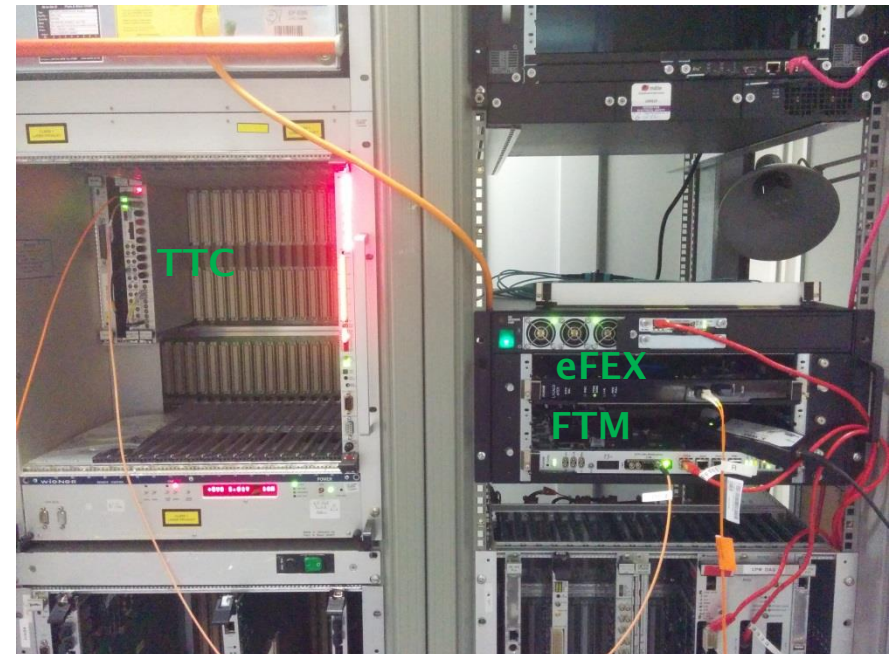


# eFEX link speed tests

- Validate TDR baseline link speed and test link speed limit
  - Two types of data sources
  - 3 different speeds (6.4G/11.2G/12.8G)



LAr LATOME AMC+ LDPB as data source @CERN  
(Altera Arria 10 FPGA)



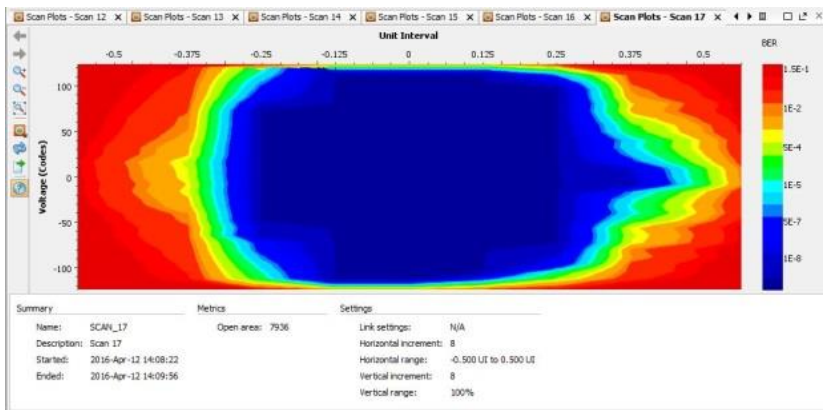
FEX Test Module as data source @RAL  
(Xilinx Virtex-7 FPGA)



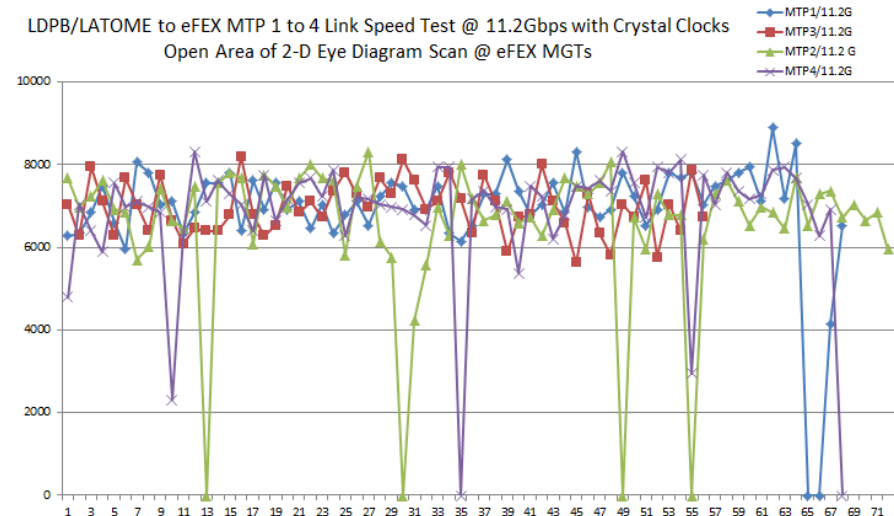
# eFEX link speed test results

- 97% eFEX high-speed links are very good
  - BER <math>10^{-14}</math> @ 6.4Gb/s (TDR baseline)
  - BER <math>10^{-14}</math> @ 11.2Gb/s (Chosen as new baseline)
    - Simplified system architecture (especially for jFEX)
    - Increased dynamic range of input calorimeter data
    - Simplified link data protocol
    - Improved trigger performance

Typical channel 2-D eye-scan @ 11.2Gb/s



LDPB/LATOME to eFEX MTP 1 to 4 Link Speed Test @ 11.2Gbps with Crystal Clocks  
Open Area of 2-D Eye Diagram Scan @ eFEX MGTs

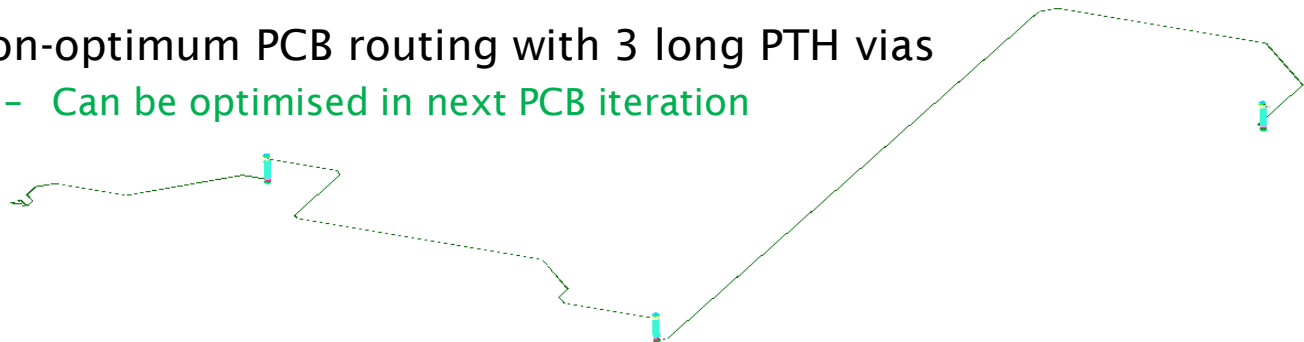
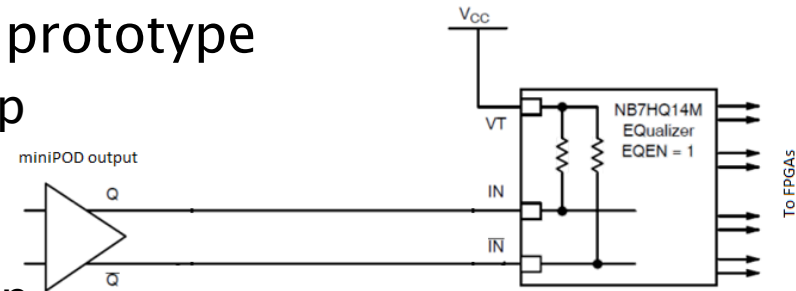




# eFEX high-speed link debugging

## ➤ 9 bad input channels on 1<sup>st</sup> eFEX prototype

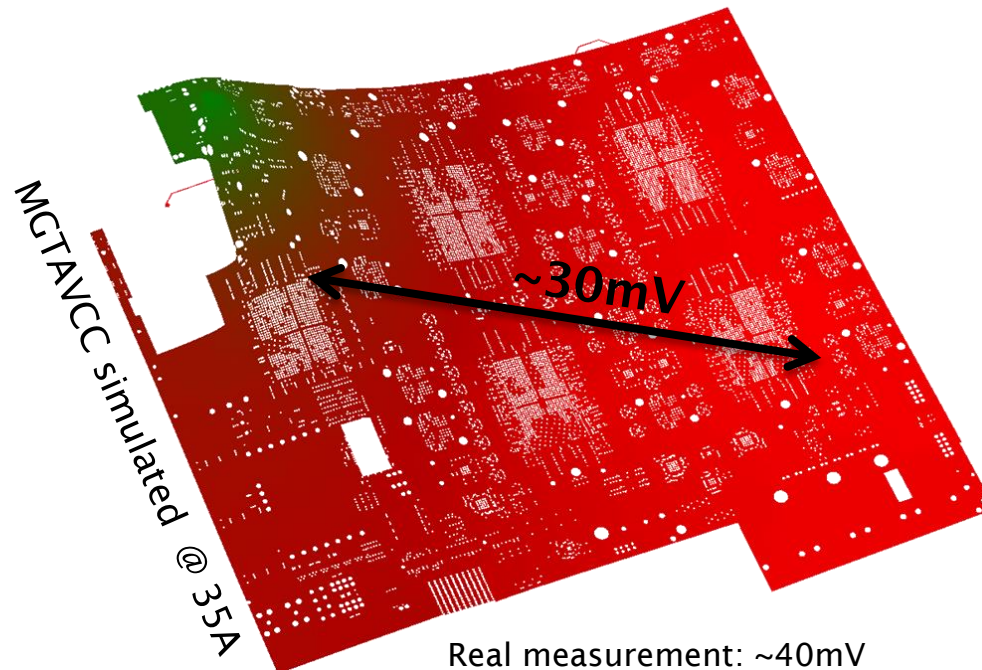
- 3 from the one fan-out buffer chip
  - BER  $\sim 5 \times 10^{-1}$
  - Bad fan-out buffer chip
- 2 from another fan-out buffer chip
  - BER  $\sim 10^{-4}$
  - Solved with replacing a miniPOD
- 4 from yet another fan-out buffer chip
  - BER  $\sim 10^{-11}$
  - Non-optimum PCB routing with 3 long PTH vias
    - Can be optimised in next PCB iteration



PCB routing topology between this buffer input and miniPOD

# eFEX power issue and simulation

- Xilinx XPE underestimated its Virtex-7 MGT power consumption by a factor of 2
  - Only half of MGTs can be activated simultaneously on eFEX
  - DC voltage drop would exceed limit (60mV) at full load
    - Need more copper in power distribution



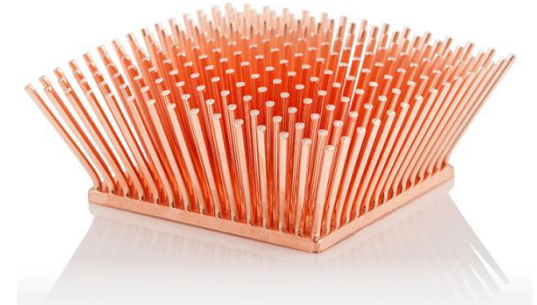




## Some open issues

### ➤ Cooling

- ~400W/module
- Temperature over 90°C(s) observed
  - Xilinx commercial FPGA rated 0°~ 85°(Cs)
- FPGA life expectancy decreases as temperature rises
  - But no quantitative number available



### ➤ Optical Fibre

- Very sensitive
- Limited mating cycles
- Cleaning MTP connectors in situ not easy
- Vibration in strong air flow inside ATCA shelf
  - Protection and long term reliability
- Dynamic reconfiguration for bad channel





# Summary

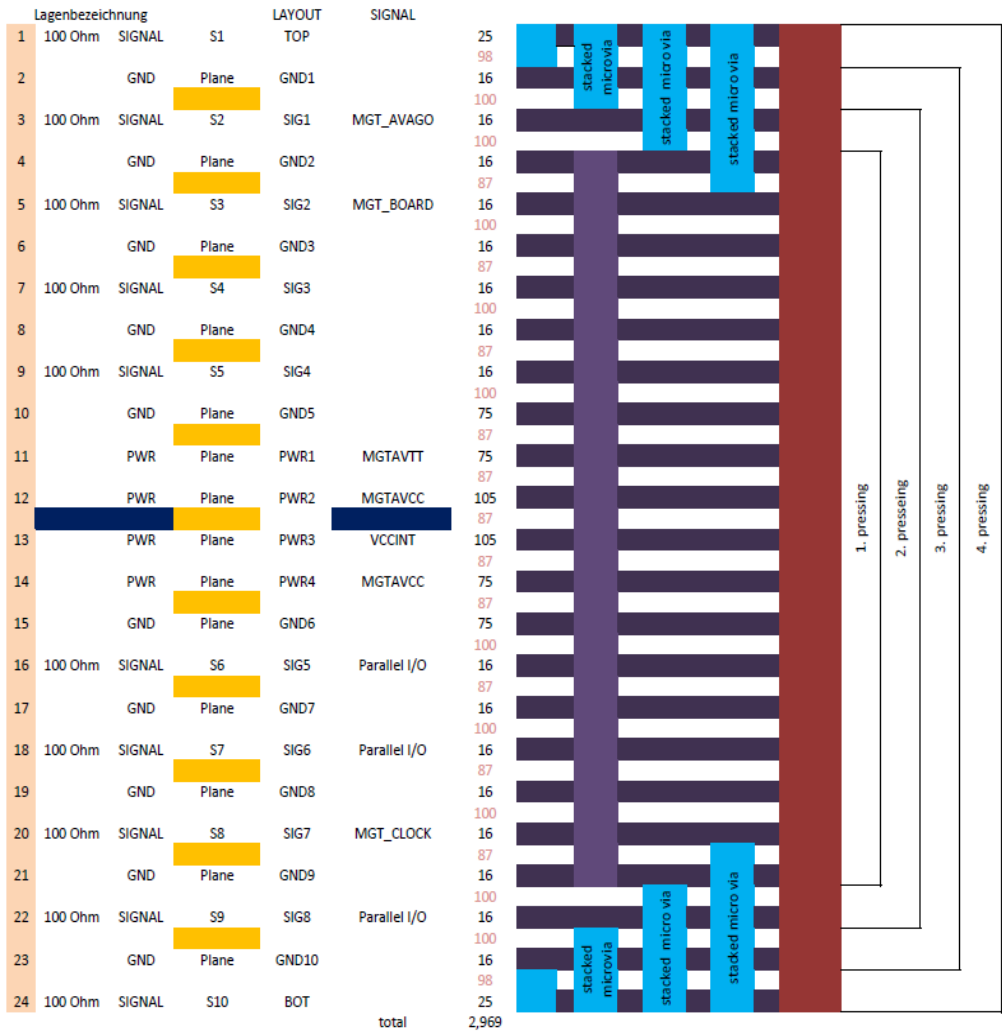
- The prototypes of ATLAS Feature Extractor trigger boards are well underway
  - eFEX: 2 delivered (1 tested), 2 more to come soon
  - jFEX: 1<sup>st</sup> module expected in Oct 2016
- The test results of eFEX 1<sup>st</sup> prototype are extremely good
  - The LAr/L1Calo link speed is re-baselined at 11.2Gb/s
  - Algorithm firmware are being developed
- Challenges to overcome with power, cooling and fibres



# Backup



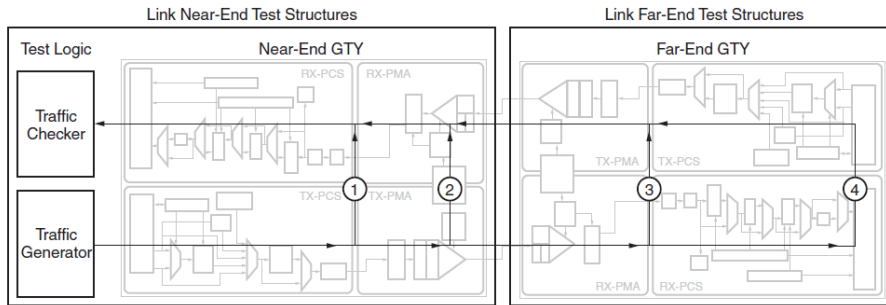
# jFEX PCB stackup



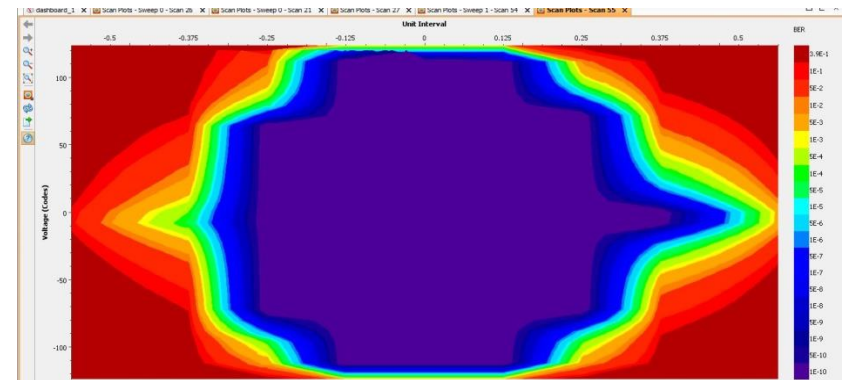


# jFEX on-board data-sharing test

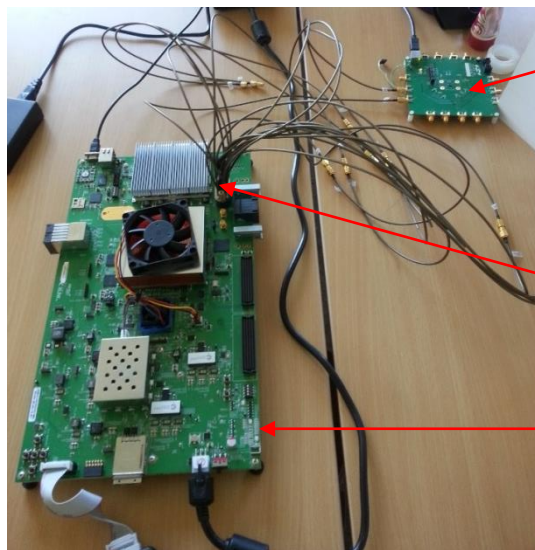
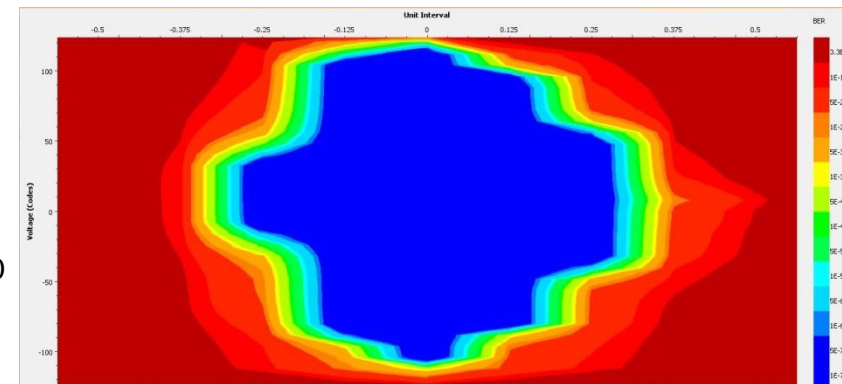
## Far-end PMA Loop-back (path 3) as inter-FPGA data sharing



25.5 Gbps - IBERT 2-D Eye scan @10<sup>-11</sup>



28 Gbps - IBERT 2D-Eye scan @ 10<sup>-8</sup>

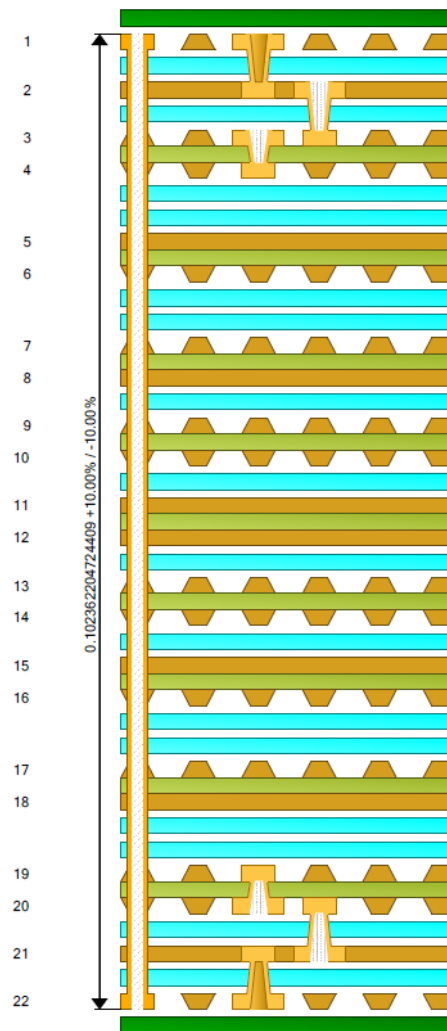
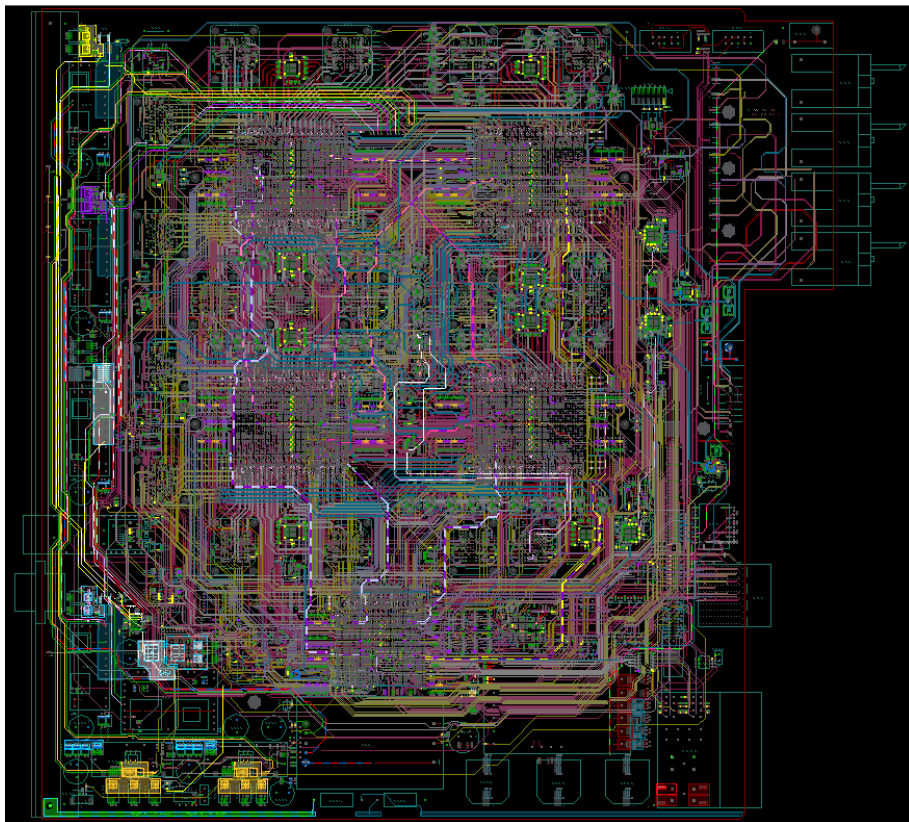


Ext clock (jitter cleaner  
eval board SiLab)

Samtec BullEye  
connector to GTY

Xilinx Eval Board VCU110  
(Ultrascale XCVU190)

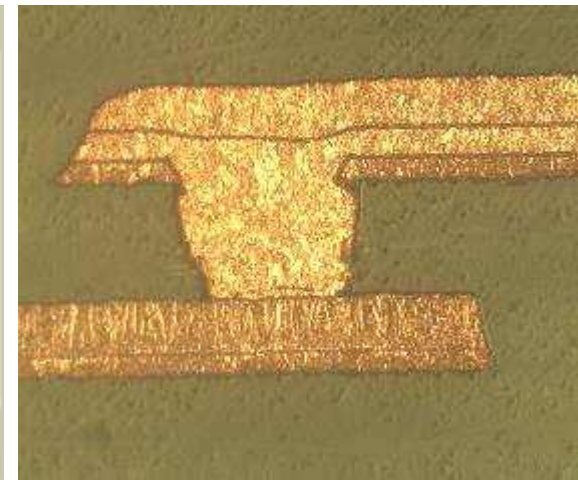
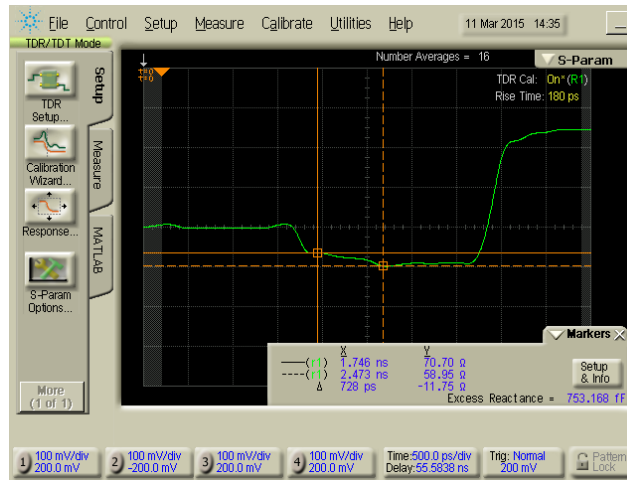
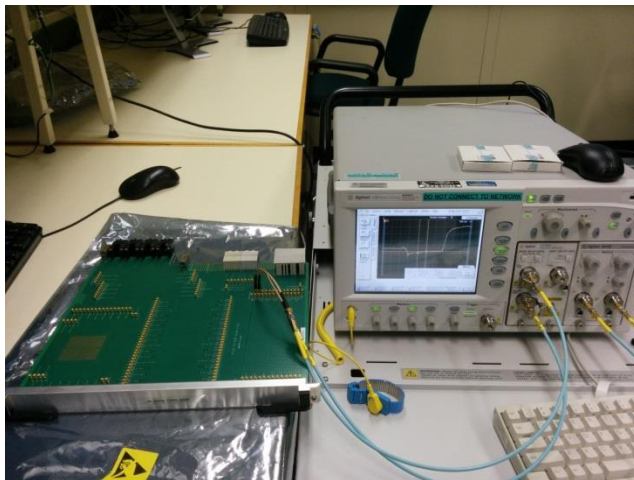
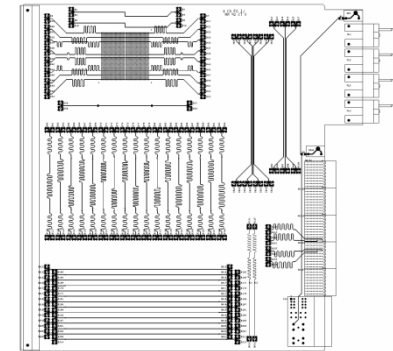
# eFEX PCB design





# eFEX Demo board

- Purpose
  - QA test on PCB
  - PCB simulation correlation
  - Mechanical test
- One critical error identified in PCB process



TDR/TDT tests on Demo PCB

Outer layer impedance too low ( $\sim 70\Omega$ ) due to over-plating