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An FPGA based track finder at Level 1 for CMS at the High Luminosity LHC

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A new CMS Tracker is under development for the High Luminosity LHC from 2025. It includes an outer tracker based on "PT-modules" which will construct stubs, built by correlating clusters in two closely spaced sensors. Reconstruction of tracks from stubs is required if the tracker is to contribute to the Level1 trigger under increased luminosity. A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented. Results from a hardware demonstrator system, where a slice of the track finder has been constructed to help gauge the performance of a full system, will be included.

Summary

The High Luminosity LHC (HL-LHC) will deliver luminosities of up to 5x10$^{34}cm^2/s$, with an average of about 140 to 200 overlapping proton-proton collisions per bunch crossing. These extreme pileup conditions place stringent requirements on the trigger system to be able to cope with the resulting event rates. One of the goals of CMS for the high luminosity upgrade is to maintain the physics performance achieved during Run 1 in 2012. While the Level-1 (L1) trigger will be upgraded to provide a maximum trigger rate of around 750 kHz (compared to <100 kHz in Run1), even with this increase in rate the thresholds for basic objects (muons, electrons, jets etc) will have to be tightened if no new information can be provided towards the L1 trigger making decision. Therefore a L1 trigger that can make use of reconstructed data from the silicon strip tracker is desirable, thanks to its superior momentum and spatial resolution for charged particles.

The tracking trigger task is to deliver track objects to the L1 trigger within about 5μs, in order to allow this information to be merged with that from other sub-detectors. Given that a 40 MHz silicon-based tracking trigger on the scale of the CMS detector has never been built, it is essential to demonstrate the feasibility of such system.

A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented, where track candidates are identified using a projective binning algorithm known as the Hough Transform. The detector is segmented into eight trigger regions in ϕ. By fully time multiplexing, each processing card receives all the data from an entire trigger region so that all regions can be treated, and demonstrated, independently. Results from a hardware demonstrator system, where a time slice of one track finding region has been constructed to help gauge the performance and requirements for a full system, will be reviewed.

The demonstrator system itself is conceptually divided into logical processing elements each of which is implemented on separate identical boards. The board is the Imperial MP7, a processing card which is capable of handling 0.94Tbps on 72+72 optical input and output links, using the Xilinx Virtex 7 V690 FPGA. One advantage of this division into steps is that it allows algorithms to be tested in isolation or as part of the daisy chain, using common hardware and infrastructure. Provided the algorithms are scaleable, it also allows for estimation of final performance without being limited to the boundaries of current FPGA technology. A description of the algorithms currently implemented will be presented and a discussion of future developments and prospects for this track finding proposal will be provided.

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