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Real Time FPGA Design for the L0 Trigger of the RICH Detector of the NA62 Experiment at CERN SPS

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The NA62 experiment aims to measure rare kaon decays, in order to precisely test the standard model. The RICH detector of the experiment is instrumental in charged-particle identification and in measurement of their crossing time, with a resolution better than 100ps. Here we describe the design of the Level-0 trigger system for the RICH, which provides a precise time reference by counting the input hit multiplicity within programmable fine-time windows. Because the design doesn't use spatial information and stands the maximum input rate of TDC-based NA2 systems, it can be employed also in other detectors.

Summary

The NA62 experiment at CERN is focused on a precise measurement of the branching-ratio of the very rare kaon decay $k^{+}\rightarrow{}^{+}$. In order to achieve that, various detectors are placed along the fiducial decay region, where a high intensity k^{+} beam is kept in vacuum. RICH detector aims to identify final-state particles (mostly π and μ) and measure their crossing time, with a resolution better than 100ps. In order to extract useful data from the intense flux, a three-level trigger system was developed. RICH L0-trigger (L0) provides precise time reference to the other levels of trigger, together with the multiplicity in a settable window. L0 is designed for *TEL62* boards, which are the general-purpose boards for trigger and acquisition. The board is composed of 4 *Pre-Processing* FPGAs receiving data from 4 daughter cards (*TDCs*) and sending the output to a *Sync-Link* FPGA, which merges the data and sends them to the *Level-0 processor* and the *PC farm*. All TEL62 FPGAs are *Stratix III* devices, clocked with a frequency of 160 MHz. In the FPGAs both the acquisition and trigger modules coexist, so the design logic occupation must be the lowest possible.

The aim of the RICH L0 primitive-generating firmware is to produce clusters of hits belonging to the same Cherenkov circle. No spatial information is used and only time clusters are produced, making this firmware very general and suitable for other detectors. In order to obtain more generality, a common 32-bit data format called RICH format was developed. Each module of the firmware uses RICH format as input and output, in order to move the modules wherever they are needed and to easily validate the data flux inside the FPGA. This format makes the firmware ready to the employment of *InterTEL* boards, which will be used to interconnect TEL62 boards.

The core of the firmware consists of 64 cells, arranged in 16 rows. A distributor sends hits belonging only to a 25ns time frame to each row, avoiding to split clusters between two consecutive bunches. Each cell takes its first input as time reference and clusters hits in input within a time-window. A collector receives clusters from the rows, time-sorts them down to 100ps and formats them with the RICH format. Particular attention was paid to reduce combinatorial paths length, in order to save logic utilization and improve the maximum clock frequency reachable by the design.

All the algorithms produced are real-time algorithms, which can stand the maximum input rate of TEL62 and TDC based detectors. After successful simulations and tests on the actual environment, the system was implemented in RICH *TEL62s*. Thanks to a very general design and to a maximum reachable clock frequency greater than the used one, the system could also be used in L0 trigger of other TDC-based detectors of the NA62 experiment.

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