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65nm Receiver with Decision Feedback Equalization for Radiation Hard Data Link at 5Gbps

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We present work to develop a radiation-hard receiver ASIC in 65nm CMOS with Decision Feedback Equalization (DFE), which is a very efficient technique for compensating the distortions caused by cable losses. Achieving the best possible compensation is particularly important for HL-LHC tracking detectors because the readout cable mass is inversely related to the tolerated amount of distortion. This work makes use of link design tools from Berkeley Wireless Research Center to determine the DFE architecture and generate the receiver circuit. Results presented include S-parameter measurements for ATLAS prototype cables, comparative eye-diagrams and plans for receiver layouts.

Summary

During the Phase-II upgrade the LHC will be prepared for a luminosity increase in order to improve the discovery potential of the machine. This means that the electronics need to be made to withstand increased radiation doses and the new readout system designed to handle higher data rates, something that is especially crucial close to the particle interaction point where the track density is the highest. For the upgrade of the ATLAS and CMS pixel detectors, located closest to the accelerator beam pipe, this requires a transmission chain that can transfer data from the pixel readout chips to the DAQ system in speeds around 5Gpbs. The cables used in this link system will be chosen based on radiation hardness consideration and low-mass constraints and will cause significantly more signal distortions during transmission than commercial high speed cables. The cable lengths depend on the geometry of the experiments, with ATLAS considering longer cables of up to 6m. In general, the less mass a cable has the greater the signal distortion caused by cable losses. Therefore, the higher the level of distortion that can be recovered, the lower the cable mass that can be used. Lowering mass is very important for tracking detectors, and so the best possible compensation for signal distortion is desired. Our goal is to design a receiver which uses an equalization technique to compensate for distortion and restore the initial signal (this can be used alone or in conjunction with driver pre-emphasis). One such equalization technique, which has gained popularity within digital communication industry applications due to its ability to expand the available bandwidth, is Decision Feedback Equalization (DFE). In this technique, any intersymbol interference (ISI) is removed by making use of previous decisions to estimate the current received symbol and reconstruct and subtract the ISI caused by previous symbols. In this way, the signal integrity can be significantly improved and data transmission speed maximized. A DFE can be implemented as a combination of simple Finite Impulse Response (FIR) filters, which are also called taps. In order to find a specific RX design that matches the ATLAS Phase-II pixel cables a Matlab-based link evaluation tool (LinkELF) has been used for initial high-level analysis of the system based on extracted cable S-parameters. S-parameters are measured on actual prototypes cables using network analyzers. LinkELF simulates the expected eye diagrams before and after equalization as a function of the number of DFE taps. Once the DFE architecture has been determined, the receiver schematics and layouts are generated using the Berkeley Analog Generator (BAG) framework, which is a tool for automated integrated circuit design developed by Berkeley Wireless Research Center. The BAG framework supports a number of CMOS nodes, including 65nm. We will present plans to fabricate a receiver designed using these tools.

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