Contribution ID: **11** Type: **Poster**

SLVS Transmitter and Receiver for Readout ASIC

Wednesday 28 September 2016 16:33 (1 minute)

Scalable Low Voltage Signaling (SLVS) Transmitter (Tx) and Receiver (Rx) IP blocks are designed in the UMC 180 nm CMOS technology as component of the readout ASIC for the muon chambers (MUCH) of the Compressed Baryonic Matter (CBM) experiment at FAIR (Darmstadt, Germany). These blocks are a prototype of the physical layer of the e-link interface that is used for ASIC-GBTx connection. The experimental results at 320 Mbit/s are presented.

Summary

In a series of the new generation of particle physics experiments (including CBM experiment at FAIR) the readout system has a following structure: several frontend ASICs are connected to a Gigabit Transceiver (GBTx) chip. Data from FE ASIC are sent to GBTx (transfer speed up to 320 Mbit/s per link), then serialized and sent to an off-detector processing system via optical link (speed up to 4.8 Gbit/s).

Connection between ASICs and GBTx is implemented by an e-link interface, its physical layer is implemented in accordance with SLVS or LVDS standards. Therefore, as part of work on the development of FE ASIC for muon chambers of the CBM experiment, the design of SLVS transmitter and receiver is necessary for providing compatibility with the e-link interface.

The SLVS standard was chosen in comparison with LVDS because of lower voltage swing (200 mV) and common-mode voltage (0.2 V). It reduces the impact on sensitive pads (e.g. charge sensitive amplifier inputs) and power consumption of the transmitter. The low common mode voltage simplifies the structure of the receiver.
The SLVS transmitter is implemented by a switched current sources based on H-bridge of N-channel MOS transistors, replica bias controls output common mode voltage. E-link standard allows a few of different transmitter output current values for different transmission speeds (up to 2 mA), but in this case only the maximum current value is provided.

The SLVS receiver is implemented by a P-MOS transistors input comparator with output buffer. Because of low common mode voltage, the provision of rail-to-rail input for this comparator is not necessary.

The transmitter and receiver are fabricated in late 2015 as part of a readout ASIC in theUMC 180 nm CMOS process which is the standard for electronics at FAIR.
The test structure contains the transmitter with serial input and differential output, which can be measured via differential probe, and the receiver with differential input and internal pad at the output for measurements via Picoprobe on probe station.

The measurements were performed at the following conditions: 40, 80, 160 and 320 MHz clock signals for transmitter and receiver and a data stream with PRBS (length $2^{11} - 1$) at the 40, 80, 160 and 320 Mbit/s speed. Transmission line is a 20 cm PCB stripline.

Tx parameters:

- Supply Voltage: 1.8 V
- Power consumption: 6.6 mW (at 320 MHz)
- Clock jitter standard deviation (at 320 MHz): 15 ps

- Total jitter (at 320 Mbit/s and 10^{-12} BER): 750 ps
- Eye height (at 320 Mbit/s): 350 mV
- Silicon area: 180x125 um^2

Rx parameters:

- Supply Voltage: 1.8 V
- Power consumption: 1.2 mW (at 320 MHz)
- Clock jitter standard deviation (at 320 MHz): 70 ps
- Total jitter (at 320 Mbit/s and 10^{-12} BER): 1.4 ns
- Eye height (at 320 Mbit/s): 1.4 V
- Silicon area: 150x55 um^2

The obtained parameters confirm the correct operation of designed blocks.

Author: BULBAKOV, Ivan (NRNU MEPhI)

Co-authors: ATKIN, Eduard (NRNU MEPHI); MALANKIN, Evgeny (NRNU MEPhI)

Presenter: BULBAKOV, Ivan (NRNU MEPhI)

Session Classification: POSTER

Track Classification: ASIC