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## Readout Channel with Majority Logic Timestamp and Digital Peak Detector for Muon chambers of the CBM Experiment

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A prototype readout channel was manufactured in UMC CMOS 180 nm for the purpose of the CBM experiment at the FAIR accelerator. The channel includes a preamplifier with fast and slow CR-RC shapers, discriminator with a differential threshold setup circuit, 6 bit SAR ADC (40 Msps, 1.5mW power consumption), digital peak detector and block of the time stamp registration. The control data, clock and output data are supplied through SLVS transmitter and receiver. The slow and fast channels have 1500 el and 2000 el ENC accordingly at a 50 pF detector capacitance. Power consumption is 10 mW/channel.

### Summary

The design and tests of the self-triggered readout channel for muon chambers of the CBM experiment are presented. The MUCH detector is built with GEMs. Since the sensors will have different granularity, the requirements to the front-end electronics are also different for the central and peripheral parts. Thus, the preamplifier is followed by two circuits: a slow channel, optimized for S/N ratio in order to use it in the periphery, and a fast one, adapted to the hit rate of the inner detector part, where the occupancy is the highest. The fast channel is also supposed to be used for the timestamp determination. Both channels are realized with CR-RC shapers with different peaking times, 60 ns and 260 ns accordingly. The measured ENC of the fast and slow shapers are no more than 2000 el and 1500 el correspondently at 50 pF of the equivalent detector capacitance. The channel is optimized to operate with the negative charge polarity. The preamplifier dynamic range is 100 fC. The channel occupancy is up to 1 MHz.

The shaper outputs are connected to the drivers, which make a single-ended to differential signal conversion. Further the signals are supplied to the differential comparator inputs. For regulating the threshold of the comparator a current 5 bit DAC is used. The DAC sets the threshold up to 80 mV with INL  $-0.20$  LSB and DNL  $-0.25$  LSB.

The signal from either slow or fast shaper (depends on occupancy) is processed by a 6 bit SAR ADC (INL  $-0.45$  LSB, DNL  $-0.70$  LSB) with a 40 Msps sampling rate and 1.5 mW power consumption. The ADC is followed by a digital peak detector. The peak detector has a function of the false peak find prevention due to the presence of noise spikes.

The chip has fast and slow discriminators. The fast discriminator output is connected to a timestamp block. Both fast and slow discriminators can be used by the logic for hit overlap detection. When the event in the channel occurs, the fast discriminator fixes the time of a 14 bit counter in the Gray code. The timestamp block also utilizes the majority logic to indicate the proper time of the event.

The final chip version is considered to be compatible with the GBTx data processing board. Thus, the data exchange is supposed to be via e-links. In the current version the data from ADC, peak detector and timestamp are serialized and sent out via SLVS transmitter at 320 Mbit/s. The 160 MHz clock signal is supplied via the SLVS receiver.

The ASIC layout area is  $3240 \times 1525 \text{ um}^2$ . The chip has been fabricated by the UMC MMRF 180 nm CMOS process as a double miniasic via Europractice. Measurements of the ASIC were carried out, including the

lab tests of the analog blocks with probe station. The results of the functionality and noise tests and their comparison with the simulation are presented.

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