A New Readout Electronics for the LHCb Muon Detector Upgrade

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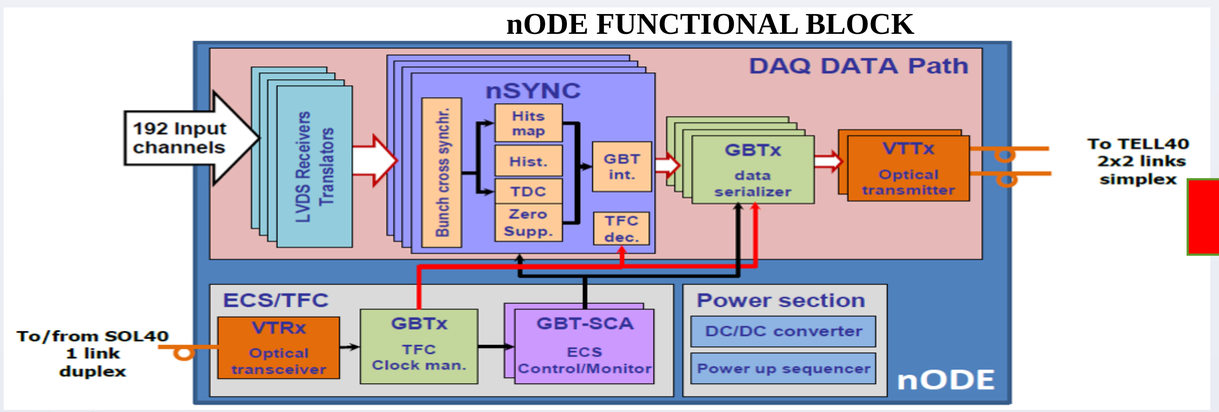
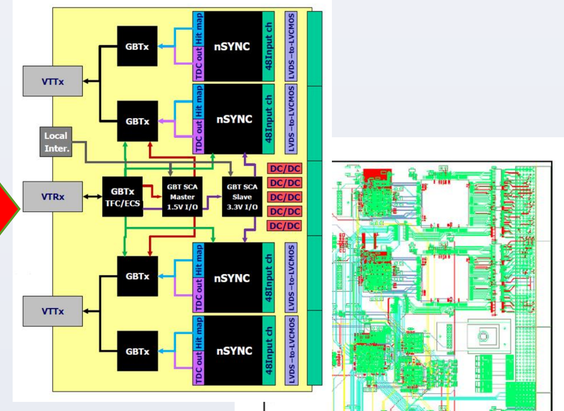
Introduction

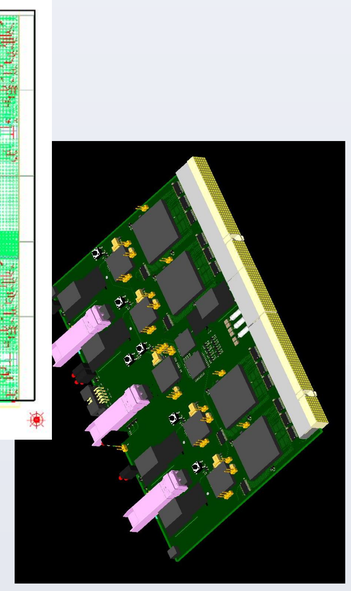
The 2018/2019 upgrade of LHCb Muon System foresees a 40 MHz readout scheme and requires the development of a new Off Detector Electronics (nODE) board that will be based on the nSYNC, a radiation tolerant custom ASIC developed in UMC 130 nm technology. The muon readout electronics has the purpose to convert the analogue signals extracted from the detector front-end channels into digital logical channels. The main changes of this upgrade involve the speedup of the readout clock, from the current 1MHz to 40 MHz (LHC clock), and the replacement of the optical communication system.

nODE Architecture

The muon readout electronics convert the analogue signals extracted from the detector front-end channels into logical channels (essentially X and Y strips). The analogue signals are amplified, shaped, discriminated and combined in logical-OR on the front-end boards before coming to the nODE board where are processed. The nODE has 192 programmable input channels and is based on a new radiation tolerant custom ASIC, the nSYNC.



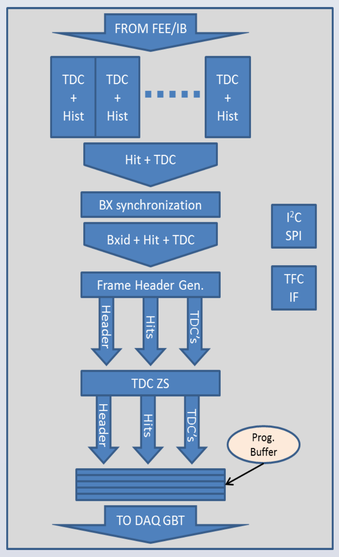




- FE & DATA electronics stage
  - 4 nSYNC (192 LVDS input channels)
    - Channel synchronization and BX alignment
    - Hits map, time measurements and histograms
    - Zero suppressions and data frame format
    - TFC commands decoder
    - GBTx interface and Data transmission
  - 4 GBTx (one per nSYNC)
    - WideBus mode
    - Fixed frame with fixed header
  - 2 VTTx (Dual optical transmitter)
- TFC/ECS electronics stage
  - 1 GBTx (Master GBTx)
    - Clock management
      - Master LHCb clock receiver
      - Clocks distribution and phase adjust
    - TFC commands receiver/fan out
      - Synchronization commands
  - 2 GBT-SCA (1.5V and 3.3V I/O)
    - ECS commands receiver/fan out
      - Initialization, monitor and debug
      - ECS protocol translation
  - 1 VTRx (Optical transceiver)
- Power stage
  - Power up sequencer
  - DC/DC converter
    - 5 FEASTMP_CLP
      - 3 DC-DC converters @ 1.5V
      - 2 DC-DC converters @ 1.2V

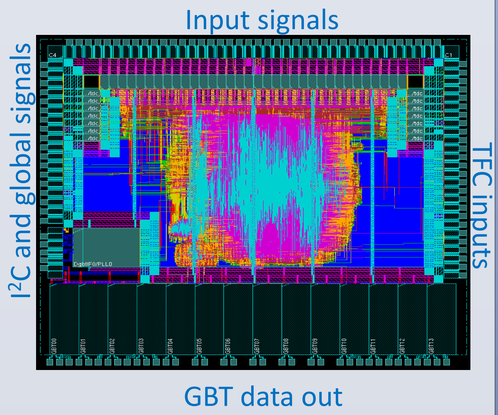
Each nSYNC communicates to its own GBTx to transmit data acquired to the DAQ system, based on a TELL40 board. The communication between nSYNC and GBTx is done using an e-link data rate of 320 Mb/s. On the nODE board an additional GBTx acts as master, it receives the master clock and the TFC command. Furthermore the GBTx master is interfaced with two GBT-SCA managing the ECS interface of the whole board.

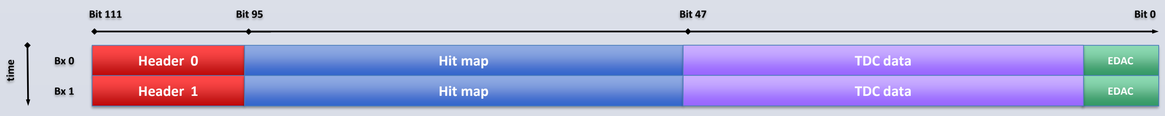
nSYNC Features and Architecture



The nSYNC is the core of the nODE. It is a 48 input channels ASIC in UMC 130 nm technology. It receives the data coming from the detectors and synchronizes them with respect to the bunch-crossing identification number (BXid). Concurrently, the incoming bits are monitored by a TDC (one for each input) that computes the arriving time of the signal inside the 40 MHz master clock period (phase time). This information is crucial for the time alignment of the whole muon detector. The system can work with several time resolutions, that is the number of slices on which the master clock is divided, from 8 to 32. The nominal resolution expected for LHCb is 16.
The data output of each TDC channel (@ 40 MHz) consist of a flag giving the simple binary info Hit/NoHit and a 5 bits-wide word with the measured phase (if any). These information go through a pipeline with programmable length in order to align different hits related to the same BXid.

The aligned data coming from the TDCs output are tagged with the correct 12-bit BXid identifier. The new complex-data is managed to create the extended frame with Header + HitMap + allTDCdata. The data are then Zero Suppressed (ZS)/truncated in order to fit the extended frame into the GBTx frame. ZS algorithm takes less than one master clock cycle. The Hit Map, that represents the "physics" information as well as the address of the TDC channels transmitted, is always sent NonZero Suppressed whatever the occupancy will be. The worst we truncate TDC data. In order to give some protection to our transmitted data, we included a Hamming code able to single error correction/double errors detection protecting all the data frame. The Hamming code requires 8 bits reducing the number of maximum TDC data we can transmit. For this reason the Hamming protection is programmable via ECS and can be disabled, to increase the max sustainable TDC occupancy. For nominal resolution the frame contains 10 channels, performing an occupancy of about 20%. The picture below show the GBTx frame (Header + HitMap + TDCdataZS).

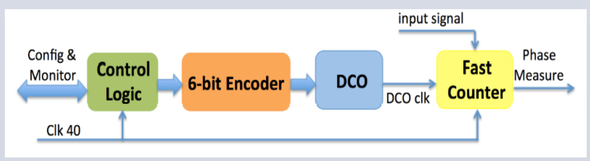




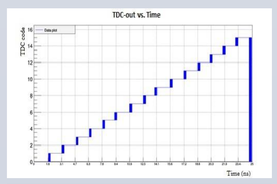
This whole frame is then transmitted to the GBTx at 320 Mb/s. An internal PLL generates the 320 MHz clock starting from the 40 MHz master clock.

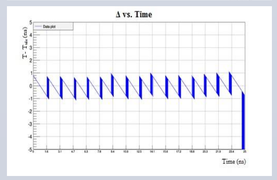
The TDC information can be also used internally to build a histogram of the incoming signal phase in order to perform the so-called fine-time synchronization that is crucial to achieve the required muon system efficiency. The histograms are read back through the ECS interface (I^2C), independently from the DAQ system. The ECS interface is used also to receive the configuration parameters and to allow the reading of the status registers from GBT-SCA. Furthermore, in order to receive the TFC commands an appropriate interface is integrated in the chip.

First Tests Results



The TDC integrated in the nSYNC channels is based on a DCO (named Giordano-DCO) fully digital developed for an INFN experiment (ALLDIGITALL) and recently **patented.** A simplified block scheme of the TDC architecture is pictured on the left: during calibration phase, the synthesizable DCO is controlled by a digital Control Logic through a 6-bit encoder. The encoder sets the DCO output frequency clock, which is then used to drive a fast counter performing the phase measurement between the 40 MHz reference clock and the input signal.



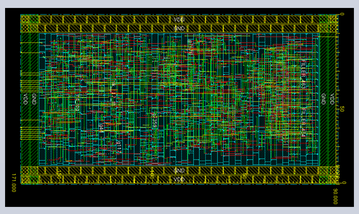


TDC was tested in a previous prototype (ADV2). Below the layout of the TDC cell and a table of its characteristic. On the left some results of tests on ADV2.

- The first plot represents a linearity test. The results refers to resolution 16 (LHCb nominal resolution) and they are quite satisfying.
- The second plot is derived from the results of the first test and represents the behavior of error, that is $T\text{-}T_{tdc}$, with respect to the phase.
- The last plot compares the error sigma vs resolution. The Sigma curve obtained from Post-Layout Simulation and the Sigma curve obtained from TDC's under test are shown along with the theoretical sigma curve plotted as reference. Results are in agreement with the expectations.

For some high resolutions we have small differences between the curves and we will investigate about it.

	TDC
Technology	UMC 130 nm
Size	90 x 171 μm².
Resolution step range	8 – 32
Reference clock	40 MHz
Voltage	1.2 V
Working Power Cons.	Around 200 μW
Rest Power Cons.	Less than 1 μW



Very preliminary tests have been performed on the nSYNC prototype:

- I^2C and TFC interfaces are ok
- PLL is ok
- Input channels are ok
- TDC's and histogram tools are ok
- We will start the test on the GBT interface in the next days

Besides an integrated simulation together with TFC and TELL40 systems on the LHCb framework has been made, showing fully compatibility of the nSYNC with such LHCb systems.