Contribution ID: **32**   Type: **Poster**

A New Readout Electronics for the LHCb Muon Detector Upgrade.

Tuesday, 27 September 2016 16:41 (1 minute)

The 2018/2019 upgrade of LHCb Muon System foresees a 40 MHz readout scheme and requires the development of a new Off Detector Electronics (nODE) board that will be based on the nSYNC, a radiation tolerant custom ASIC developed in UMC 130 nm technology.
Each nODE board has 192 input channels processed by 4 nSYNCs. The nSYNC is equipped with fully digital TDCs and it implements all the required functionalities for the readout: bunch crossing alignment, data zero suppression, time measurements.
Optical interfaces, based on GBT and Versatile link components, are used to communicate with DAQ, TFC and ECS systems.

Summary

The 2018/2019 upgrade of LHCb Muon System electronics includes some requirements that cannot be more fulfilled by the current readout system. The muon readout electronics has the purpose to convert the analogue signals extracted from the detector front-end channels into digital logical channels. The main changes of this upgrade involve the speedup of the readout clock, from the current 1MHz to 40 MHz (LHC clock), and the replacement of the optical communication system.
In this work, we present the new Off Detector Electronics (nODE) board and the nSYNC, a VLSI integrated circuit developed in UMC 130 nm technology.
After they have been amplified, shaped, discriminated, the signals coming from the detector, are processed in the new Off Detector Electronic (nODE) boards. They will replace the present ODEs and will be mechanically and electrically compatible with the present boards to avoid infrastructure modifications.
The nODE has 192 programmable input channels and is based on a new radiation tolerant custom ASIC, the nSYNC, which integrates all the required functionalities (clock synchronization, bunch crossing alignment, trigger hits production, time measurements, histogram capability and buffers).
The board uses only optical interfaces to communicate with the data acquisition and TFC/ECS systems. Such interfaces are based on the GBT and Versatile link components to guarantee full compatibility with the new electronic systems foreseen for the LHCb upgrade.
In each nODE there are 4 different nSYNC chips. Each nSYNC communicates to its own GBTx to transmit data to the DAQ system. The communication between nSYNC and GBTx is achieved using an e-link data rate of 320 Mb/s.
An additional GBTx (the Master GBTx) is used to receive the master 40 MHz clock and the TFC commands and to distribute them to the nSYNCs and to the other GBTx. Furthermore, the GBT master is interfaced with one GBT-SCA managing the ECS interface of the whole board.
The main purpose of the nSYNC is to synchronize the data coming from the detectors with respect to the bunch-crossing identification number (BXid). Each nSYNC channel is equipped with a fully-digital TDC that computes the arriving time of the signal inside the master clock period in order to achieve the crucial time alignment of the whole muon detector. The system can work with several time resolutions, that is the number of slices on which the master clock is divided, starting from 8 to 32. The nominal resolution expected for LHCb is 16.

To overcome the bandwidth limitation, the TDC data are zero suppressed inside the nSYNC through a combinatorial algorithm that requires only one clock cycle. The BXid tagged information, the digital hit maps of the channels and the TDC zero suppressed data are combined in data-frame that is transmitted to the DAQ at each clock cycle.

The chip includes also an I2C interface to receive the configuration parameters and to allow the reading of the status registers from GBT-SCA.

Primary author: CADEDDU, Sandro (Universita e INFN (IT))

Co-authors: LAI, Adriano (Universita e INFN (IT)); BALLA, Alessandro (Istituto Nazionale Fisica Nucleare (IT)); CARDINI, Alessandro (INFN Cagliari, Italy); LOI, Angelo (INFN - National Institute for Nuclear Physics); CASU, Luigi (Universita e INFN (IT)); CARLETTI, Maurizio (Istituto Nazionale Fisica Nucleare Frascati (IT)); GATTA, Maurizio (Istituto Nazionale Fisica Nucleare Frascati (IT)); CIAMBRONE, Paolo (Istituto Nazionale Fisica Nucleare Frascati (IT))

Presenters: CASU, Luigi (Universita e INFN (IT)); CADEDDU, Sandro (Universita e INFN (IT))

Session Classification: POSTER

Track Classification: ASIC