Development of a depleted monolithic CMOS pixel sensor in a 150 nm CMOS technology for the ATLAS Inner Tracker upgrade

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Introduction

	STAR	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC	
					Outer	Inner
BX-time [ns]	110	20 000	350	25		
Part. Rate [kHz/mm^2]	4	10	250	1000	1000	10 000
Fluence [n_{eq}/cm^2]	> 10^{12}	>10^{13}	10^{12}	2x10^{15}	10^{15}	2x10^{16}
Ion. Dose [Mrad]	0.2	0.7	0.4	80	50	> 1000

Monolithic CMOS pixels
- Small pixel (in principle)
- Low material
- Low cost

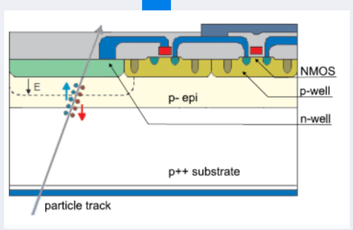

Fig. 1 conventional monolithic CMOS pixel

Hybrid pixels
- Fast
- Rad. hard

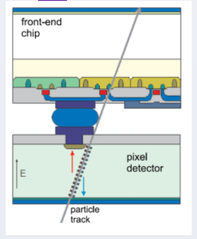

Fig. 2 hybrid pixel

Depleted monolithic CMOS pixels
- Inherit the features of conventional CMOS pixels
- May approach the hybrid performance by depleting the sensing volume
- A possible candidate for outer layers of ATLAS ITk upgrade

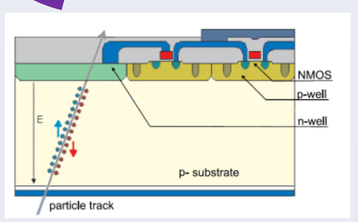

Fig. 3 depleted monolithic CMOS pixel

R&D route of depleted CMOS pixel sensors in LFoundry CMOS technology

❖ Implementation concept

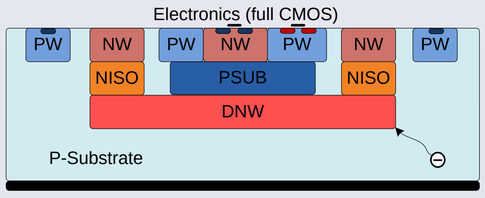

Fig. 4 Cross section of a depleted CMOS pixel

LFoundry CMOS3E technology
- *150 nm CMOS*
- *2kΩcm p-type bulk*
- *Multiple wells*
- *Thinning & back-side metallization possible*

- Charge collection diode realized by deep N-well (DNW)
- Full CMOS with isolation (PSUB) between NW & DNW
- Large fill factor for fast charge collection & radiation hardness
- However, large sensor capacitance => x-talk, noise & speed (power) penalties

❖ Prototypes

- *CCPD_LF[1,2]: submitted in Sep. 2014*

  - 33 x 125 µm^2 pixels
    => 6 CCPD_LF pixels equal to 2 FE-I4 pixels
  - Fast R/O coupled to FE-I4 & also stand-alone testability
  - Promising measurement results
    - Depletion depth reaching ~ 160 µm
    - Noise < 150 e-
    - 91% in-time hits for high threshold (~ 2600e-)
    - Still operate with acceptable performance loss after 50 Mrad, 10^{15} n_{eq}/cm^2

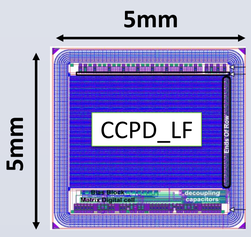

Fig. 5 Layout of CCPD_LF

- *LF-CPIX: submitted in March 2016*

  - Large size demonstrator chip
  - 50 x 250 µm^2 pixels => equal to FE-I4 pixels
  - 3 types of pixels with different add-on electronics
  - Improved designs
    - Faster & less noisy pre-amplifier
    - Comparator with less dispersion
    - Better protection for sensitive nets
  - New guardring strategy for less sensitive area and higher breakdown voltage (≳ 150 V)
  - Silicon expected by end of Sep. 2016

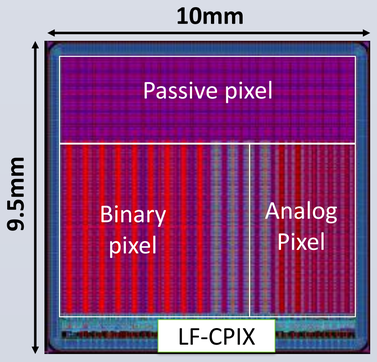

Fig. 6 Layout of LF-CPIX

- *LF-Monopix01: submitted in Aug. 2016*

  - Fast R/O monolithic design
  - Floor plan based on LF-CPIX
    - Bottom part kept almost the same
    - 30 rows removed on the top for extra periphery & I/O
  - Additional R/O logic in the pixel
    - Larger sensor capacitance => noise & timing penalties
    - Special design techniques required to avoid cross talk to sensing node

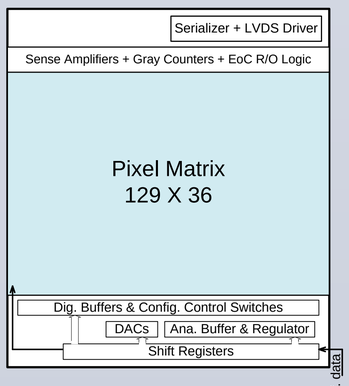

Fig. 7 Block diagram of LF-Monopix01

Design details of LF-Monopix01

❖ Pixel: LF-CPIX pixel + R/O logic

- FE-I3 like column drain R/O architecture [3]
- In-pixel RAMs for time stamp recording
- Low cross-talk operation is the key design point
  - Current steering logic for token transmission
    => constant current bias => low noise
  - Data R/O with source follower
    => avoid large current injection to pixel during R/O

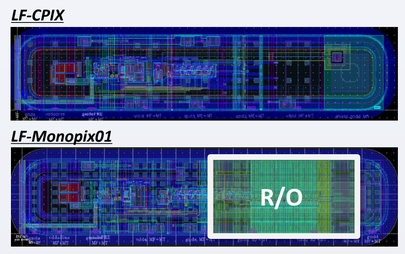

Fig. 8 Pixel layout: LF-CPIX & LF-Monopix01

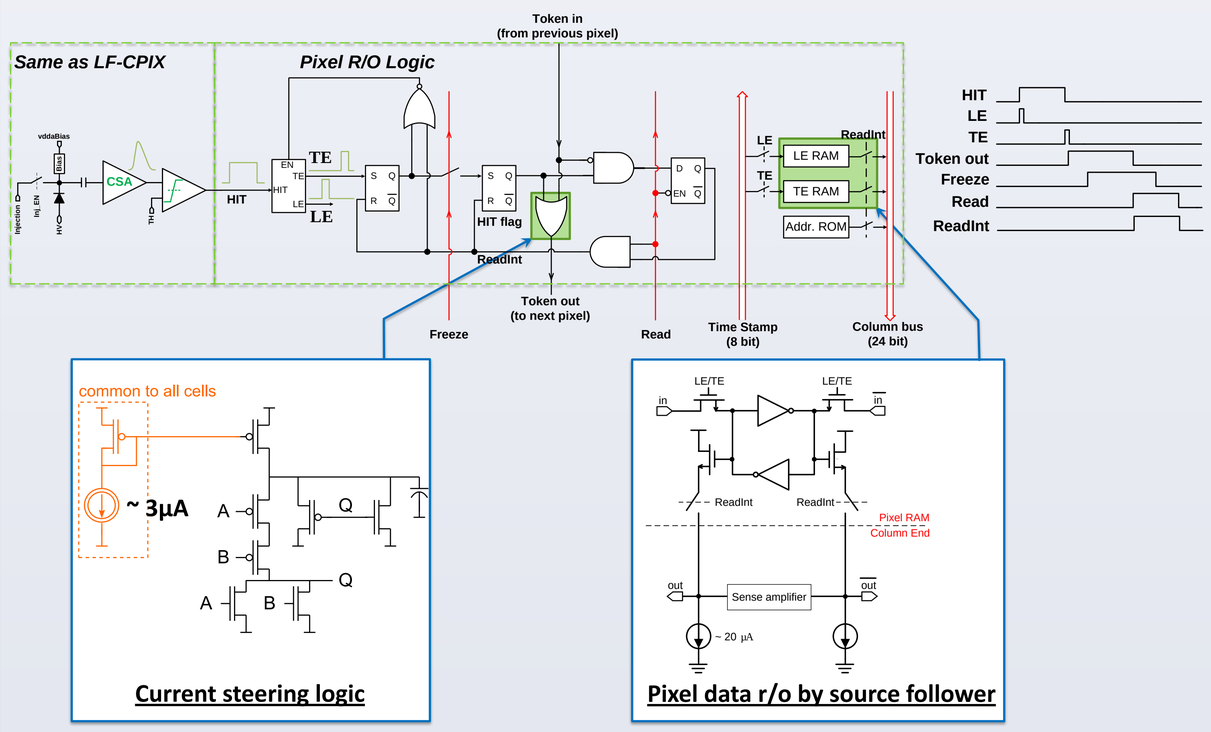

Fig. 9 Pixel schematic of LF-Monopix01 and timing diagram for operation

- Timing improved
  - Pre-amplifier: trading power for speed
  - Faster discriminator design
  - Time walk < 25 ns achieved (simulation)

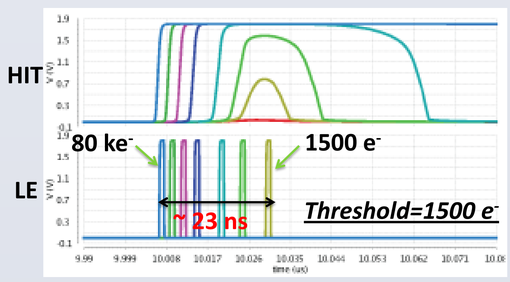

Fig. 10 Time walk simulation for one pixel

❖ Column R/O scheme

- End-of-Column (EoC) circuit
  - Sense amplifiers => receive & latch data
  - Gray counter => provide time info. (40 MHz)
  - EoC R/O logic => R/O priority scan at column level
  - Digital buffers
- Serializer and LVDS driver => 160 Mbps output rate
- Off-chip R/O controller for design simplicity

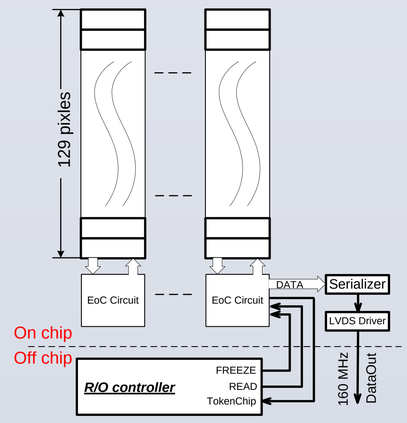

Fig. 11 EoC R/O scheme

Conclusion

- Since a few years a lot of activity in the field of depleted CMOS pixels for ATLAS
- Promising results obtained in LFoundry 150 nm CMOS technology
  - Large size demonstrator chip to be tested soon (Oct. 2016)
- A first monolithic design in LFoundry was recently submitted
  - Aimed at the outer layers of ATLAS ITk upgrade
  - FE-I3 like R/O architecture
  - Extensive design efforts for low cross-talk and fast response
  - Chip functions verified in post layout using FastSPICE simulation tools

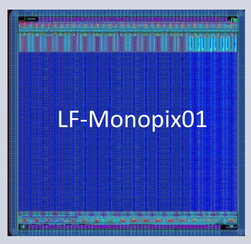

Fig. 12 Layout of LF-Monopix01

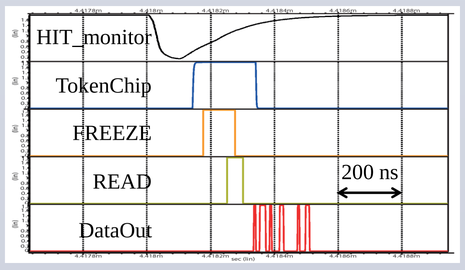

Fig. 13 Full chip post layout simulation with one pixel fired in the pixel matrix

Reference

[1] P. Rymaszewski et al., JINST 11 (2016) 02 C02045
[2] T. Hirono et al., doi:10.1016/j.nima.2016.01.088
[3] I. Peric et al., doi:10.1016/j.nima.2006.05.032

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