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Design of a Depleted Monolithic CMOS Sensor in a 150 nm CMOS Technology for the ATLAS Inner Tracker Upgrade

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CMOS pixel sensors with notable depletion have been demonstrated to be feasible candidates for the ATLAS Inner Tracker (ITk) upgrade, replacing the current passive sensors. A further step to exploit the potential of CMOS sensors is to investigate the suitability of equipping the outer layers of the ATLAS ITk upgrade with fully monolithic CMOS sensors. In this work, a monolithic CMOS pixel sensor, named MONOPIX-01, has been designed in the LFoundry 150 nm CMOS technology. The submission is foreseen in the middle of May 2016. Design and simulation results will be presented.

Summary

Standard CMOS pixel sensors have proven to be high precision devices in high energy particle physics experiments, thanks to their fine granularity and low material. Moreover, the use of commercial technologies makes them very suitable for large area trackers due to their low cost. However, existing CMOS detectors in commission or under construction still suffer from limited speed and radiation hardness, excluding them from being used in the extreme radiation environment like ATLAS. A recent trend to exploit the high-voltage/high-resistivity CMOS technologies to increase the depletion of the CMOS sensors have eventually made them feasible candidates for the ATLAS upgrade.

Aimed at qualifying available CMOS technologies to build high performance, cost efficient CMOS detectors for the ATLAS ITk upgrade, an R&D collaboration called “CMOS demonstrator” was started. Various depleted CMOS sensors have been developed in different technologies. Encouraging measurement results have been obtained, demonstrating the feasibility of CMOS sensors being candidates for the ATLAS ITk upgrade. However, these sensors are either passive or active ones with first stage(s) of front-end electronics integrated on the sensor substrate. The data readout and processing rely on a readout chip, bump bonded or glued to the sensor. A more ambitious step to explore the potential of depleted CMOS sensors will be the development of fully monolithic sensors, which may be suitable for the outer layers of the ATLAS ITk upgrade.

This work focuses on the design of a monolithic sensor in a 150 nm CMOS technology, namely MONOPIX-01. This technology features quadruple wells, and a high resistivity ($> 2 \text{ k}\Omega\cdot\text{cm}$) P-type substrate is used for implementing the sensor. The charge collection node is formed by a deep N-well, which is also used to host the in-pixel readout electronics. A deep P-type layer is used to isolate the N-well from the deep N-well, so that full CMOS capability is achievable in the pixel. The design contains an array of 142×36 pixels, with two pixel variants featuring different pre-amplifying stages. The pixel size is $250 \mu\text{m} \times 50 \mu\text{m}$. The readout of the pixel array employs the “column drain” architecture. In each pixel, the charge signal is amplified by an amplifier, and then compared to a programmable threshold by a discriminator. Two 8-bit gray-coded time stamps, corresponding to the rising leading edge and trailing edge of the discriminator output, are stored in two in-pixel RAM cells. A readout controller initiates the priority scan after receiving a hit flag from the pixel array, so that the hit pixels are read out successively. The data is serialized and sent out by a LVDS driver with a bit rate of 160 Mbps. For design simplicity, the readout controller will be implemented off chip by the FPGA. The submission is scheduled in May 2016.

Short overview of existing development in the same technology, as well as the design and simulation results of MONOPIX-01 will be presented.

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