Pixel architectures in HV/HR CMOS Process for ATLAS Inner Detector Upgrade

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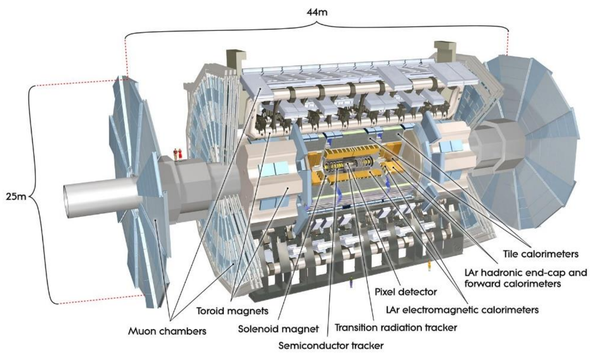
ATLAS Phase-II Inner Tracker Project



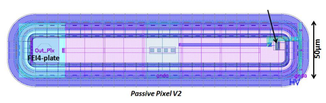
The ATLAS experiment at CERN

Challenges for phase 2:
- **Radiation hardness**
- **Readout time (high rates)**

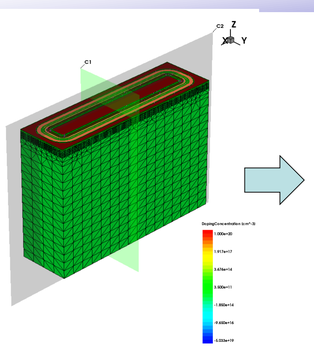
	ATLAS-LHC	ATLAS-HL-LHC	
Bunch crossing (ns)	25	25	
Particle rates [kHz/mm²]	1000	1000	10000
Neutrons flux [n_{eq}/cm²]	2x10^{15}	1x10^{15}	1x10^{16}
Dose (ionizing part) [MRad]	80	50	1000
		Outer Barrel	Inner Barrel

→ **The HV-CMOS pixel sensors developed using commercial processes seem to be well suited for the ATLAS ITK upgrade, especially for the outer barrels**

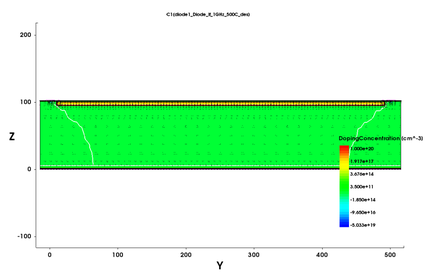
Sentaurus TCAD simulation of the charge collection diode



Cadence layout of the charge collection diode (GDS2 file)



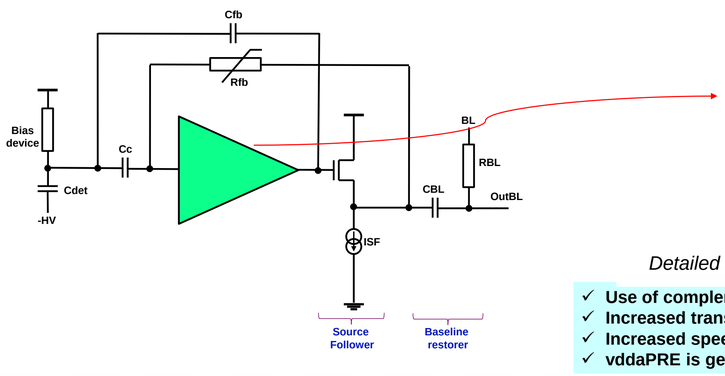
Reconstructed 3D structure of the diode

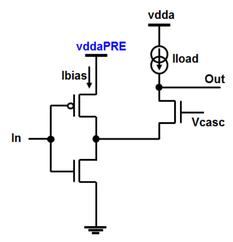


Simulation result for a backside thinned diode

Some critical parameters of the charge collection diode (diode capacitance, breakdown voltage, amount of collected charge) have been simulated and optimized using the Sentaurus TCAD software. The doping profile has been provided by the founder and the layout of the diode has been imported from Cadence software.

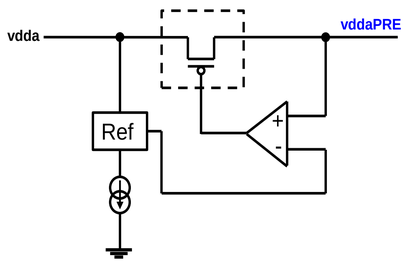
New CMOS-Input Preamp





Detailed schematic of the new CMOS-input preamp

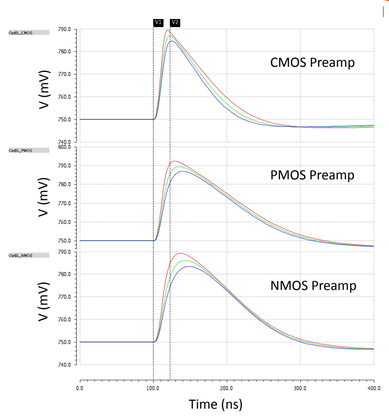
- ✓ **Use of complementary NMOS and PMOS input transistors**
- ✓ **Increased transconductance for a given bias current**
- ✓ **Increased speed and less noise**
- ✓ **vddaPRE is generated with an on-chip special bias circuitry**

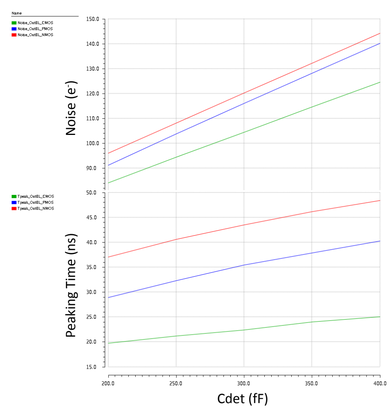


vddaPRE is generated with a special on-chip bias circuit which is a regulator.

- The reference circuit is a copy of the pixel CSA
- The error amplifier is an OTA
- The ballast transistor is distributed over the columns

Simulation Results



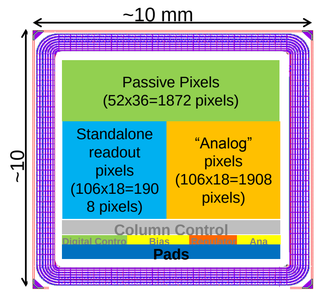


Transient simulation results showing the output signal of the preamplifier after the BL restorer (input of discriminator) for different detector capacitance values (obtained using the same bias current for the three amplifiers implemented in LFCPIX demonstrator).

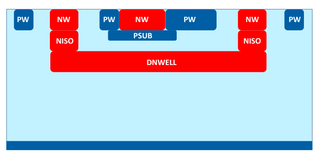
Simulated input referred noise and peaking time values for the three preamplifiers.

→ The CMOS-input preamplifier shows better performances in terms of speed, noise and power dissipation

Main Specifications of the LFCPIX Demonstrator



LFCPIX demonstrator

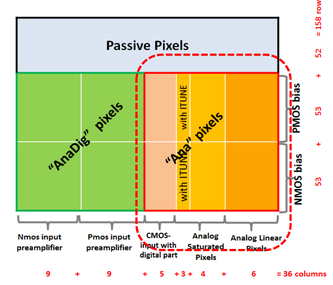


Cross section of LFCPIX pixel structure with CMOS electronics integrated inside charge collection diode

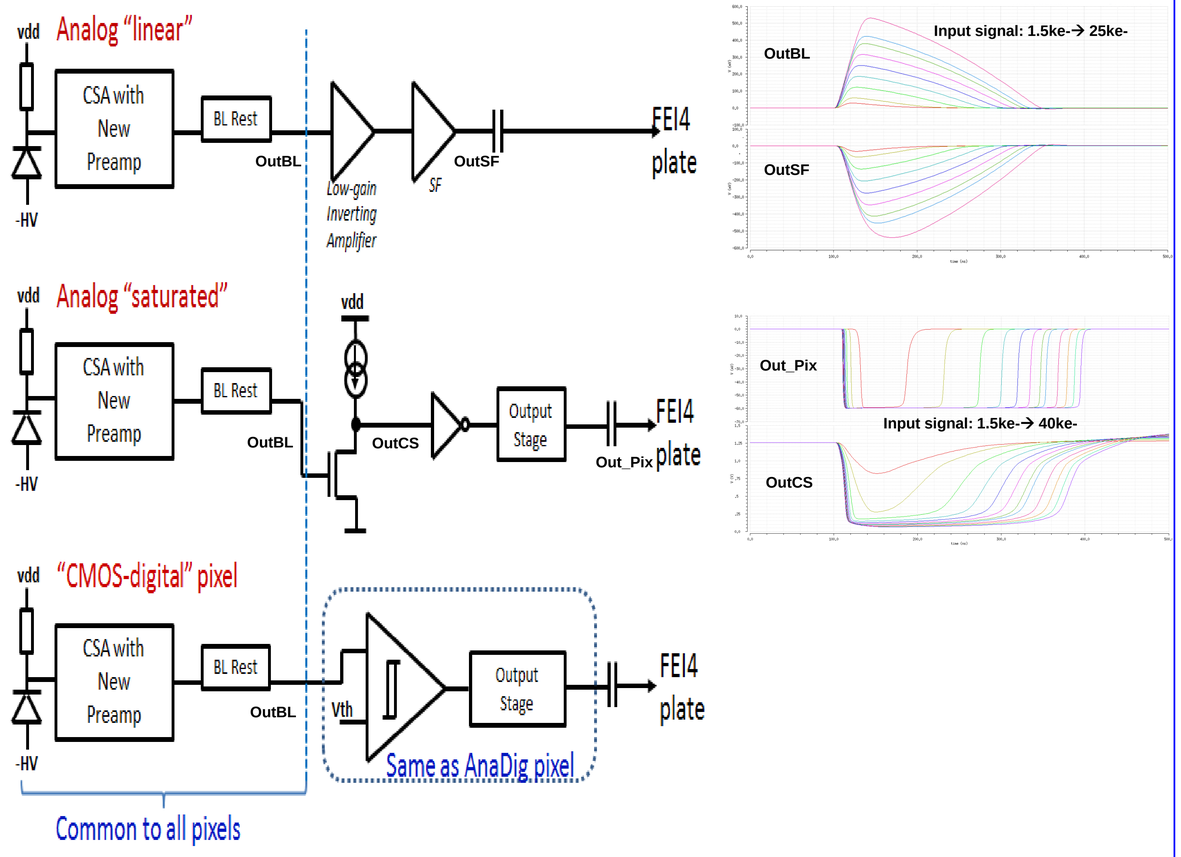
- ➢ **Process: LFoundry 150 nm HV-CMOS**
- ➢ **Use of HR (High Resistivity) substrates (~2kΩ.cm)**
- ➢ **CPPM, IRFU, Bonn collaboration**
- ➢ **Based on previous CCPD_LF prototypes (Bonn, CPPM coll.)**
- ➢ **Several FE-I4 compatible pixel flavors:**
  - **Passive (only charge collection diode)**
  - **Standalone readout digital pixels (diode + preamp + discri + local DAC + register)**
  - **"Analog" pixels (pixels with CMOS-input preamp, details given in the section below)**
- ➢ **Typical pixel properties:**
  - **pitch: 50 µmx 250 µm (FE-I4 pitch)**
  - **power dissipation: ~40 µW (analog)**
  - **electronics integrated inside charge collection diode**
  - **optimized version of CCPD_LF discriminator**
- ➢ **Programmable global configuration register**
- ➢ **Global and in-pixel DACs**
- ➢ **2 versions with different guard rings (increase of breakdown voltage)**
- ➢ **Submitted to fabrication in march 2016**

Pixel flavors implemented in the "Analog" Sub-array

Several pixel flavors have been implemented in the LFCPIX demonstrator. All these pixel are compatible with the FE-I4 readout chip (bump bonding or glue). Some of them are standalone readable without a readout chip. In the "Ana" pixels area, all pixels use the CMOS-input preamplifier. There are also digital pixels in this area. Two different bias schemes have been implemented for charge collection diodes.

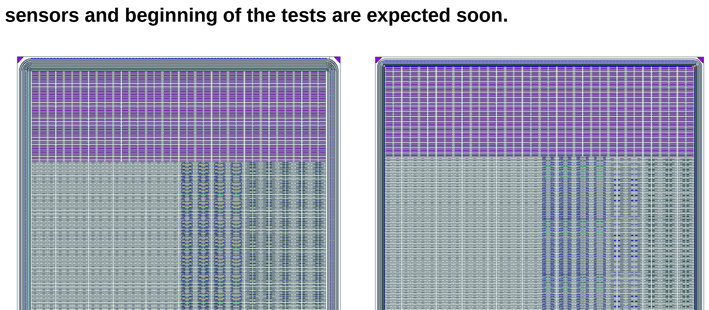


Placement of different pixel flavors in LF-CPIX



Prospects & Conclusions

- ➢ **A demonstrator chip (LFCPIX) has been designed and submitted to fabrication in the LFoundry 150 nm HV voltage process. The chip will be fabricated on HR wafers.**
- ➢ **Several pixel flavors have been implemented in this chip**
- ➢ **Three different preamplifier architectures (PMOS-input, NMOS-input and CMOS-input) have been implemented in this chip. According to the simulations, the new CMOS-input preamplifier allows low noise and increased speed compared with to the two others. The chip will allow the choice of the best preamplifier architecture.**
- ➢ **Several aspects of the demonstrator have been optimized in order to improve the critical parameters of the previous CCPD_LF prototypes such as breakdown voltage, noise, dispersion, time walk etc.**
- ➢ **All pixels are compatible with the FE-I4 readout chip. Some of them are also standalone readout paving the way for a fully monolithic CMOS sensor (they have already been used in the LF_MONOPIX-1 demonstrator).**
- ➢ **The fabricated sensors and beginning of the tests are expected soon.**



The layouts of the two LFCPIX chips (version 1 and 2) submitted to fabrication

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