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Pixel Architectures in HV/HR CMOS Process for ATLAS Inner Detector Upgrade

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Some pixel architectures designed in LFoundry 150 nm HV CMOS process for the ATLAS Inner Detector upgrade will be presented. These pixels can be readout standalone or can be connected to the FE-I4 readout chip via bump bonding or glue. Negative high voltage is applied to the HR (>2 kOhms.cm) substrate in order to deplete the DNW (Deep N-Well) charge collection diode, ensuring good charge collection and radiation tolerance. In these pixels, the front-end has been implemented inside the diode using both NMOS and PMOS transistors. The pixel pitch is 50 μmx250 μm for all pixels.

Summary

In this work, some pixels designed in LFoundry 150 nm HV CMOS process and implemented in a sensor demonstrator chip LFCPIX developed for the upgrade of the ATLAS Inner Detector will be presented. Modern CMOS processes offer multiple well structures in order to isolate the MOS transistors from the substrate. Thanks to this feature, it is possible to implement the pixel front-end electronics inside a DNW that forms also the cathode of a charge collection diode. It is possible to apply a high voltage (about -100 V) to the substrate without changing the operating parameters of the transistors.

Firstly, a new CSA (Charge Sensitive Amplifier) with complementary NMOS and PMOS input transistors has been proposed and designed for this pixels. The two input transistors contribute to the total transconductance of the input stage, improving speed and noise performances for a given power dissipation. Four different pixel flavors compatible with the input of the FE-I4 chip have been designed using all this new preamplifier.

The first pixel flavor generates a negative analog pulse proportional to the impinging particle. The signal is inverted using a low-gain amplifier. The second one generates a saturated negative pulse thanks to a high gain inverting amplifier. There is also a second version of this pixel with offset-correction of the amplifier using an in-pixel 4 bit DAC. The last pixel uses the classical approach using a preamplifier and a discriminator with in-pixel DAC based offset correction. The hits are memorized on a latch in the two last pixels.
The bias current of the preamplifier is ~14 μA, and the total bias current of the pixel is ~20 μA including the discriminating stage. Simulations show an input referred noise of ~130 e- and a peaking time ~20 ns. The TW (Time Walk) of the discriminator is less than 10 ns and needs a priori no TW compensation in this process.

All these pixels have been implemented in a demonstrator chip submitted to fabrication in March 2016. The pixel size is 50 μm x 250 μm for all pixels. The layout of the pixel has been optimized carefully to minimize coupling from digital signals into the collection diode. A special chip level bias circuit for the pixels was also designed and implemented in this chip. This circuit, which is a regulator, provides an adjustable bias current for all in-pixel preamplifiers.

The first preliminary experimental results of these pixels are expected at the time of the conference.

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