CATIROC

Charge And Time Integrated Read Out Chip

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CATIROC vs PARISROC

CATIROC is an upgraded version of **PARISROC2** designed to read huge photodetection areas for neutrinos experiments. This “System-on-Chip” is a very innovative concept as it sends out only relevant data by network to the central data storage turning the detector into a smart one.

CATIROC improvements:

- A new time measurement architecture built around a “fine time” and a “coarse time”
- The “coarse time” sped up by a factor of 4 with a 26-bit Gray Counter working at 40MHz
- The fine time with two TAC ramps for each channel
- Charge and time encoded by a 10-bit ADC at 160MHz (4 x faster then PARISROC2)
- Data sent-out in a data-driven way at 80 MHz (8 x faster then PARISROC2) on two lines (each one for 8 channels) which speeds up the data rate by a factor of 2

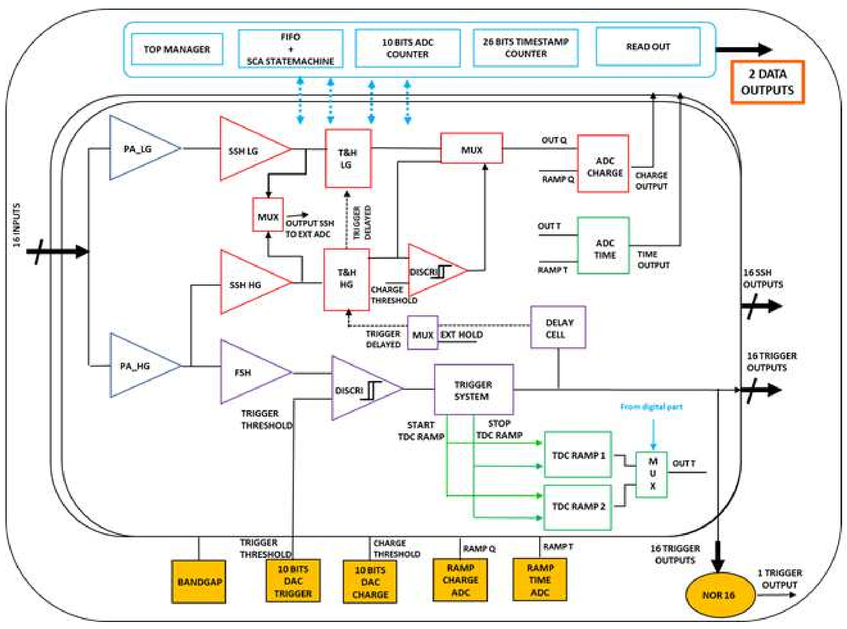
Specifications

- 16 independent channels
- Single photoelectron sensitive : Autotrigger mode
  - 100% trigger efficiency @ 1/3 p.e.
- Charge measurement :
  - Input range 160 fC -100 pC
- Time measurement:
  - Time stamp: 26 bits counter @ 40 MHz
  - Fine time: resolution < 500 ps
- Digital:
  - Conversion: 10 bits ADC at 160 MHz
  - Read out: 80 MHz
  - Read out frame: 50 bits
- Outputs:
  - 16 trigger outputs
  - NOR16
  - 16 slow shaper outputs
  - Charge measurement over 10 bits
  - Time measurement over 10 bits
- Data driven

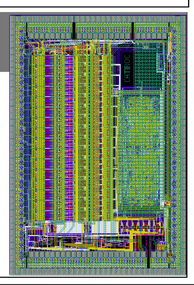
Architecture

- 16 inputs preamplifiers
  - 2 gain paths (high and low gain)
  - PMTs gain adjustment on 8 bits/ch
  - Input dynamic range : 160 fC to 100 pC
- Trigger channel
  - Fast shaper (t= 5ns)
  - Low offset discriminator
  - Threshold by common 10-bit DAC (50 fC);
  - “OR” of 16 triggers output.
- Charge channel:
  - Slow shaper CRRC2

  variable shaping time (t= 25ns, 50ns, 100ns)
  - SCA with depth 2
- Charge and fine time measurement :
  - 10 bit Wilkinson ADC
  - T&H on slow shaper for charge measurement
  - T&H on TAC ramp (25 ns) for fine time measurement
  - Coarse time measurement : timestamp with 25 ns step (40 MHz).
- Serialization of digital output information



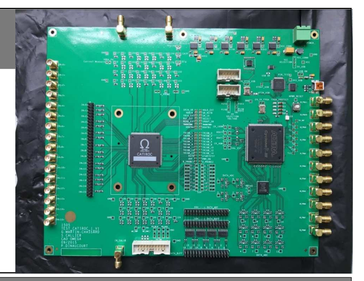
Chip status



- Submission: February 2015
- Process: AMS 0.35µm SiGe
- Die dimensions: 3.3mm x 4mm (13.2 mm²)
- Packaging: TQFP208
- Power supply: 0-3.3V
- Dissipation: 10 mW/ch

Test Board

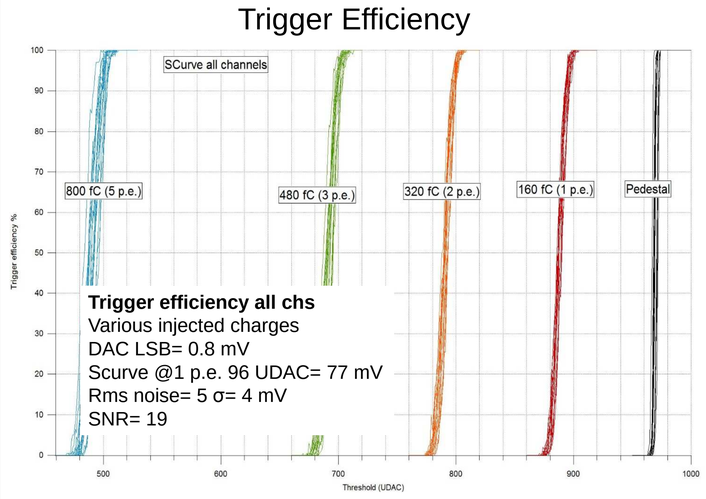
- 16 SMA connector input
- ASIC test pins
- 16 trigger outputs
- 16 ssh outputs
- An external 14-bit 16 channel ADC (ANALOG DEVICES)
- An FPGA Cyclone3
- USB interface
- Power supply
- ASIC CATIROC:
- 328 slow control bits
- Various digital signals



Measurements

Input charge made by a pulse generator:
1 p.e. = 160 fC @ PMT gain 10^6

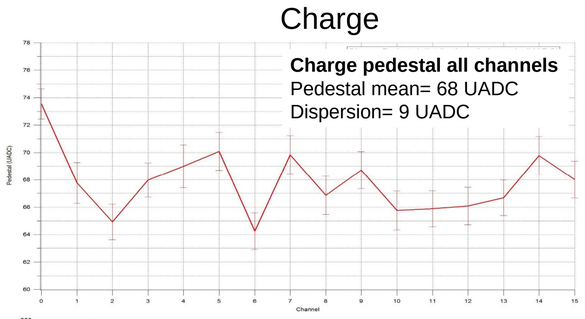
Trigger Efficiency



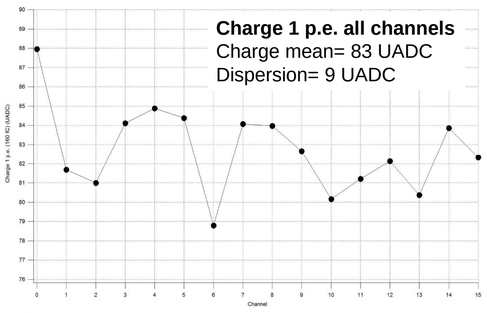
Trigger efficiency all chs
Various injected charges
DAC LSB= 0.8 mV
Scurve @1 p.e. 96 UDAC= 77 mV
Rms noise= 5 σ= 4 mV
SNR= 19

Trigger Efficiency ch0:
100% at 80 fC

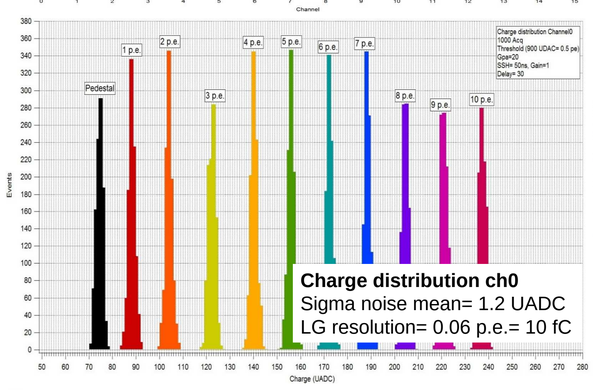
Charge



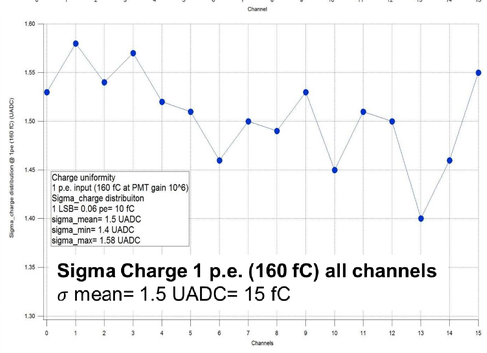
Charge pedestal all channels
Pedestal mean= 68 UADC
Dispersion= 9 UADC



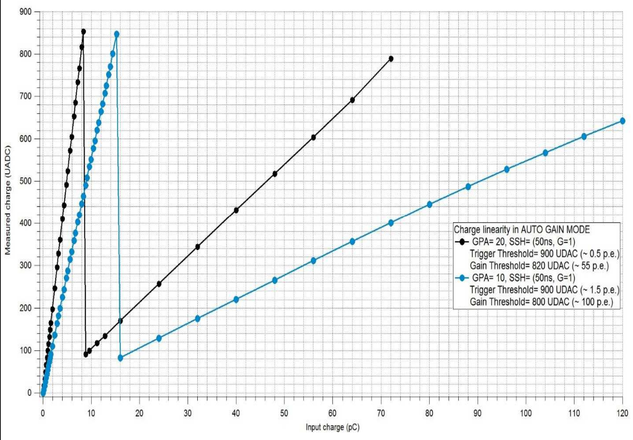
Charge 1 p.e. all channels
Charge mean= 83 UADC
Dispersion= 9 UADC



Charge distribution ch0
Sigma noise mean= 1.2 UADC
LG resolution= 0.06 p.e.= 10 fC



Sigma Charge 1 p.e. (160 fC) all channels
σ mean= 1.5 UADC= 15 fC



- **Charge linearity ch0 (PA_gain= 20);(ssh @ 50 ns, G=1):**

LG:
Trigger threshold= 0.5pe, Gain threshold= 55 p.e.
Residuals%: [-0.5, 1] % up to 70 pC
LSB= 0.5 p.e.= 80 fC

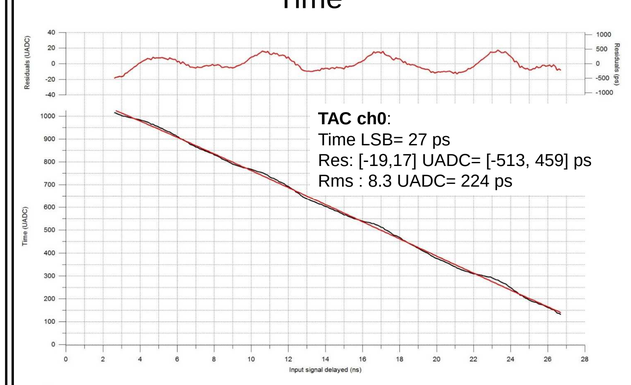
HG:
Trigger threshold= 0.5pe, Gain threshold= 55 p.e.
Residuals%: [-0.7, 0.5] % up to 9 pC
LSB= 0.06 p.e.= 10 fC

- **Charge linearity ch0 (PA_gain= 10);(ssh @ 50 ns, G=1):**

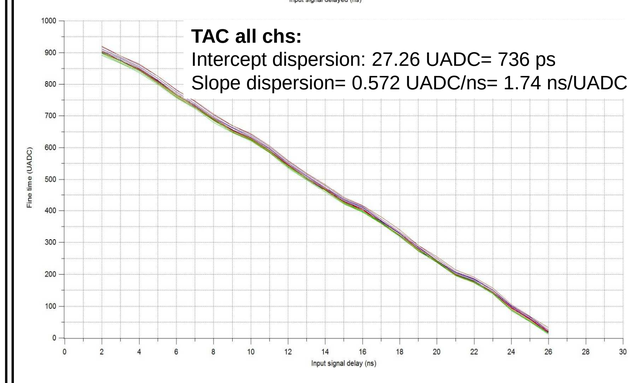
LG:
Trigger threshold= 1.5pe, Gain threshold= 100 p.e.
Residuals%: [-2.3, 1.3] % up to 120 pC
LSB= 1 p.e.= 160 fC

HG:
Trigger threshold= 1 pe, Gain threshold= 100 p.e.
Residuals%: [-0.4, 1] % up to 15 pC
LSB= 0.1 p.e.= 16 fC

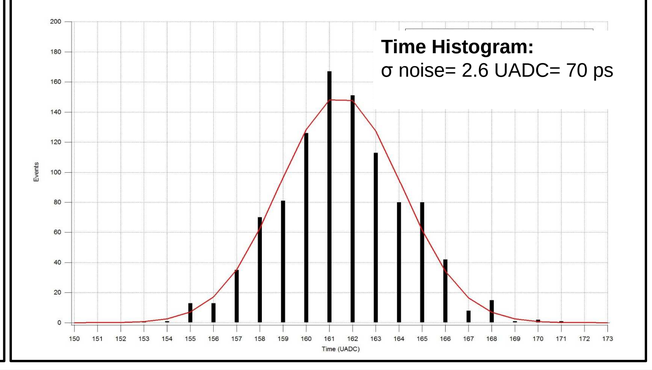
Time



TAC ch0:
Time LSB= 27 ps
Res: [-19,17] UADC= [-513, 459] ps
Rms : 8.3 UADC= 224 ps



TAC all chs:
Intercept dispersion: 27.26 UADC= 736 ps
Slope dispersion= 0.572 UADC/ns= 1.74 ns/UADC

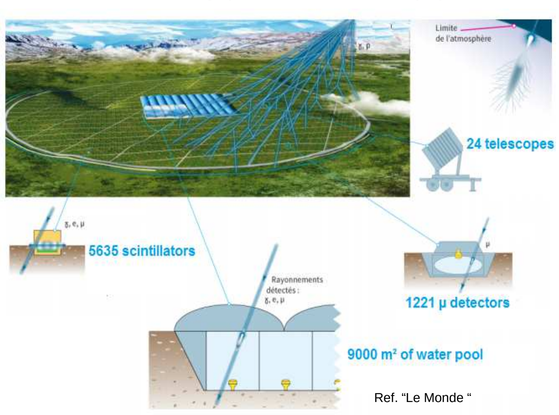


Time Histogram:
σ noise= 2.6 UADC= 70 ps

Experiments (CATIROC is under evaluation)

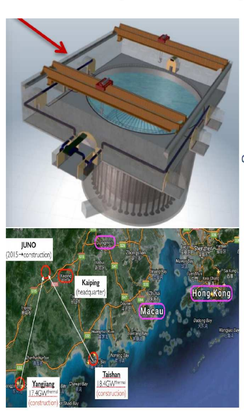
LHAASO: The Large High Altitude Air Shower Observatory (Cherenkov Telescope)

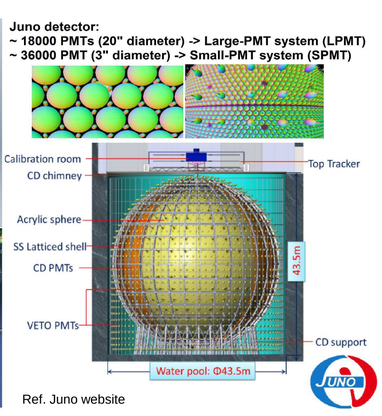
LHAASO CATIROC board prototype
IHEP-IPNO-OMEGA



Ref. “Le Monde “

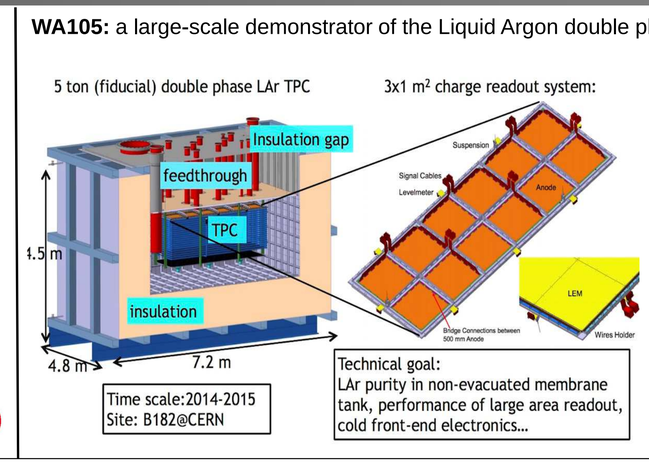
JUNO: Jiangmen Underground Neutrino Observatory (SPMTs)





Ref. Juno website

WA105: a large-scale demonstrator of the Liquid Argon double phase TPC



WA105 PARISROC2 board
APC-LAPP-OMEGA