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Performance of CATIROC: ASIC for Smart Readout of Large Photomultiplier Arrays

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CATIROC is an upgraded version of PARISROC2 designed to read huge photodetection areas for neutrinos experiments. This "System-on-Chip"is a very innovative concept as it sends out only relevant data by network to the central data storage turning the detector into a smart one. The ASIC integrates a self-triggering mode down to 50 fC which provides time measurement better than 1 ns and charge measurement up to 100 pC. Data are converted internally over 10 bits @160 MHz and read-out at 80 MHz.
The chip was produced in 2015; architecture and testbench measurements will be presented.

Summary

CATIROC is a successor of PARISROC2 with several improved features concerning the hit rate and the time measurement. PARISROC2 was designed in 2009 to readout huge photodetection areas of next generation neutrino experiments using water Cerenkov detectors, as continuation of the Super-Kamiokande family. Replacing large and onerous photodetectors by arrays of smaller ones is important to make the next generation of such detectors affordable. This relies on the integration of the front-end electronics on the array itself to turn it into a "smart sensor".
CATIROC is designed in AMS 0.35µm SiGe technology and keeps the same architecture as PARISROC2: it integrates 16 independent and self-triggered channels to provide charge and time measurements which are managed by a common digital part.
The main chip specifications are:
• An adjustable gain channel by channel
• Auto-trigger on 1/3 of photoelectron (p.e.) (50 fC at PM gain of 106)
• Charge measurement efficient for 1 p.e. and up to 600 p.e. (100 pC)
• 16 shaper outputs (enabling the use of an external ADC)
• 16 trigger outputs
• Time tagging better than 1 ns
• Internal ADC
• Serial data readout

The charge channel is made of a high and low gain voltage preamplifier followed by a variable slow shaper for small and large signals to ensure a good charge precision (˜ 30 fC). The two shaper signals are then stored in two analog memories (each one with a depth of two) working in a "ping-pong"mode in order to minimize the dead time during digitization: while a channel is digitized, the shaper output is sent to the second capacitor.
The time channel is made by the high gain preamplifier followed by a fast shaper (15 ns) and a discriminator. Thanks to a Time to Amplitude Converter (TAC), the signal is saved into an analog memory, in parallel with the charge, and is converted into digital data by the ADC. Significant modifications compared to Parisroc2 concern this timing branch. A new time measurement architecture built around a "fine time"and a "coarse time"has been implemented in CATIROC. The "coarse time"has been sped up by a factor of 4 with a 26-bit Gray Counter working at 40MHz. Two TAC ramps are sampled at the same time and an internal module tags the valid one: only the good time value is then converted.
Charge and time are then encoded by a 10-bit ADC at 160MHz (4 times faster compared to PARISROC2). The data are sent-out in a data-driven way at 80 MHz (8 times compared to PARISROC2) on two lines (each for 8 channels) which speeds up the data rate by a factor of 2.
A digital part manages all the acquisition, the conversion and the readout.

Several international experiments are interested by the ASIC such as the two Chinese projects LHAASO and JUNO, and the European project WA105.
CATIROC was received in September 2016. The architecture and the measurements will be detailed in the presentation.

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