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uTRiG: A Mixed Signal Silicon Photomultiplier Readout ASIC for Ultra-Fast Timing and Ultra-High Rate Applications

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We present the development of uTRiG, a mixed signal Silicon Photomultiplier readout ASIC in UMC 180nm CMOS technology, dedicated to the Mu3e experiment. It extends the ultra-fast timing performance of the STiCv3 chip with a fast digital readout for ultra-high rate applications. The high timing performance of the silicon proven, fully differential SiPM readout channels and 50 ps time binning TDCs are complemented by a redesigned digital readout logic and a gigabit data link, allowing event rates up to 1.3 MHz/channel. The design of uTRiG and the characterization results of the data link will be presented.

Summary

uTRiG is a mixed signal Silicon Photomultiplier (SiPM) readout ASIC in UMC 180nm CMOS technology, being developed for ultra-fast timing and ultra-high rate applications. The ASIC is dedicated to the readout of the tile detector and the fibre detector of the Mu3e experiment, which is searching for the lepton-flavour violating decay of $\mu^+ \rightarrow e^+e^+e^-$. To reduce the combinatorial background at high rates and to facilitate event reconstruction, a good timing resolution of 100 ps sigma and 500 ps sigma is required for the Mu3e tile detector and the Mu3e fibre detector, respectively. An event rate as high as 1.3 MHz/channel poses another challenge for the development of uTRiG.

uTRiG will feature 32 fully differential analog front-end channels, 50 ps time binning TDCs and a digital part to process and transfer the event data via a gigabit LVDS serial link with 8b/10b encoding to the Data Acquisition (DAQ) system. It benefits from the development of the STiCv3 ASIC by inheriting the analog front-end and the TDC, which both have been silicon-proven to provide excellent timing performance.

To cope with the high event rate, a customized LVDS transmitter cell has been developed to boost the data transmission rate of the chip to 1.28 Gbps. A single-ended to differential pre-driver and a Bridge-Switched Current Source LVDS driver with common-mode feedback have been implemented, both optimized for a gigabit data transmission rate using 1.8 V transistors. A prototype ASIC was fabricated in 2015 to validate the LVDS transmitter cell, also including a demonstrator digital part with a dual-edge serializer cell to transfer data at both the rising and the falling edge of the

driving clock. Preliminary tests has showed that the performance of the LVDS
data link exceeds the requirements of the Mu3e experiment.

An external validation functionality is also implemented
to reduce the load of the LVDS data link. The event data
recorded by the analog front-end and the TDC will stay in the FIFO
memory and will not be read out without an external validation signal.
The arrival of the external validation signal opens a matching window,
selecting the valid event data to be read out. The offset and the
width of the matching window is 1.6 us and 3.2 us at maximum
respectively. Both can be configured with a resolution of 200 ns. The
external validation functionality can be turned off such that all the
recorded data will be read out.

The design of uTRiG and the characterization results of the LVDS data link
will be presented.

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