Silicon micro-strips detectors are the baseline for the tracker region of the future International Linear Collider (ILC). Lately, variations of this type of sensors, like resistive micro-strips, Low Gain Avalanche Detectors (LGAD) and inverse LGAD (ILGAD) [1], have been presented to be considered as the technology for the future tracker.

ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout silicon micro-strips is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout [3], i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascade structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage. The CSA has programmable gain and a configurable input stage in order to adapt to the different strip flavours (resistive micro-strips, LGADs and ILGADs). The fabricated prototype is 0.866 mm x 0.965 mm and includes the biasing circuit for the CSA and shaper, 4 analog channels (CSA & Shaper) and programmable charge injection circuits included for testing purposes.

**Test and characterization**

ASIC:
- CSA gain of 8.86 mV/fC with feedback C = 100 fF
- Channel gain of 2.64 mV/fC with feedback C = 100 fF
- Vrms noise = 0.73 mV

Pixelated LGAD + ASIC:
- LGAD biased @ 420 V
- LGAD back illuminated
- Micro positioning and motors used to move LGAD board
- 100 μm pinhole

Appendix:
- Power supply: 1.8 V
- Power consumption x channel < 160 μW
- Optimum L and Ibias to maintain ENC below 100 e- with Cc of 25 fF
- CR-RC shaper with a folded cascade structure, Cs and Rs are passive

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