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Readout Electronics for Silicon Micro-Strip Sensors

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In the future ILC (International Large Detector), Silicon strip detectors will be used in the tracker to measure position and energy of the particles. A specific readout chip must be designed targeted to the accelerator operation and expected performance. A multichannel readout ASIC for Silicon microstrips in AMS 180nm technology has been fabricated. The main intended goals for this readout ASIC are low power, wide dynamic range, low noise and adaptability to different variety of silicon sensors. The details of the design to fulfil the requirements and the experimental results will be presented at the conference.

Summary

Silicon micro-strips detectors are the baseline for the tracker region of the future International Linear Collider (ILC). Lately, variations of this type of sensors, like resistive micro-strips, Low Gain Avalanche Detectors (LGAD) and inverse LGAD (iLGAD) [1], have been presented to be considered as the technology for the future tracker.

In this paper, an ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout silicon micro-strips is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout [2], i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascade structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage. The CSA has programmable gain and a configurable input stage in order to adapt to the different strip flavours (resistive micro-strips, LGADs and iLGADs). The fabricated prototype is 0.865 mm x 0.965 mm and includes the biasing circuit for the CSA and the shaper, 4 analog channels (CSA+shaper) and programmable charge injection circuits included for testing purposes.

The front-end is compliant with the ILC design regarding noise and power constraints. Power constraints require that all modules have to be designed with power-off capabilities and pulsed power mode of operation to match the ILC structure of operation. Furthermore, low power readout ASIC is required to avoid cooling systems inside the detector area. Noise constraints require to maintain a low equivalent noise charge (ENC), therefore special attention have been taken in the design of the preamplifier and the shaper as they are the dominant contribution of noise. Specifically, the main contribution of noise comes from the input transistor, the feedback capacitor of the CSA and the shaping time of the shaper. However, the addition of more elements to the readout circuit like the biasing circuit, input stage adaptors and the programmable gain increases the value of the ENC.

Noise and power analysis performed during simulation fixed the size of the input transistor in W/L =960 um/0.2 um. The shaping time is fixed by design at 1 us and, in this ASIC version, the feedback elements of the shaper are passive, which means that the area of the shaper can be reduced using active elements in future versions. Finally, the different gains of the CSA have been selected to maintain an ENC below 400 electrons for a detector capacitor of 20 pF, with a power consumption of 150 uW per channel.

[1] G. Pellegrini et al., “Recent Technological Developments on LGAD and iLGAD Detectors for Tracking and Timing Applications”, Instrumentation and detectors, arXiv:1511.07175.

[2] F. Anghinolfi et al., in: IEEE Transaction on nuclear science, vol. 49, nº 3, pp.1080-1085, 2002.

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