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ASPIC and CABAC: Two ASICs to Readout and Pilot CCD

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For several years, a group of engineers and physicists from LAL and LPNHE have been working on the design of two front end ASICs dedicated to Charge Couple Devices (CCD). ASPIC (Analogue Signal Processing Integrated Circuit), designed in AMS CMOS 0.35µm 5V technology, is meant to readout and process the analog signals of CCDs. CABAC (Clocks And Biases ASIC for CCDs), designed in AMS CMOS 0.35µm 50V technology, produces the clocks and biases needed by the CCDs to work at their full potential. This paper presents the performances of the final versions of these two ASICs.

Summary

The digital camera of the LSST (Large Synoptic Survey Telescope) project will be made of 189 CCDs of 4096x4096 pixels each. In order to pilot and readout these CCDs in parallel, two front end ASICs have been designed over the past 9 years taking into account the specific requirements of LSST experiment while being generic enough to be suitable for different types of CCD.
At first, the efforts were put on the design of the integrated circuit ASPIC (Analogue Signal Processing Integrated Circuit) dedicated to the readout and process simultaneously eight CCD output signals. It has been designed in AMS CMOS 0.35µm 5V « C35B4 » technology and mainly features an amplification of each one of the 8 input signals with a programmable gain and a correlated double sampling using a Dual Slope Integration which allows subtracting an important part of the noise. It took 7 years (2007 to 2014) and 3 versions of ASPIC to match the challenging specifications: 25 mW power dissipation, 0.5% linearity, 13 µV noise and 0.05 % crosstalk between channels. A fourth version was nonetheless designed and submitted in 2014 to improve some aspects of the circuit such as the substrate coupling between channels. This version showed good performances and worked as intended associated (or not) to a CCD. More than one thousand ASPIC4 have been produced in 2015 and will be tested in May-June 2016.
Since the end of 2011, another ASIC was designed by the group in parallel to ASPIC. It is named CABAC, which stands for Clocks And Biases ASIC for CCDs, and is meant to pilot the CCDs by providing different sets of clocks (4 parallel and 4 series) and biases (power of the output stage of the CCD and 3 polarizations). These parameters are highly configurable which allows tuning them efficiently for any type of CCD. Nevertheless the first version of CABAC (CABAC0) was developed taking the e2v CCD as a reference since it was the one that would most likely be used for LSST camera. It was also a safe way to start a design in a technology (AMS CMOS 0.35µm 50V « H35B4D3 ») never used at IN2P3. The tests showed encouraging results and useful experience. The second version of CABAC was almost a new prototype since it was developed in order to be compatible with another type of CCD, one working with negative voltages (contrary to e2v one). Unfortunately the tests carried out end of 2014 showed an excessive fragility of the ASIC despite satisfactory performances when all the precautions (complex power on sequence) were taken. Therefore a new version (CABAC2) was designed beginning of 2015 and tested in May 2015. The results, over a sample of 100 ASICs, showed a 95% yield. It was proven that all the clocks and biases could be adjusted finely.
The performances and the design of these two ASICs will be presented in this paper.

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